FEDL7716-06
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OKI Semiconductor

MSM7716

Single Rail Linear CODEC

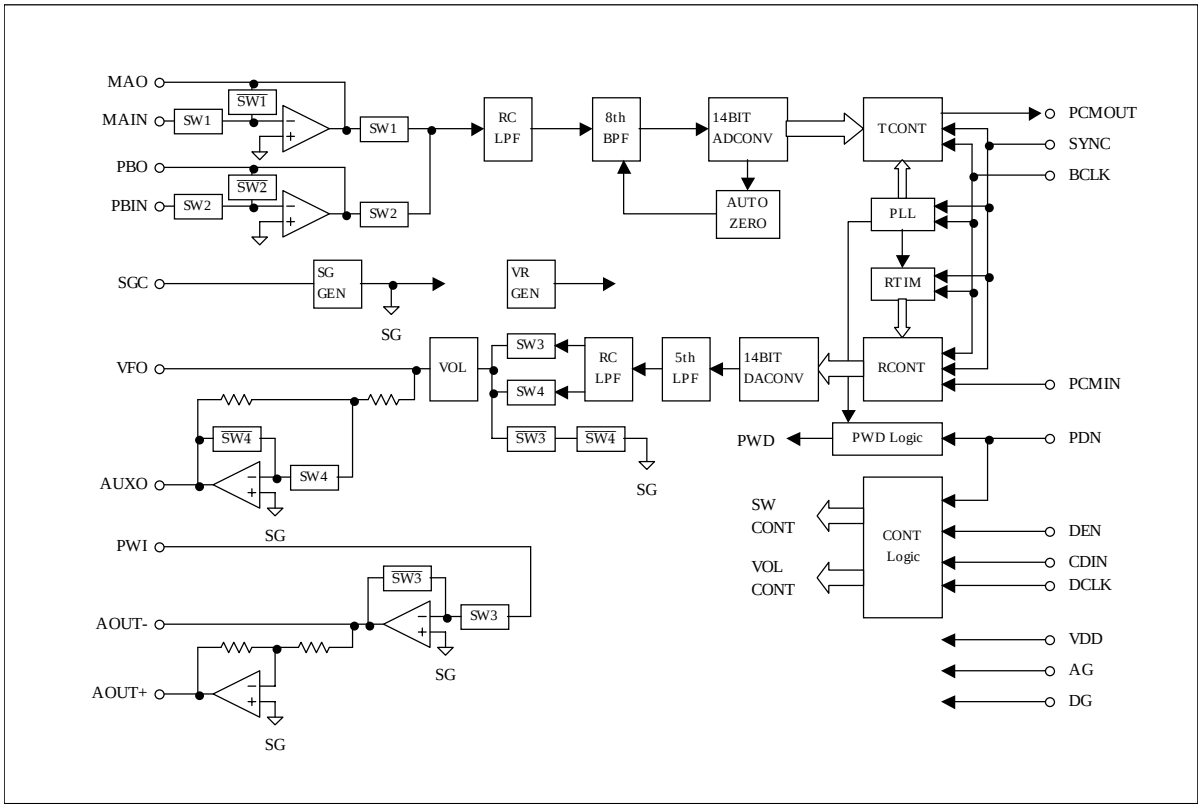
GENERAL DESCRIPTION

The MSM7716 is a single-channel CODEC CMOS IC for voice signals that contains filters for linear A/D and D/A conversion.
Designed especially for a single-power supply and low-power applications, the device is optimized for applications for the analog interfaces of audio signal processing DSPs and digital wireless systems.
The analog output signal can directly drive a ceramic type handset receiver. In addition, levels for analog outputs can be set by external control.

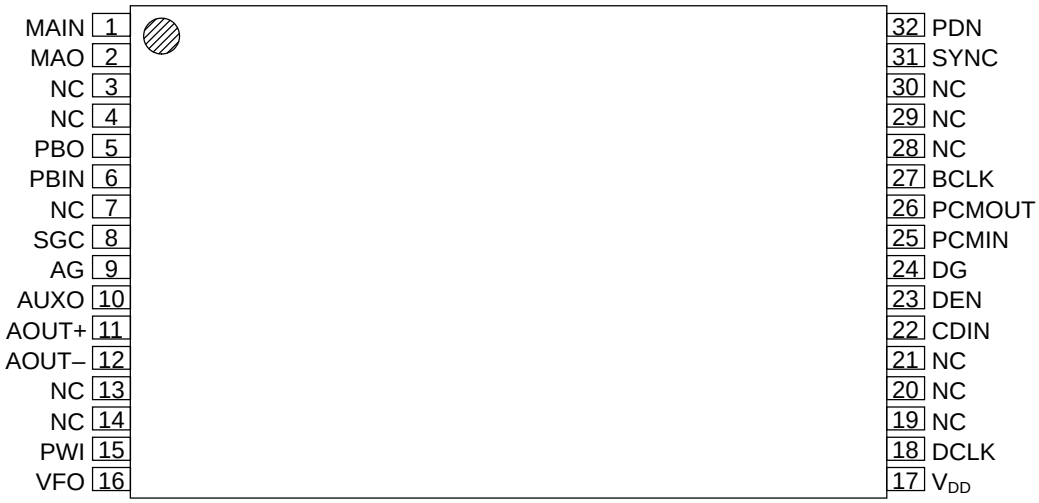
FEATURES

- Single power supply : +2.7V to +3.6 V
- Low power consumption
  Operating mode : 24 mW Typ.
  Power down mode : 0.05 mW Typ.
- Digital signal input/output interface : 14-bit serial code in 2's complement format
- Sampling frequency(fs) : 4 to 16 kHz
- Transmission clock frequency : fs × 14 min., 2048 kHz max.
- Filter characteristics : when fs = 8 kHz, complies with ITU-T Recommendation G. 714
- Built-in PLL eliminates a master clock
- Two input circuits in transmit section
- Two output circuits in receive section
- Transmit gain adjustable using an external resistor
- Receive gain adjustable by external control 8 steps, 4 dB/step
- Transmit mic-amp is eliminated by the gain setting of a maximum of 36 dB.
- Analog outputs can drive a load of a minimum of 1 kΩ ; an amplitude of a maximum of 4.0 V_{PP} with push-pull driving.
- Built-in reference voltage supply
- Package options:
  32-pin plastic TSOP (TSOP(1)32-P-814-0.50-1K) (MSM7716TS-K)
  30-pin plastic SSOP (SSOP30-P-56-0.65-K) (MSM7716GS-K)

BLOCK DIAGRAM

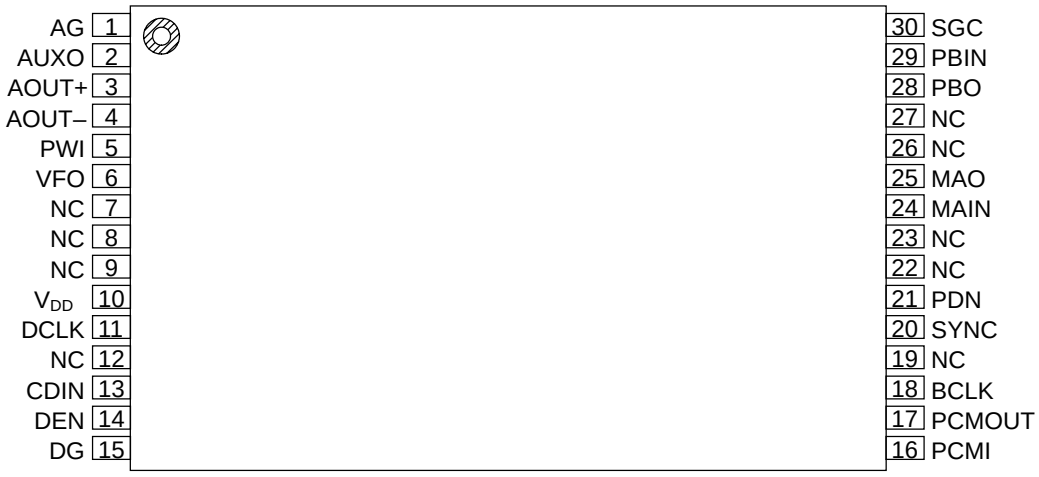


PIN CONFIGURATION (TOP VIEW)



NC : No connect pin

32-Pin Plastic TSOP



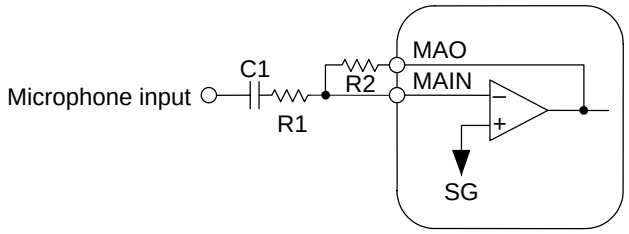
NC : No connect pin

30-Pin Plastic SSOP

PIN AND FUNCTIONAL DESCRIPTIONS

MAIN, MAO

Transmit microphone input and the level adjustment.
MAIN is connected to the noninverting input of the op-amp, and MAO is connected to the output of the op-amp. The level adjustment should be configured as shown below.
During power saving and power down modes, the MAO output is in high impedance state.

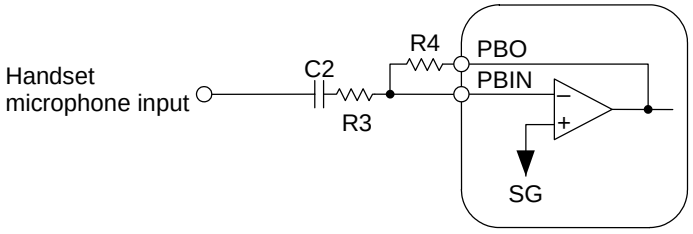


R1 : variable
R2 > 20 kΩ
C1 > 1/ (2 × 3.14 × 30 × R3) (F)

Gain = R2/R1 < 63

PBIN, PBO

Transmit handset input and the level adjustment.
PBIN is connected to the noninverting input of the op-amp, and PBO is connected to the output of the op-amp. The level adjustment should be configured as shown below.
During power saving and power down, the PBO output is in high impedance state.



R3 : variable
R4 > 20 kΩ
C2 > 1/ (2 × 3.14 × 30 × R3) (F)

Gain = R4/R3 < 63

V_{DD}

Power supply pin for +2.7 to 3.6 V (Typically 3.0 V).

AG

Analog signal ground.

DG

Ground pin for the digital signal circuits.
This ground is separated from the analog signal ground in this device. The DG pin must be connected to the AG pin on the printed circuit board.

VFO

Receive filter output.
The output signal has an amplitude of 2.0 V_{PP} above and below the signal ground voltage when the digital signal of +3 dBm0 is input to PCMIN. VFO can drive a load of 20 kΩ or more.
This output can be externally controlled in the level range of 0 to –28 dB in 4 dB increments.
During power saving or power down, VFO output is at the voltage level (V_{DD}/2) of SG with a high impedance state.

PWI, AOUT+, AOUT–

PWI is connected to the inverting input of the receive driver.
The receive driver output is connected to the AOUT– pin. Thus, a receive level can be adjusted with the pins PWI, AOUT–, and VFO described above.
The output of AOUT+ is inverted with respect to the output of AOUT– with a gain of 1.
The output signal amplitudes are a maximum of 2.0 V_{PP}.
These outputs, above and below the signal ground voltage (V_{DD}/2), can drive a load of a minimum of 1 kΩ with push-pull driving (a load connected between AOUT+ and AOUT–).
The output amplitudes are 4 V_{PP} maximum during push-pull driving. These outputs can be mute controlled externally. These outputs are operational during power saving and output the SG voltage (V_{DD}/2) in the high impedance state.

AUXO

Auxiliary receive filter output.
The output signal is inverted with respect to the VFO output with a gain of 1. The output signal swings above and below the SG voltage (V_{DD}/2), and can drive a minimum load of 0.5 kΩ with respect to the SG voltage.
The output can be mute controlled externally.
During power saving and power down, AUXO outputs the SG voltage (V_{DD}/2) in the high impedance state.

BCLK

Shift clock signal input for PCMIN and PCMOUT.
The frequency is equal to the data rate. Setting this signal to logic “1” or “0” drives both transmit and receive circuits to the power-saving state.

SYNC

Synchronizing signal input.
In the transmit section, the PCM output signal from the PCMOUT pin is output synchronously with this synchronizing signal. This synchronizing signal triggers the PLL and synchronizes all timing signals of the transmit section.
In the receive section, 14 bits required are selected from serial input of PCM signals on the PCMIN pin by the synchronizing signal.
Signals in the receive section are synchronized by this synchronizing signal. This signal must be synchronized in phase with the BCLK.
When this signal frequency is 8 kHz, the transmit and receive section have the frequency characteristics specified by ITU-T G. 714. The frequency characteristics for 8 kHz are specified in this data sheet.
For different frequencies of the SYNC signal, the frequency values in this data sheet should be translated according to the following equation:

$$\frac{\text{Frequency values described in the data sheet}}{8\ \text{kHz}} \times \text{the SYNC frequency values to be actually used}$$

Setting this signal to logic “1” or “0” drives the device to power-saving state.

PCMIN

PCM signal input.
A serial PCM signal input to this pin is converted to an analog signal synchronously with the SYNC signal and BCLK signal.
The data rate of the PCM signal is equal to the frequency of the BCLK signal.
The PCM signal is shifted at a falling edge of the BCLK signal. The PCM signal is latched into the internal register when shifted by 14 bits.
The top of the data (MSD) is identified at the rising edge of SYNC.
The input signal should be input in the 14-bit 2’s complement format.
The MSD bit represents the polarity of the signal with respect to the signal ground.

PCMOUT

PCM signal output.
The PCM output signal is output from MSD in sequential order, synchronously with the rising edge of the BCLK signal.
MSD may be output at the rising edge of the SYNC signal, depending on the timing between BCLK and SYNC.
This pin is in high impedance state except during 14-bit PCM output, and is in either in high impedance or in “L” output state during power down and power saving mode.
A pull-up resistor must be connected to this pin, because its output is configured as an open drain.
The output coding format is in 14-bit 2’s complement.
The MSD represents a polarity of the signal with respect to the signal ground.

Table 1

Input/Output Level	PCMIN/PCMOUT													
	MSD													
+Full scale	0	1	1	1	1	1	1	1	1	1	1	1	1	1
+1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
–1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
–Full scale	1	0	0	0	0	0	0	0	0	0	0	0	0	0

PDN

Power down control signal input.
A digital “L” level drives both transmit and receive circuits to a power down state.
The control registers are set to the initial state.
Be sure to initialize the control registers by to execute this power down by keeping this pin to digital '0' level for 100 ns or longer after the power is turned on the power and the V_{DD} exceeds 2.7 V.

SGC

Connection of a bypass capacitor for generating the signal ground voltage level.
Connect a 0.1 μF capacitor with excellent high frequency characteristics between the AG pin and the SGC pin.

DEN, DCLK, CDIN

Serial control ports for the microcontroller interface.
Writing data to the 8-bit control register enables control of the receive output level and the signal path.
DEN is the “Enable” signal pin, DCLK is the data shift clock input pin, and CDIN is the control data input pin.
When powered down (PDN = 0), the initial values are set as shown in Tables 2, 3, and 4. The initial values are held unless the control data is written after power-down release.
The control data is shifted at the rising edge of the DCLK signal and latched into the internal control register at the rising edge of the DEN signal.
When the microcontroller interface is not used, these pins should be connected to DG.
The bit map of the 8-bit control register is shown below.

B7	B6	B5	B4	B3	B2	B1	B0
SW1	SW2	SW3	SW4	—	VOL1	VOL2	VOL3

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	AG = DG = 0 V	–0.3 to +7.0	V
Analog Input Voltage	V_{AIN}	AG = DG = 0 V	–0.3 to V_{DD} +0.3	V
Digital Input Voltage	V_{DIN}	AG = DG = 0 V	–0.3 to V_{DD} +0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	2.7	3.0	3.6	V
Operating Temperature	Ta	—	–30	+25	+85	°C
Analog Input Voltage	V_{AIN}	Gain = 1	—	—	1.4	V_{PP}
High Level Input Voltage	V_{IH}	SYNC, BCLK, PCMIN, PDN, DEN, DCLK, CDIN	$0.45 \times V_{DD}$	—	V_{DD}	V
Low Level Input Voltage	V_{IL}		0	—	$0.16 \times V_{DD}$	V
Clock Frequency	F_C	BCLK	$14 \times F_S$	—	$128 \times F_S$	kHz
Sync Pulse Frequency	F_S	SYNC	4.0	8.0	16	kHz
Clock Duty Ratio	D_C	BCLK	40	50	60	%
Digital Input Rise Time	t_{lr}	SYNC, BCLK, PCMIN, PDN, DEN, DCLK, CDIN	—	—	50	ns
Digital Input Fall Time	t_{lf}		—	—	50	ns
Sync Pulse Setting Time	t_{XS}, t_{RS}	BCLK → SYNC, See Fig. 1	100	—	—	ns
	t_{SX}, t_{SR}	SYNC → BCLK, See Fig. 1	100	—	—	ns
High Level Sync Pulse Width *1	t_{WSH}	SYNC, See Fig. 1	1 BCLK	—	—	—
Low Level Sync Pulse Width *1	t_{WSL}	SYNC, See Fig. 1	1 BCLK	—	—	—
PCMIN Setup Time	t_{DS}	Refer to Fig. 1	100	—	—	ns
PCMIN Hold Time	t_{DH}	Refer to Fig. 1	100	—	—	ns
Digital Output Load	R_{DL}	Pull-up resistor	0.5	—	—	kΩ
	C_{DL}	—	—	—	100	pF
DCLK Pulse Width	t_{WCL}	DCLK Low width, See Fig. 2	50	—	—	ns
	t_{WCH}	DCLK High width, See Fig. 2	50	—	—	
DEN Setting Time 1	t_{CDL}	DCLK → DEN, See Fig. 2	50	—	—	ns
	t_{DCL}	DEN → DCLK, See Fig. 2	50	—	—	
DEN Setting Time 2	t_{CDH}	DCLK → DEN, See Fig. 2	50	—	—	ns
	t_{DCH}	DEN → DCLK, See Fig. 2	50	—	—	
CDIN Setup Time	t_{CDS}	See Fig. 2	50	—	—	ns
CDIN Hold Time	t_{CDH}	See Fig. 2	50	—	—	
Analog Input Allowable DC Offset	V_{off}	Transmit gain stage, Gain = 0 dB	–100	—	+100	mV
		Transmit gain stage, Gain = 20 dB	–10	—	+10	mV
Allowable Jitter Width	—	SYNC, BCLK	—	—	1000	ns

*1 For example, the minimum pulse width of SYNC is 488 ns when the frequency of BCLK is 2048 kHz.

RECOMMENDED OPERATING CONDITIONS (Continued)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital Output Delay Time	t_{SD}	CL = 50 pF + 1 LSTTL Pull-up resistor = 500 Ω	20	—	100	ns
	t_{XD1}		20	—	100	
	t_{XD2}		20	—	100	
	t_{XD3}		20	—	100	

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(Fs = 8 kHz, V_{DD} = 2.7 to 3.6 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating mode No signal	V_{DD} = 3.6 V	—	10.0	17.0	mA
			V_{DD} = 3.0 V	—	8.0	13.0	
	I_{DD2}	Power-saving mode, PDN = 1, SYNC, BCLK → OFF		—	6.0	11.0	mA
	I_{DD3}	Power-down mode, PDN = 0		—	0.01	0.05	mA
High Level Input Voltage	V_{IH}	SYNC, BCLK, PCMIN, DEN, CDIN, DCLK, PDN		$0.45 \times V_{DD}$	—	V_{DD}	V
Low Level Input Voltage	V_{IL}			0.0	—	$0.16 \times V_{DD}$	V
High Level Input Leakage Current	I_{IH}	—		—	—	2.0	μA
Low Level Input Leakage Current	I_{IL}	—		—	—	0.5	μA
Digital Output Low Voltage	V_{OL}	PCMOUT pull-up resistor = 500 Ω		0.0	0.2	0.4	V
Digital Output Leakage Current	I_O	—		—	—	10	μA
Input Capacitance	C_{IN}	—		—	5	—	pF

Transmit Analog Interface Characteristics

(Fs = 8 kHz, V_{DD} = 2.7 to 3.6 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Input Resistance	R_{INX}	MAIN, PBIN		10	—	—	MΩ
Output Load Resistance	R_{LGX}	MAO, PBO with respect to SG		20	—	—	kΩ
Output Load Capacitance	C_{LGX}			—	—	30	pF
Output Amplitude	V_{OGX}			–0.7	—	+0.7	V
Offset Voltage	V_{OSGX}		Gain = 1	–20	—	+20	mV

Receive Analog Interface Characteristics

(Fs = 8 kHz, V_{DD} = 2.7 to 3.6 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Resistance	R_{OAO}	AUXO, AOUT+, AOUT–	—	—	10	Ω
	R_{OVO}	VFO	—	—	100	Ω
Output Load Resistance	R_{LAO}	AUXO, AOUT+, AOUT– (each) with respect to SG	0.5	—	—	kΩ
	R_{LVO}	VFO with respect to SG	20	—	—	kΩ
Output Load Capacitance	C_{LAO}	Output open	—	—	50	pF
Output Amplitude	V_{OAO}	AUXO, AOUT+, AOUT–, VFO with respect to SG	–1.0	—	+1.0	V
Offset Voltage	V_{OSA}	AUXO, AOUT+, AOUT–, VFO with respect to SG	–100	—	+100	mV

AC Characteristics

(F_S = 8 kHz, V_{DD} = 2.7 to 3.6 V, Ta = –30 to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Overall Frequency Response	Loss 1	60	0	Analog to Analog	20	—	—	dB
	Loss 2	300			–0.2	—	+0.4	
	Loss 3	1020			Reference			
	Loss 4	2020			–0.2	—	+0.4	
	Loss 5	3000			–0.2	—	+0.4	
	Loss 6	3400			0	—	1.6	
Transmit Frequency Response (Expected Value)	Loss T1	60	0		20	—	—	dB
	Loss T2	300			–0.15	—	+0.2	
	Loss T3	1020			Reference			
	Loss T4	2020			–0.15	—	+0.2	
	Loss T5	3000			–0.15	—	+0.2	
	Loss T6	3400			0	—	0.8	
Receive Frequency Response (Expected Value)	Loss R1	300	0		–0.15	—	+0.2	dB
	Loss R2	1020			Reference			
	Loss R3	2020			–0.15	—	+0.2	
	Loss R4	3000			–0.15	—	+0.2	
	Loss R5	3400			0.0	—	0.8	
Overall Signal to Distortion Ratio	SD 1	1020	3	Analog to Analog *1	55.9	—	—	dB
	SD 2		0		55.9	—	—	
	SD 3		–10		55.9	—	—	
	SD 4		–20		45.9	—	—	
	SD 5		–30		35.9	—	—	
	SD 6		–40		25.9	—	—	
	SD 7		–50		15.9	—	—	
Transmit Signal to Distortion Ratio (Expected Value)	SD T1	1020	3	*1	58	—	—	dB
	SD T2		0		58	—	—	
	SD T3		–10		58	—	—	
	SD T4		–20		48	—	—	
	SD T5		–30		38	—	—	
	SD T6		–40		28	—	—	
	SD T7		–50		18	—	—	
Receive Signal to Distortion Ratio (Expected Value)	SD R1	1020	3	*1	58	—	—	dB
	SD R2		0		58	—	—	
	SD R3		–10		58	—	—	
	SD R4		–20		48	—	—	
	SD R5		–30		38	—	—	
	SD R6		–40		28	—	—	
	SD R7		–50		18	—	—	

*1 Psophometric filter is used.

AC Characteristics (Continued)

(F_S = 8 kHz, V_{DD} = 2.7 to 3.6 V, Ta = –30 to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Overall Gain Tracking	GT 1	1020	3	Analog to Analog	–0.4	+0.01	+0.4	dB
	GT 2		–10		Reference			
	GT 3		–40		–0.3	0.00	+0.8	
	GT 4		–50		–1.3	–0.03	+1.3	
	GT 5		–55		–1.6	–0.15	+1.6	
Transmit Gain Tracking (Expected Value)	GT T1	1020	3		–0.3	+0.01	+0.3	dB
	GT T2		–10		Reference			
	GT T3		–40		–0.3	0.00	+0.3	
	GT T4		–50		–0.6	–0.03	+0.6	
	GT T5		–55		–1.2	+0.15	+1.2	
Receive Gain Tracking (Expected Value)	GT R1	1020	3		–0.3	–0.06	+0.3	dB
	GT R2		–10		Reference			
	GT R3		–40		–0.3	–0.02	+0.3	
	GT R4		–50		–0.6	–0.02	+0.6	
	GT R5		–55		–1.2	–0.27	+1.2	

AC Characteristics (Continued)

(F_S = 8 kHz, V_{DD} = 2.7 to 3.6 V, Ta = –30 to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Overall Idle Channel Noise	Nidle A	—	—	AIN: no signal *1	—	–70	–66	dBm0p
Transmit Idle Channel Noise (Expected Value)	Nidle T	—	—	AIN: no signal *1	—	–71	–67	dBm0p
Receive Idle Channel Noise (Expected Value)	Nidle R	—	—		—	–76	–74	
Absolute Level (Initial Level)	AV T	1020	0	V_{DD}=3.0 V Ta=25°C *2	0.338	0.350	0.362	Vrms
	AV R				0.483	0.500	0.518	
Absolute Level (Deviation of Temperature and Power)	AV Tt			V_{DD} = +2.7 to 3.6 V Ta = –30 to 85°C	–0.2	—	+0.2	dB
	AV Rt				–0.2	—	+0.2	dB
Absolute Delay	t_D	1020	0	A to A BCLK = 64 kHz	—	—	0.6	ms
Transmit Group Delay	t_{GD} T1	500	0	*3	—	—	0.325	ms
	t_{GD} T2	600 to 2600			—	—	0.175	
	t_{GD} T3	2800			—	—	0.325	
Receive Group Delay	t_{GD} R1	500 to 2600	0	*3	—	0.00	0.125	ms
	t_{GD} R2	2800			—	0.12	0.325	
Crosstalk Attenuation	CR T	1020	0	TRANS→RECV	75	85	—	dB
	CR R			RECV→TRANS	70	80	—	

*1 Psophometric filter is used.
*2 AVT is defined at MAO and PBO-PCMOUT.
AVR is defined at PCMIN-VFO.
VOL = 0 dB
*3 Minimum value of the group delay distortion

AC Characteristics (Continued)

(F_S = 8 kHz, V_{DD} = 2.7 to 3.6 V, Ta = –30 to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Discrimination	DIS	4.6 to 72 kHz	0	0 to 4000 Hz	30	32	—	dB
Out-of-band Spurious	S	300 to 3400	0	4.6 to 100 kHz	—	–37.5	–35	dBm0
Intermodulation Distortion	IMD	fa = 470 fb = 320	–4	2fa – fb	—	–52	–40	dBm0
Power Supply Noise Rejection Ratio	PSR T	0 to 50 kHz	50 mV_{PP}	*1	—	30	—	dB
	PSR R							
Auxiliary Output Gain	G_{AUX}	1020	0	VFO to AUXO	–1.0	0	+1.0	dB
VOL Gain Setting Value	G_{V2}	1020	0	Set at –4 dB	–5	–4	–3	dB
	G_{V3}			–8 dB	–9	–8	–7	
	G_{V4}			-12 dB	–13	–12	–11	
	G_{V5}			-16 dB	–17	–16	–15	
	G_{V6}			-20 dB	–21	–20	–19	
	G_{V7}			-24 dB	–25	–24	–23	
	G_{V8}			-28 dB	–29	–28	–27	

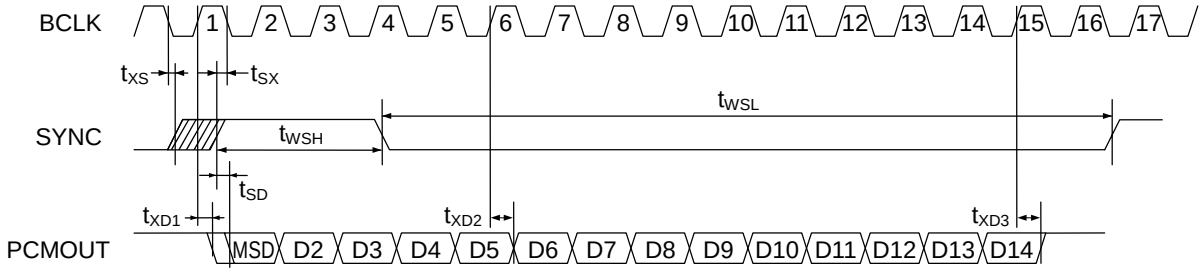
Referenced to 0 dB setting

*1 Measured inband.

TIMING DIAGRAM

PCM Data Output Timing

Transmit Timing



When $t_{XS} \leq 1/2 \bullet Fc$, the Delay of the MSD bit is defined as t_{XD1}.
When $t_{SX} < 1/2 \bullet Fc$, the Delay of the MSD bit is defined as t_{SD}.

Receive Timing

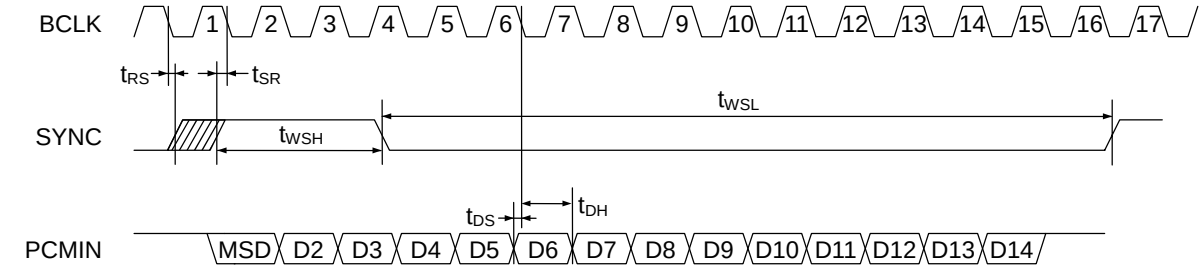


Figure 1 Basic Timing Diagram

MCU Interface Timing

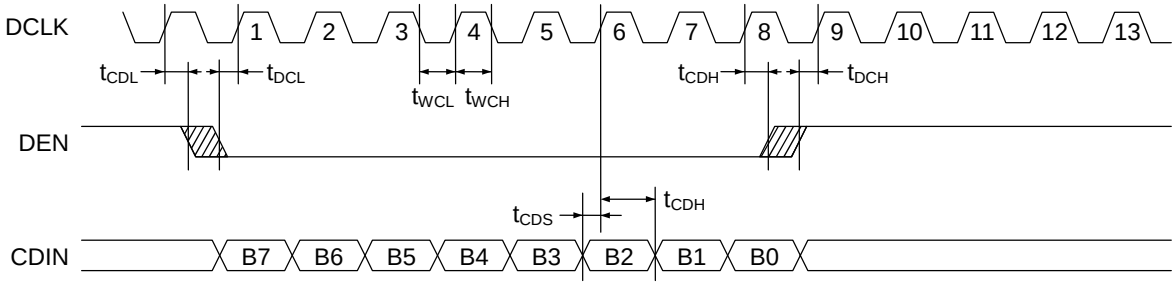


Figure 2 MCU Interface Timing Diagram

FUNCTIONAL DESCRIPTION

Control Data Description

SW1, SW2·····Control bits for the transmit speech path switch.
The AD converter input is selected according to the bit data shown in Table 2.

Table 2

State	SW 2	SW 1	AD Converter Input	MAO Output	PBO Output	Remarks
T1	0	0	No signal (muting state)	SG	SG	—
T2	0	1	Input signal to MAIN	Effective	SG	At initial setting
T3	1	0	Input signal to PBIN	SG	Effective	—
T4	1	1	Addition signal of both MAIN and PBIN	Effective	Effective	The gain of each input drops by 6dB

SW3, SW4·····Control bits for the receive speech path switch.
The control should be performed according to Table 3.

Table 3

State	SW4	SW3	AOUT+, AOUT– Output	AUXO Output	Remarks
R1	0	0	SG	SG	—
R2	0	1	PWI	SG	At initial setting
R3	1	0	SG	DA	—
R4	1	1	PWI	DA	—

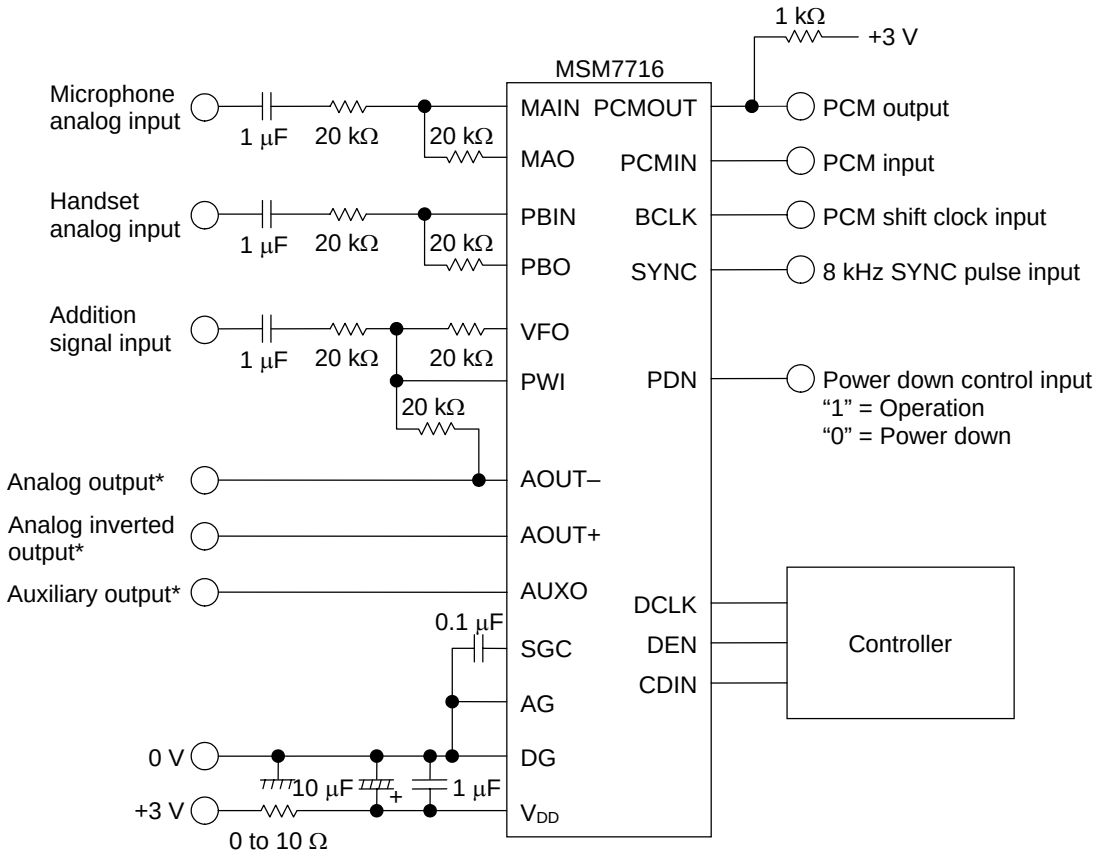
DA: DA converter output. SG: signal ground voltage.

VOL1, VOL2, VOL3·····Control bits for the receive signal output level.
By controlling these bits, the output levels of VFO and AUXO can be controlled according to Table 4.

Table 4

VOL1	VOL2	VOL3	Receive Signal Gain	Remarks
0	0	0	0 dB	At initial setting
0	0	1	–4 dB	—
0	1	0	–8 dB	—
0	1	1	–12 dB	—
1	0	0	–16 dB	—
1	0	1	–20 dB	—
1	1	0	–24 dB	—
1	1	1	–28 dB	—

APPLICATION CIRCUIT

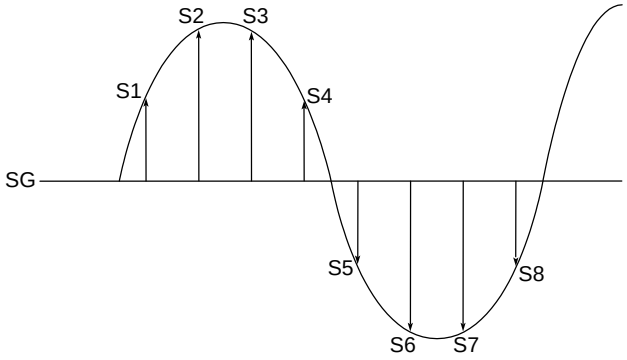


* The swing of the analog output signal is a maximum of ±1.0 V above and below the $V_{DD}/2$ offset level.

APPLICATION INFORMATION

Digital pattern for 0 dBm0

The digital pattern for 0 dBm0 is shown below.
(SYNC frequency = 8 kHz, signal frequency = 1 kHz)



Sample No.	MSD	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14
S1	0	0	1	0	0	0	1	0	1	0	1	0	1	1
S2	0	1	0	1	0	0	1	1	1	0	1	1	1	0
S3	0	1	0	1	0	0	1	1	1	0	1	1	1	0
S4	0	0	1	0	0	0	1	0	1	0	1	0	1	1
S5	1	1	0	1	1	1	0	1	0	1	0	1	0	0
S6	1	0	1	0	1	1	0	0	0	1	0	0	0	1
S7	1	0	1	0	1	1	0	0	0	1	0	0	0	1
S8	1	1	0	1	1	1	0	1	0	1	0	1	0	0

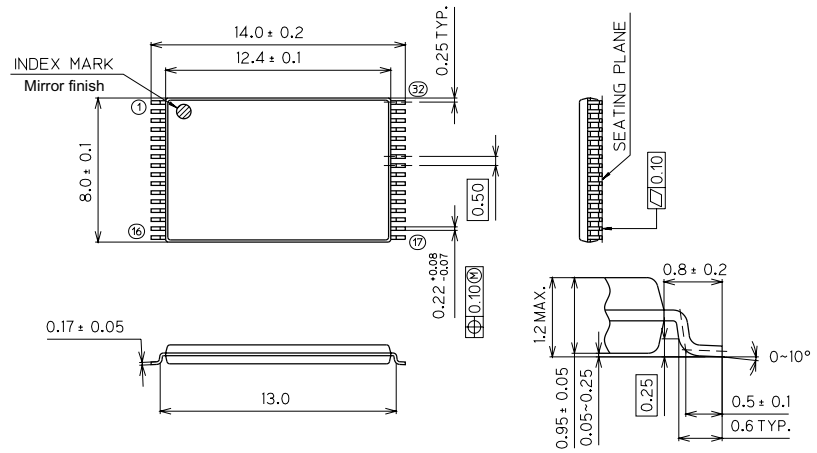
NOTES ON USE

- To ensure proper electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.
- Connect the AG pin and the DG pin as close as possible. Connect to the system ground with low impedance.
- Mount the device directly on the board when mounted on PCBs. Do not use IC sockets. If the use of IC socket is unavoidable, use the short lead type socket.
- When mounted on a frame, use electro-magnetic shielding, if any electro-magnetic wave sources such as power supply transformers surround the device.
- Keep the voltage on the V_{DD} pin not lower than –0.3 V even instantaneously to avoid latch-up that may otherwise occur when power is turned on.
- Use a low noise (particularly, low level type of high frequency spike noise or pulse noise) power supply to avoid erroneous operation and the degradation of the characteristics of these devices.

PACKAGE DIMENSIONS

(Unit: mm)

TSOP(1)32-P-0814-0.50-1K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.27 TYP.
Rev. No./Last Revised	3/Dec. 10, 1996

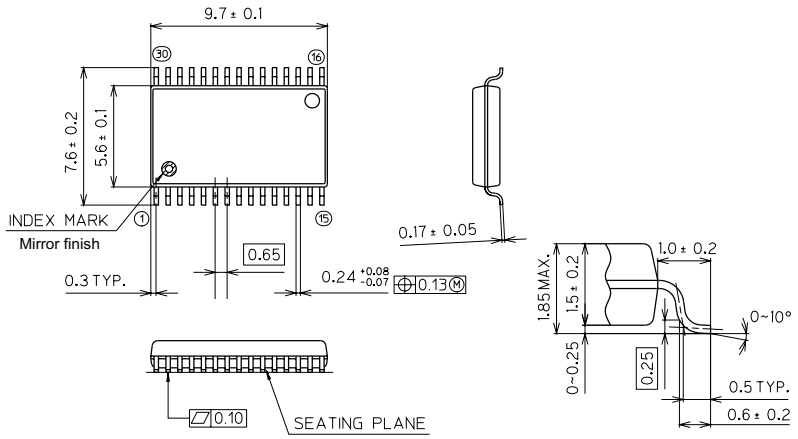
Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit: mm)

SSOP30-P-56-0.65-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.19 TYP.
Rev. No./Last Revised	5/Dec. 5, 1996

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Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7716-04	Jan 7, 2003	–	–	Final edition 4
		2	2	Correction of SW3/4 insertion
FEDL7716-05	Jun 5, 2003	7	7	Correction of PCMOUT output during power down and power saving mode
		14	14	Correction of Receive Idle Channel Noise
FEDL7716-06	Jun 17, 2004	2	2	Correction of SW1/2 insertion
		17	17	- Addition of attenuation level to remarks for T4 setting in Table 2 - Addition of MAO and PBO State in Table 2

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