OKI Semiconductor

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MSM6895/6896

Multi-Function PCM CODEC

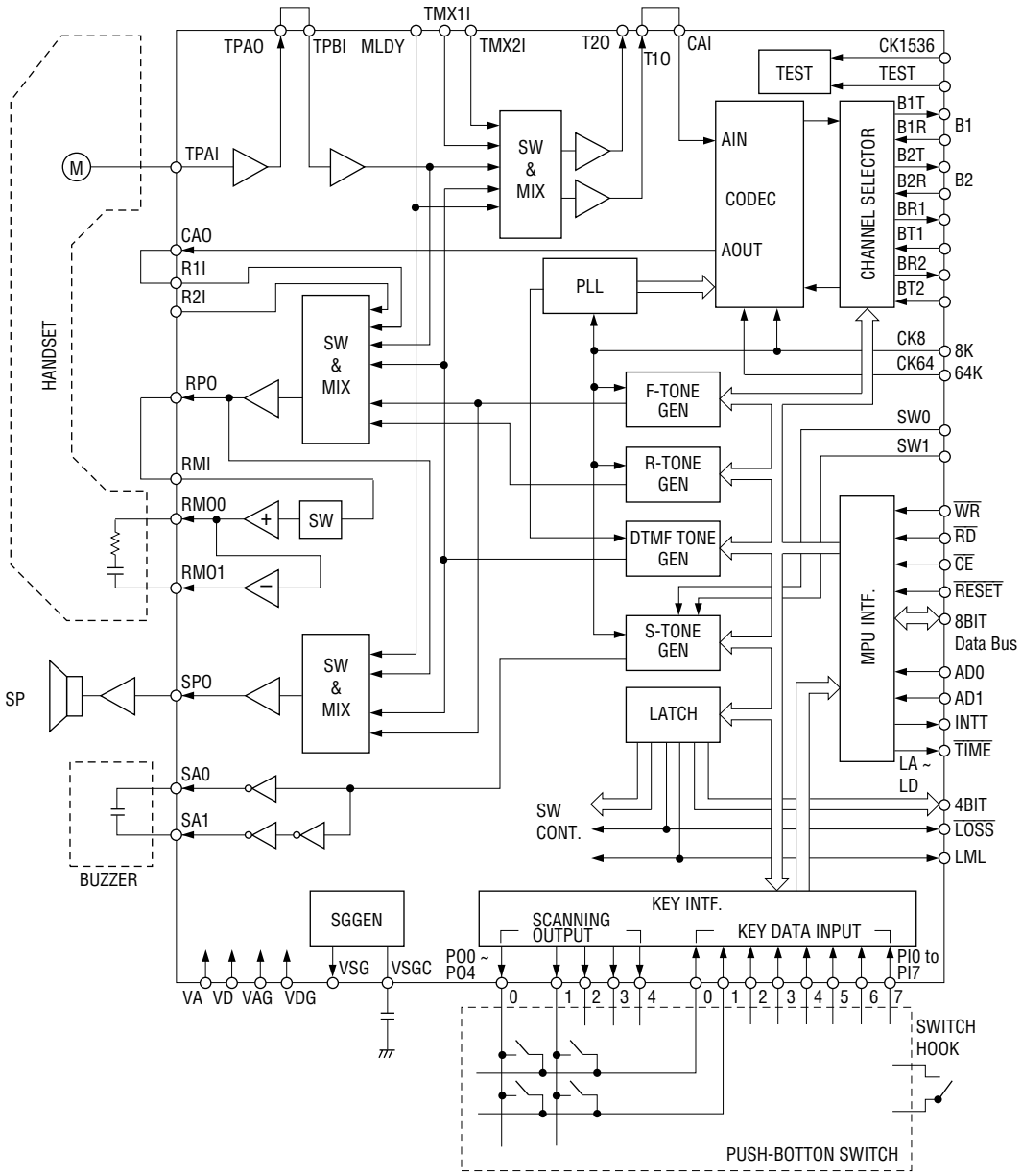
GENERAL DESCRIPTION

The MSM6895/MSM6896, developed especially for low-power and multi-function applications in ISDN telephone terminals, are single +5 V power supply CODEC LSI devices. The devices consist of the analog speech paths directly connectable to a handset, the calling circuit directly connectable to a piezosounder, the push-button key scanning interface between push buttons and control processors, the dial tone generator, the B-channel interface, the CODEC, and the processor interface. The functions can be controlled via the 8-bit data bus.

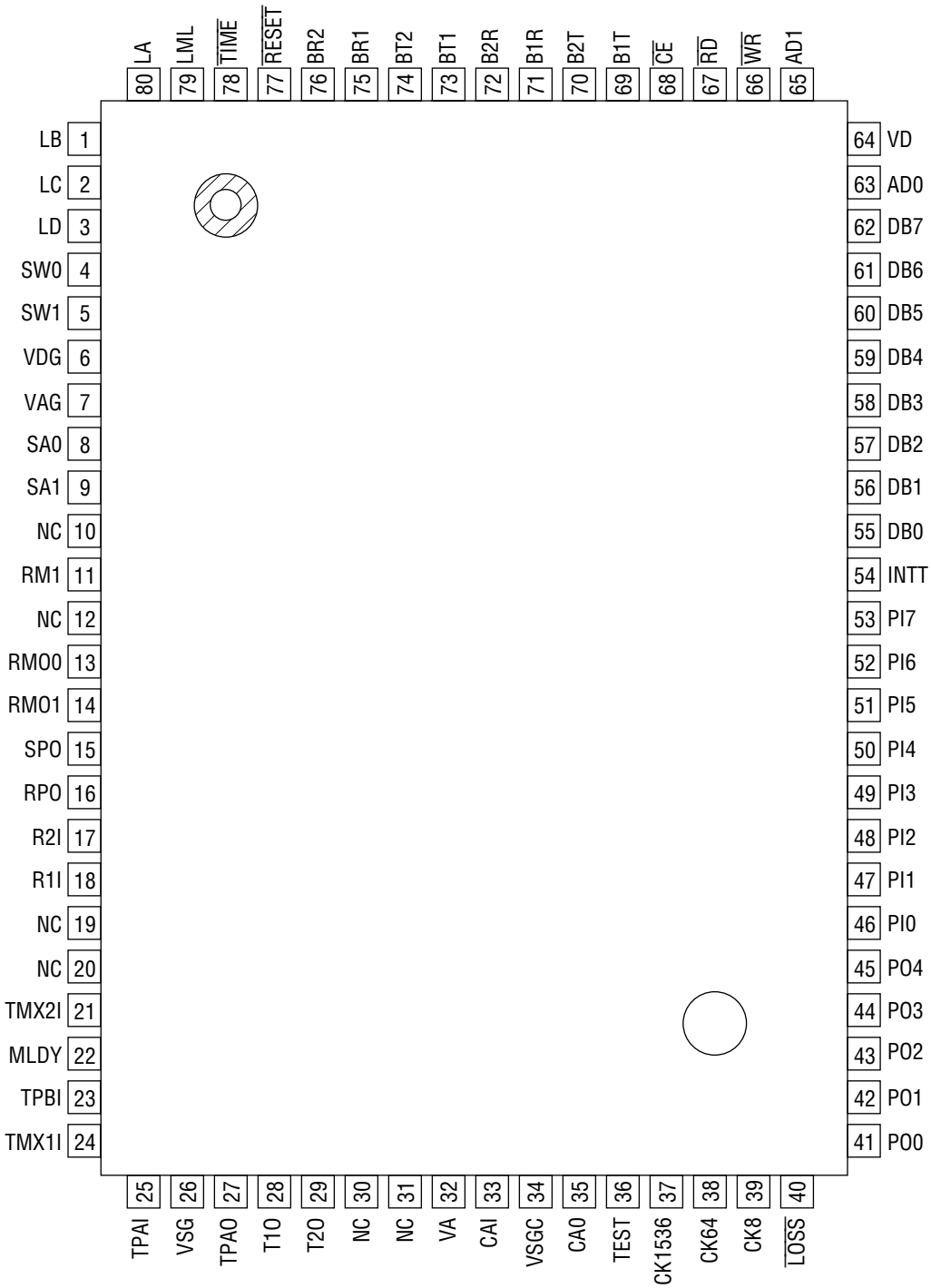
FEATURES

- Single +5 V Power Supply
- Low Power Dissipation
  - Power ON Mode : 20 mW Typ. 53 mW Max.
  - CODEC Power Down Mode : 10 mW Typ. 21 mW Max.
- In compliance with ITU-T's companding law
  - μ-law : MSM6895
  - A-law : MSM6896
- Transmission clocks
  - Continuous CLK : 64, 128, 256 kHz
  - Burst CLK : 192, 384, 768, 1536, 2048 kHz
- Built-in PLL
- Built-in Reference Voltage Supply
- Ringing Tone : Controlled by processor, 9 modes
- Ringing Tone Combination : Controlled by processor, 6 modes
- Information Tone : Controlled by processor, 9 modes
- Built-in PB Tone Generator
- B-Channel Selectable
- General Latch Output for Speech path Control : 4 bits
- Watchdog Timer : 500 ms
- Key Scanning I/O
  - Output : 5 bits
  - Input : 8 bits
- Direct Connection to Handset
- Built-in Preamplifier for Loudspeaker
- Handfree Interface
- Digital and Analog Interface for the phone-conference speech paths
- Package:
  80-pin plastic QFP (QFP80-P-1420-0.80-BK) (Product name : MSM6895GS-BK)
  (Product name : MSM6896GS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC : No connect pin

80-Pin Plastic QFP

PIN DESCRIPTION

Pin	Symbol	Type	Description	Pin	Symbol	Type	Description
1	LB	DO	Data Latch Output B	31	—	—	NC
2	LC	DO	Data Latch Output C	32	VA	—	+5 V Analog Power Supply
3	LD	DO	Data Latch Output D	33	CAI	AI	Analog Signal Input to CODEC
4	SW0	DI	Sounder Tone Select (1)	34	VSGC	AO	Bypass Capacitor for Signal Ground
5	SW1	DI	Sounder Tone Select (2)	35	CAO	AO	Analog Signal Output from CODEC
6	VDG	—	Digital Ground	36	TEST	DI	Control Input for Test
7	VAG	—	Analog Ground	37	CK1536	DI	Clock Input for Test
8	SA0	DO	Sounder Output (+)	38	CK64	DI	Transmission Colck Input
9	SA1	DO	Sounder Output (–)	39	CK8	DI	Frame Synchronous Clock Input
10	—	—	NC	40	$\overline{\text{LOSS}}$	DO	Howler Tone Control Signal
11	RMI	AI	Receive Main Amp Input	41	PO0	DO	Key Scanning Signal Output (0)
12	—	—	NC	42	PO1	DO	Key Scanning Signal Output (1)
13	RMO0	AO	Receive MainAmp Output (+)	43	PO2	DO	Key Scanning Signal Output (2)
14	RMO1	AO	Receive MainAmp Output (–)	44	PO3	DO	Key Scanning Signal Output (3)
15	SPO	AO	Speaker Pre-Amp Output	45	PO4	DO	Key Scanning Signal Output (4)
16	RPO	AO	Receive Pre-Amp Output	46	PI0	DI	Key Scanned Data Input (0)
17	R2I	AI	Receive Addition Signal Input	47	PI1	DI	Key Scanned Data Input (1)
18	R1I	AI	Receive Signal Input	48	PI2	DI	Key Scanned Data Input (2)
19	—	—	NC	49	PI3	DI	Key Scanned Data Input (3)
20	—	—	NC	50	PI4	DI	Key Scanned Data Input (4)
21	TMX2I	AI	Transmit Addtion Signal Input (2)	51	PI5	DI	Key Scanned Data Input (5)
22	MLDY	AI	Hold Tone Input	52	PI6	DI	Key Scanned Data Input (6)
23	TPBI	AI	Transmit Pre-Amp (B) Input	53	PI7	DI	Key Scanned Data Input (7)
24	TMX1I	AI	Transmit Addtion Signal Input (1)	54	INTT	DO	Interrupt Output
25	TPAI	AI	Transmit Pre-Amp (A) Input	55	DB0	I/O	Data Bus (0)
26	VSG	AO	Signal Ground	56	DB1	I/O	Data Bus (1)
27	TPAO	AO	Transmit Pre-Amp (A) Output	57	DB2	I/O	Data Bus (2)
28	T1O	AO	Transmit Signal Output (1)	58	DB3	I/O	Data Bus (3)
29	T2O	AO	Transmit Signal Output (2)	59	DB4	I/O	Data Bus (4)
30	—	—	NC	60	DB5	I/O	Data Bus (5)

PIN DESCRIPTION (Continued)

Pin	Symbol	Type	Description	Pin	Symbol	Type	Description
61	DB6	I/O	Data Bus (6)	71	B1R	DI	B1 Channel Recive Input
62	DB7	I/O	Data Bus (7)	72	B2R	DI	B2 Channel Recive Input
63	AD0	DI	Address Data (0)	73	BT1	DI	B Channel Selector Transmit Data (1)
64	VD	—	+5 V Digital Power Supply	74	BT2	DI	B Channel Selector Transmit Data (2)
65	AD1	DI	Address Data Input (1)	75	BR1	DO	B Channel Selector Receive Data (1)
66	$\overline{WR}$	DI	Write Signal Input	76	BR2	DO	B Channel Selector Receive Data (2)
67	$\overline{RD}$	DI	Read Signal Input	77	$\overline{RESET}$	DI	Reset Input
68	$\overline{CE}$	DI	Chip Enable	78	$\overline{TIME}$	DO	Timer Output
69	B1T	DO	B1 Channel Transmit Output	79	LML	DO	Hold Tone Control Output
70	B2T	DO	B2 Channel Transmit Output	80	LA	DO	Data Latch Output (A)

PIN AND FUNCTIONAL DESCRIPTIONS

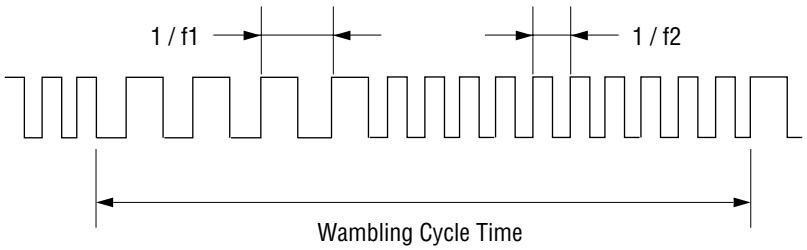
LA, LB, LC, LD

General latch outputs for external control.
Statuses of these outputs are controlled via the processor interface. Refer to the description of the control data for details.

SW0, SW1

External control signal inputs for setting the tone combination of the ringing tone.
When the external control for setting the tone combination is selected, the tone combination is set by these pins.

SW0	SW1		Wambling Cycle	f1	f2
0	0	Tone combination 1	16 Hz	1000 Hz	1333 Hz
0	1	Tone combination 2	16 Hz	800 Hz	1000 Hz
1	0	Tone combination 3	8 Hz	800 Hz	1000 Hz
1	1	Tone combination 1	16 Hz	1000 Hz	1333 Hz



VDG

Digital Ground.

VAG

Analog Ground.

SA0, SA1

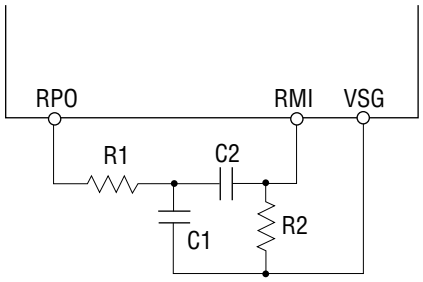
Sounder (ringing tone) driving outputs.
The output signal on SA1 is inverted against the signal on SA0. The sounder circuit can be easily configured by connecting a piezo-sounder between SA0 and SA1. Through processor control, the ringing tone volume is selectable from four levels and one of six tone combinations is selectable. Initially, the ringing tone volume is set at a maximum and the tone combination is set externally. If these pins are used with no-load, tone volume cannot be controlled.
When tone volume control is required, a load resistor must be connected between SA0 and SA1.

RMI, RMO0, RMO1

Receive main amplifier input and outputs.
RMI is the main amplifier input and RMO0 and RMO1 are the main amplifier outputs. The output signal on RMO1 is inverted against RMO0, so the earphone of a piezo electric-type handset is directly connected between RMO0 and RMO1. The RMI input pin is connected to the receive preamplifier output pin (RPO).

If the adjusting of receive path frequency characteristics is required, insert the following circuit for adjustment. During initial setting, the speech path from RMI to RMO0 and RMO1 is disconnected and the output of RMO0 and RMO1 is at the VSG level (VA/2). The speech path is provided by processor control.

A circuit example for adjustment of frequency characteristics



SPO

Output of preamplifier for speaker.
Since the driving capability is 2.4 V_{PP} for the load of 20 kΩ, SPO can not directly drive a speaker. During initial setting, SPO is in a non-signal state (VSG level), and a speech signal, RTONE0, RTONE1, FTONE, hold acknowledge tone, and PB signal acknowledge tone are output through processor control.

R1I, R2I, RPO

Receive preamplifier inputs and output.
R1I and R2I are for the inputs and RPO is for the output of the receive preamplifier. Normally, R1I is connected via an AC-coupling capacitor to the CODEC analog output (CAO), and R2I is used as the mixing signal input pin.
During initial setting, the RPO output is in non-signal state (VSG level), and speech signal, RTONE1, RTONE2, FTONE, PB acknowledge tone, and side tone signal are output through processor control. And if the three-party speech function is required, the R2I pin is connected to the analog output of the other CODEC.

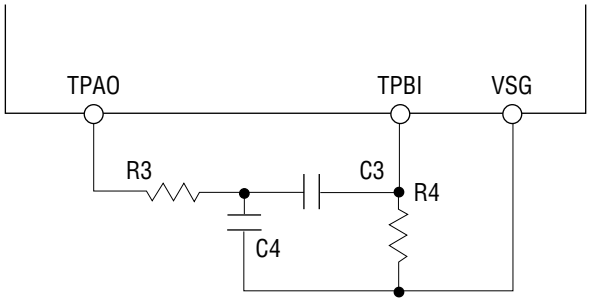
MLDY

Hold tone signal input.
This pin is connected to the output of external melody IC. Through processor control, the signal applied to MLDYI is output from the TO output pin as a hold tone on the transmit path, and from the SPO output pin as a hold acknowledge tone on the receive path.

TPBI

Transmit signal input.
When the handset is used, TPBI is connected to the transmit preamplifier output pin (TPAO). If adjustment of frequency characteristics on the transmit path is required, insert a circuit for adjustment of characteristic between TPAO and TPBI. Through processor control, the signal applied to this pin is output via the T1O and T2O pins on the transmit path output and its side tone via the RPO pin.

A circuit example for adjustment of frequency characteristics



TMX1I, TMX2I

Transmit addition signal inputs.
Through processor control, the input signals to TMX1I and TMX2I are added to the transmit signal and are output to T1O and T2O respectively.

TPAI, TPAO

The transmit preamplifier input and output.
TPAI is the input and TPAO is the output. Connect TPAI to the microphone of handset via an AC-coupling capacitor if the DC offset appears at a transmit signal (offset from SGT). The transmit path from TPAI to TPAO is always established regardless of processor control.

VSG

Signal ground level output.
The output level is equal to a half of the power supply voltage.

VSGC

Bypass capacitor connecting pin for signal ground level.
Insert a 0.1 µF capacitor with good higher frequency characteristic, between VSGC and VAG.

VA, VD

+5 V power supply.
VA is for an analog circuit and VD is for digital supply. Connect both VA and VD to the +5 V analog path of the system.

CAI

CODEC analog output.
Connect CAI to T1O.

CAO

CODEC analog output.
Connect CAO to R1I via an AC-Coupling capacitor.

TEST, CK1536

External master clock inputs.
Since the MSM6895 and MSM6896 contain PLL internally, the external clock signal is eliminated. But the device can operate with the external clock through these pins.
When these pins are not used, leave these pins open or at 0 V.

Mode	TEST pin	CK1536 pin
Internal PLL	0 V	open or 0 V
External master clock	Digital "1"	Input the signal of 1536 kHz

When the external clock is used, the CK1536 signal is required to be synchronized in phase with the CK8 signal.

CK64

CODEC PCM data input and output shift clock input.
When the continuous clock is set, the frequency is one of 64 kHz, 128 kHz, and 256 kHz. When the burst clock is used, one of 192, 384, 768, 1536, and 2048 kHz is available. If the BCLOCK signal is not applied, PLL is out of synchronization and goes into the self-running mode.

CK8

Synchronous signal input.
CODEC PCM data is sent out sequencially from MSB at the rising edge of the CK64 signal in synchronization with the rise of the synchronous signal. PCM data should be entered from MSB in synchronization with the rise of the synchronous signal. PCM data is shifted in at the falling edge of the CK64 signal.

Since the CK8 signal is used for a trigger signal for PLL and for a clock signal to the tone generator, if this signal is not applied, not only any tone can not be output, but also PLL goes out of synchronization and goes into self-running mode. This signal has to be synchronous with the CK64 signal and its frequency must be within 8 kHz ±50 ppm to ensure the CODEC AC characteristics (mainly frequency characteristics).

$\overline{\text{LOSS}}$

Signal output for controlling the external circuits.
When the howler tone of sounder is selected through processor control, the output is in a digital "1".
Initially, this output is set to a digital "0".

PO0, PO1, PO2, PO3, PO4, PO5, PO6, PO7

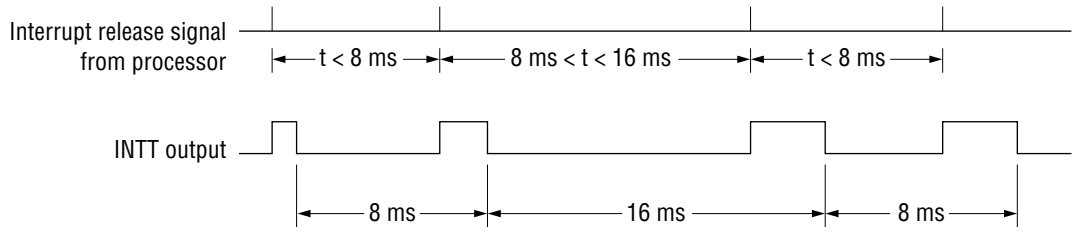
Key scanning outputs.
These output pins need external pull-up resistors because of their open- drain circuits. Through processor control, these outputs can be set open or to digital "0". Initially, these outputs are set at an opened state.

PI0, PI1, PI2, PI3, PI4, PI5, PI6, PI7

Key scanning inputs.
In the READ mode, data on PI0 to PI7 can be read out of the processor via data bus (DB0 to DB7).

INTT

Interrupt signal output to the processor.
INTT outputs interrupt signals (digital "0") at intervals of 8 ms by the interrupt release control signal from the processor. INTT does not output any signal while no CK8 signal is input.



DB0, DB1, DB2, DB3, DB4, DB5, DB6, DB7

Data bus inputs and outputs.

AD0, AD1

Address data inputs for the internal control registers.
Addressing of the internal control registers is executed by AD0 and AD1 and sub address data, DB7 and DB6.

	AD1	AD0	DB7	DB6	Function
Write	0	0	0	0	Sounder Control
	0	0	0	1	Control of function key acknowledge tone
	0	0	1	0	PB tone control
	0	0	1	1	Control of the internal control latch and the general-purpose latch, Reset control of the watch dog timer.
	0	1	—	—	Control of channel selector
	1	0	—	—	Key scanning output control, interrupt release control
	1	1	0	0	Volume control and tone combination control of sounder
	1	1	0	1	CODEC power down control
	1	1	1	0	Level control of transmit path, PB tone, and Hold tone, Gain control of receive path
	1	1	1	1	Frequency control of howler tone
Read	1	0	—	—	Read of the key scanning data

$\overline{WR}$

Write signal for internal control registers.
Data on the data bus is written into the registers at the rising edge of $\overline{WR}$ under the condition of digital "0" of $\overline{CE}$ (Chip Enable). While $\overline{CE}$ is in digital "1" state, $\overline{WR}$ becomes invalid. The Write cycle is a minimum of 2 µs, but if the CK64 and CK8 signals are silent, the write cycle requires a minimum of 50 µs.
A minimum of 2 µs specified as the write cycle is valid 10 ms after CK64 and CK8 signals are input.

$\overline{RD}$

Read signal input to read PI0 to PI7 out of the processor.
When $\overline{CE}$ and $\overline{RD}$ are in digital "0" state, the digital values on PI0 to PI7 are output onto the data buses DB0 to DB7. While $\overline{CE}$ is in digital "1" state, the $\overline{RD}$ signal becomes invalid.

$\overline{CE}$

Chip Enable signal input.
When $\overline{CE}$ is in digital "0" state, $\overline{WR}$ and $\overline{RD}$ are valid.

B1T, B2T, B1R, B2R

B channel interface inputs and outputs.
B1T and B2T are outputs, and B1R and B2R are inputs. Through channel control by the processor, various data paths are set. The CODEC input and output signals are input and output via these pins.
Initially the B1T and B2T outputs are fixed in a digital "1", and the B1R and B2R inputs are neglected.

BR1, BR2, BT1, BT2

External digital inputs and outputs to the B-channel.
BR1 and BR2 are outputs, and BT1 and BT2 are inputs. Through channel control by processor, the digital paths are set between these input and output pins and the B channel.
These signals are applied to another CODEC interface of three-party the speech path and to the interface of 64 kbps at the rate adaptor circuit.
Initially the BR1 and BR2 outputs are fixed in a digital "1", and the BT1 and BT2 inputs are neglected.

$\overline{RESET}$

Reset signal input.
Digital "0" input to $\overline{RESET}$ makes all of internal control registers to be initialized. When powered on, this $\overline{RESET}$ signal should be input for initializing the system.

$\overline{TIME}$

Watchdog timer output.
When the processor does not reset the timer, the 500 ms period (Digital "0" : 4 ms) digital signal is continuously output. When $\overline{RESET}$ is at digital "0", this timer is reset. And, in about 500 ms after $\overline{RESET}$ goes to digital "1", the first timer output signal is issued and then the timer signal is output at intervals of a 500 ms. If the CK8 signal is not input, the $\overline{TIME}$ signal is not output.

LML

Control signal output for external hold tone generator.
LML goes to digital "1" state when the hold tone transmit mode on transmit path or the hold acknowledge tone mode on receive path is selected. During initialized state, LML is in digital "0" state.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	VAG, VDG = 0 V	0 to 7	V
Analog Input Voltage	V_{AIN}	VAG, VDG = 0 V	–0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	VAG, VDG = 0 V	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_D	VA, VD (Voltage must be fixed)	4.75	5.0	5.25	V
Operating Temperature	Ta	—	–10	+25	+70	°C
Input High Voltage	V_{IH}	All Digital Input Pins	2.2	—	V_{DD}	V
Input Low Voltage	V_{IL}	All Digital Input Pins	0	—	0.8	V
Digital Input Rise Time	t_{Ir}	All Digital Input Pins	—	—	50	ns
Digital Input Fall Time	t_{If}	All Digital Input Pins	—	—	50	ns
Digital Output Load	R_{DL}	PO0 to PO4 Output	10	—	—	kΩ
	C_{DL}		—	—	100	pF

Recommended Operating Conditions (CODEC Digital Interface)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock Frequency	F_C	CK64	—	64 128 256	—	kHz
Sync Pulse Frequency	F_S	CK8	—	8.0	—	kHz
Clock Duty Ratio	D_C	CK64	40	50	60	%
Sync Pulse Setting Time	t_{XS}	CK64→CK8 See Fig.1	—	—	100	ns
	t_{SX}	CK8→CK64 See Fig.1	—	—	100	ns
Sync Pulse Width	t_{WS}	—	1 CK64	—	100	µs
Data Setup Time	t_{DS}	B1R, B2R	100	—	—	ns
Data Hold Time	t_{DH}	B1R, B2R	100	—	—	ns
Allowable Jitter Width	—	CK8	—	—	500	ns

Recommended Operating Conditions (Processor Digital Interface)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Write Pulse Period	P_W	$\overline{WR}$	See Fig.2	2000	—	—	ns
Write Pulse Width	T_W	$\overline{WR}$		100	—	—	ns
Read Pulse Width	T_R	$\overline{RD}$		200	—	—	ns
Address Data Setup Time	t_{AW1}	AD0, AD1→$\overline{WR}$		10	—	—	ns
	t_{AR1}	AD0, AD1→$\overline{RD}$		80	—	—	ns
Address Data Hold Time	t_{AW2}	$\overline{WR}$→AD0, AD1		50	—	—	ns
	t_{AR2}	$\overline{RD}$→AD0, AD1		10	—	—	ns
$\overline{CE}$ Setup Time	t_{CW1}	$\overline{CE}$→$\overline{WR}$		10	—	—	ns
	t_{CR1}	$\overline{CE}$→$\overline{RD}$		80	—	—	ns
$\overline{CE}$ Hold Time	t_{CW2}	$\overline{WR}$→$\overline{CE}$		50	—	—	ns
	t_{CR2}	$\overline{RD}$→$\overline{CE}$		10	—	—	ns
Data Setup Time	t_{DW1}	DB0 to 7→$\overline{WR}$		110	—	—	ns
Data Hold Time	t_{DW2}	$\overline{WR}$→DB0 to 7		20	—	—	ns
Reset Pulse Width	t_{WRES}	$\overline{RESET}$		100	—	—	ns

Recommend Operating Conditions (Analog Interface)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog Input Voltage	V_{AIN}	TPAI	—	—	0.24	V_{PP}
		TPBI	—	—	0.31	
		TMX1I, TMX2I (Transmit Gain: Typ.)	—	—	2.40	
		MLDYI (Transmit Gain: Typ.)	—	—	1.90	
		R1I, R2I (Transmit Gain: Typ.)	—	—	1.20	
		RMI	—	—	0.51	
		CAI	—	—	2.40	
Analog Load Resistance	R_{AL}	TPAO, T1O, T2O, RPO, SPO, CAO	20	—	—	kΩ
		RMO0, RMO1	3	—	—	
Analog Load Capacitance	C_{AL}	TPAO, T1O, T2O, RPO, SPO, CAO	—	—	100	pF
		RMO0, RMO1	—	—	55	nF
Allowable Analog Input Offset Voltage	V_{off}	TPAI, TPBI, RMI	–10	—	+10	mV
		MLDYI, TMX1I, TMX2I	–50	—	+50	
		R1I, R2I	–25	—	+25	
		CAI	–100	—	+100	

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(V_{DD} = 5 V ±5%, Ta = –10°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating Mode (No Signal, Sounder OFF)	—	3.9	10.0	mA
	I_{DD2}	CODEC Receive Power Down	—	3.3	8.0	mA
	I_{DD3}	CODEC Transmit Power Down	—	2.8	7.0	mA
	I_{DD4}	CODEC Transmit/Receive Power Down	—	2.2	4.0	mA
Input High Voltage	V_{IH}	—	2.2	—	V_{DD}	V
Input Low Voltage	V_{IL}	—	0.0	—	0.8	V
High Input Leakage Current	I_{IH}	—	—	—	2.0	µA
Low Input Leakage Current	I_{IL}	—	—	—	0.5	µA
Digital Output High Voltage	V_{OH}	I_{OH} = 0.4 mA	2.4	—	V_{DD}	V
		I_{OH} = 1 µA	3.8	—	V_{DD}	
Digital Output Low Voltage	V_{OL}	I_{OL} = –1.6 mA	0.0	—	0.4	V
Digital Output Leakage Current	I_O	—	—	—	10	µA
Analog Output Offset Voltage	V_{off}	TPAO, T1O, T2O, CAO, RPO, RMO1, RMO2, SPO	–100	—	+100	mV
Input Capacitance	C_{IN}	—	—	5	—	pF
Analog Input Resistance	R_{IN}	TPAI, TPBI, MLDYI, RMI	—	10	—	MΩ
		TMX1I, TMX2I, R1I, R2I	10	—	—	kΩ
		CAI (fin : < 4 kHz)	—	1	—	MΩ
VSG Voltage	—	—	VA/2 –0.05	VA/2	VA/2 +0.05	V
VSG Drive Current	I_{SGF}	FORCE Current	1.0	1.5	—	mA
	I_{SGS}	SINK Current	0.3	0.5	—	

AC Characteristics 1 (CODEC)

(V_{DD} = 5 V ±5%, Ta = –10°C to +70°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Transmit Frequency Response	Loss T1	60	0		20	27	—	dB
	Loss T2	300			–0.15	+0.07	+0.20	
	Loss T3	1020			Reference			
	Loss T4	2020			–0.15	–0.03	+0.20	
	Loss T5	3000			–0.15	+0.06	+0.20	
	Loss T6	3400			0.0	0.38	0.80	
Receive Frequency Response	Loss R1	300	0		–0.15	–0.03	+0.20	dB
	Loss R2	1020			Reference			
	Loss R3	2020			–0.15	–0.02	+0.20	
	Loss R4	3000			–0.15	+0.15	+0.20	
	Loss R5	3400			0.0	0.56	0.80	
Transmit Signal to Distortion Ratio	SD T1	1020	3	*1	35	43.0	—	dB
	SD T2		0		35	41.0	—	
	SD T3		–30		35	38.0	—	
	SD T4		–40	*2	29	31.0	—	
					28			
	SD T5		–45	*2	24	26.5	—	
					23			
Receive Signal to Distortion Ratio	SD R1	1020	3	*1	37	43.0	—	dB
	SD R2		0		37	41.0	—	
	SD R3		–30		37	40.0	—	
	SD R4		–40	*2	31	34.0	—	
					30			
	SD R5		–45	*2	26	31.0	—	
					25			
Transmit Gain Tracking	GT T1	1020	3		–0.3	+0.01	+0.3	dB
	GT T2		–10		Reference			
	GT T3		–40		–0.3	+0.13	+0.3	
	GT T4		–50		–0.6	+0.32	+0.6	
	GT T5		–55		–1.5	+0.64	+1.5	
Receive Gain Tracking	GT R1	1020	3		–0.2	0.0	+0.2	dB
	GT R2		–10		Reference			
	GT R3		–40		–0.2	–0.06	+0.2	
	GT R4		–50		–0.4	–0.20	+0.4	
	GT R5		–55		–0.8	–0.27	+0.8	

Notes: *1 Psophometric filter is used
*2 Upper is specified for the MSM6895, lower for the MSM6896

AC Characteristics 1 (CODEC) (Continued)

(V_{DD} = 5 V ±5%, Ta = –10°C to +70°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition		Min.	Typ.	Max.	Unit
Idle Channel Noise	Nidle T	—	—	AIN = SG *1	*2	—	–73.5 –71	–70 –69	dBm0p
	Nidle R	—	—	*1 *3		—	–77.8	–74	
Absolute Amplitude	AV T	1020	0	Transmit CODEC		0.5671	0.6007	0.6363	Vrms
	AV R			Receive CODEC		0.5671	0.6007	0.6363	
Absolute Delay Time	Td	1020	0	A to A CK64 = 64 kHz		—	0.58	0.60	ms
Transmit Group Delay	tgd T1	500	0	*4		—	0.19	0.75	ms
	tgd T2	600				—	0.12	0.35	
	tgd T3	1000				—	0.02	0.125	
	tgd T4	2600				—	0.05	0.125	
	tgd T5	2800				—	0.08	0.75	
Receive Group Delay	tgd R1	500	0	*4		—	0.0	0.75	ms
	tgd R2	600				—	0.0	0.35	
	tgd R3	1000				—	0.0	0.125	
	tgd R4	2600				—	0.09	0.125	
	tgd R5	2800				—	0.12	0.75	
Crosstalk Attenuation	CR T	1020	0	Transmit → Receive		66	86	—	dB
	CR R			Receive → Transmit		70	78	—	
Discrimination	DIS	4.6 kHz to 72 kHz	–25	0 to 4000 Hz		30	32.0	—	dB
Out-of-band Signal Spurious	S	300 to 3400	0	4.6 kHz to 100 kHz		—	–37.5	–35	dBm0
Intermodulation Distortion	IMD	fa = 470 fb = 320	–4	2fa–fb		—	–52	–35	dBm0
Power Supply Noise Rejection Ratio	PSR T	0 to 50 kHz	100 mV_{pp}	*5		—	30	—	dB
	PSR R								

Notes: *1 Psophometric filter is used
*2 Upper is specified for the MSM6895, lower for the MSM6896
*3 PCM data for MSM6895: All "1"
PCM data for MSM6896: "11010101"
*4 Minimum value of the group delay distortion
*5 The measurement under idle channel noise

AC Characteristics 2 (Transmit Path)

(V_{DD} = 5 V ±5%, Ta = –10°C to +70°C)

Parameter	Symbol	Freq. (Hz)	Level (dBV)	Condition	Min.	Typ.	Max.	Unit
Pre-Amp Gain	GTPA	1020	–24.4	TPAI-TPAO	18.0	20.0	22.0	dB
Transmit Path 1 Gain	GTPB1	1020	–22.1	TPBI-T1O	15.7	17.7	19.7	dB
Transmit Path 2 Gain	GTPB2			TPBI-T2O	15.7	17.7	19.7	dB
Transmit Addition Signal 1 Gain	GTMX1	1020	–4.4	TMX1I-T1O	–2.0	0.0	+2.0	dB
Transmit Addition Signal 2 Gain	GTMX2			TMX1I-T2O	–2.0	0.0	+2.0	dB
In-Channel PB Signal Output Level	VPBT1	—	—	T1O Set at typical gain	–17.4	–15.4	–13.4	dBV
	VPBT2	—	—	T2O Set at typical gain	–17.4	–15.4	–13.4	dBV
In-Channel PB Signal Output Level Setting	GPBT1	—	—	For typical setting – 3 dB	–5.0	–3.0	–1.0	dB
	GPBT2			– 6 dB	–8.0	–6.0	–4.0	dB
In-Channel PB Signal Frequency Deviation	DfPBT	—	—	T1O, T2O	–0.9	—	+0.9	%
In-Channel PB Signal Distortion	THDPBT	—	—	In-Band Distortion	—	–35	–30	dB
Hold Tone Path Gain	GPAT1	1020	–22.4	MLDYI-T1O Set at typical gain	–4.0	–2.0	0.0	dB
	GPAT2			MLDYI-T2O	–4.0	–2.0	0.0	
Hold Tone Path Gain Setting	RG1 PAT	1020	–22.4	For typical setting –3 dB	–5.0	–3.0	–1.0	dB
	RG2 PAT			–6 dB	–8.0	–6.0	–4.0	dB
Idle Channel Noise	Ni TPA	—	—	TPAI: 510 Ω at termination Meature at TPAO *6	—	–93	—	dBV
	Ni TPB	—	—	T1O, T2O *6	—	–91	—	dBV
Maximum Output Voltage Swing	VOT	—	—	TPAO, T1O, T2O, R_L = 20 kΩ	2.4	—	—	V_{PP}

Note: *6 Noise band width: 0.3 kHz to 3.4 kHz, non-weighted

AC Characteristics 3 (Receive Path)

(V_{DD} = 5 V ±5%, Ta = −10°C to +70°C)

Parameter	Symbol	Freq. (Hz)	Level (dBV)	Condition		Min.	Typ.	Max.	Unit
Receive Main Amp. Gain	GRMO0	1020	−19.4	RMI-RMO0		13.2	15.3	17.3	dB
	GRMO1		−19.4	RMI-RMO1		13.2	15.3	17.3	dB
Receive Main Amp. Output Gain Difference	DGRMO	1020	−19.4	RMO0/RMO1		—	−0.01	—	dB
Receive Main Amp. Output Phase Difference	DPRMO	1020	−19.4	RMO0/RMO1		—	−179.6	—	deg
Receive Signal Path Gain	GRPA	1020	−14.4	R1I-RPO	Set at typical	−8.0	−6.0	−4.0	dB
Receive Signal Path Gain Setting	RG RPA1	1020	−23.4	For typical setting	+3 dB	1.0	3.0	5.0	dB
	RG RPA2				+6 dB	4.0	6.0	8.0	
	RG RPA3				+9 dB	7.0	9.0	11.0	
Receive Addition Signal Path Gain	GRPB	1020	−14.4	R2I-RPO	Set at typical	−8.0	−6.0	−4.0	dB
Receive Addition Signal Path Gain Setting	RG RPB1	1020	−14.4	For typical setting	+3 dB	1.0	3.0	5.0	dB
	RG RPB2				+6 dB	4.0	6.0	8.0	
	RG RPB3				+9 dB	7.0	9.0	11.0	
Speaker Preamp. Gain	GSP	1020	−4.4	R1I-SPO	Set at typical	−8.0	−6.0	−4.0	dB
				R2I-SPO	Set at typical	−8.0	−6.0	−4.0	
Hold Acknowledge Tone Path Gain	GPAS	1020	−7.4	MLDYI-SPO		−5.0	−3.0	−1.0	dB
PB Acknowledge Tone Output Level	VPBRP	—	—	RPO		−32.1	−30.1	−28.1	dBV
	VPBRP			SPO		−30.2	−28.2	−26.2	dBV
PB Acknowledge Tone Frequency Difference	DfPBR	—	—	RPO, SPO		−0.9	—	+0.9	%
PB Acknowledge Tone Distortion	THD PBR	—	—	RPO, SPO		—	−35	−30	dB
Side Tone Path Gain	GSIDE	1020	−21.4	TPBI-RPO		8.9	10.9	12.9	dB
Idle Channel Noise	Ni RPO	—	—	RPO	*6	—	−86	—	dBV
	Ni SPO	—	—	SPO	*6	—	−86	—	dBV
	Ni RMO	—	—	RMI, VSG RM00, RM01	*6	—	−95	—	dBV

Note: *6 Noise band width: 0.3 kHz to 3.4 kHz, non-weighted

AC Characteristics 3 (Receive Path) (Continued)

(V_{DD} = 5 V ±5%, Ta = –10°C to +70°C)

Parameter	Symbol	Freq. (Hz)	Level (dBV)	Condition	Min.	Typ.	Max.	Unit
Maximum Output Amplitude	VOR	—	—	RPO, SPO R_L = 20 kΩ	2.4	—	—	V_{PP}
	VOM	—	—	RMO0, RMO1 R_L = 3 kΩ +55 nF	3.0	—	—	V_{PP}
RTONE0 Output Amplitude *7	VRT0	—	—	RPO	77.2	91.7	109.0	mV_{PP}
RTONE1 Output Amplitude *8	VRT1	—	—	RPO	132.0	157.0	187.0	mV_{PP}
FTONE Output Amplitude	VFTRP	—	—	RPO	135.5	161.0	191.5	mV_{PP}
	VFTSP			SPO	159.0	189.0	224.6	

Notes: *7 DT, PDT, SDT, CRBT, IIT
*8 RBT, DT, T250

AC Characteristics 4 (Ringing Tone Output Circuit)

(V_{DD} = 5 V ±5%, Ta = –10°C to +70°C)

Parameter	Symbol	Freq. (Hz)	Level (dBV)	Condition		Min.	Typ.	Max.	Unit
Calling Tone Output Amplitude *9	VST1	—	—	SA0-SA1 730 Ω to VDG	Volume 1	3.25	4.0	—	V_{PP}
	VST2				Volume 2	0.73	1.28	1.98	
	VST3				Volume 3	0.25	0.47	0.65	
	VST4				Volume 4	0.13	0.28	0.45	
Howler Tone Output Amplitude	VHOW	—	—	VDG		3.25	4.0	—	V_{PP}

Note: *9. IR-1, IR-2, SIR-1, SIR-2, CR, T1K, HR, SPT

Digital Interface Characteristics

(V_{DD} = 5 V ±5%, Ta = –10°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital Output (Latch) Delay Time	t_{PDLA}	$\overline{WR}$→LA, LB, LC, LD, LML, $\overline{LOSS}$	0.5	—	1.9	µs
key Scanning Output Delay Time	t_{PDSCN}	$\overline{WR}$→PO0, PO1, PO2, PO3, PO4 Pull-up resistor : 10 kΩ	0.5	—	1.9	µs
Digital Output (Data) Delay Time	t_{PDDATA}	$\overline{RD}$→DB0 to DB7	20	52	150	ns
Digital Path Delay Time	t_{PDPATH}	BT1→BR1, BR2 BT2→BR1, BR2	20	52	150	ns
CODEC Data Output Delay Time	t_{PDCOD}	CK64→B1T, B2T	20	50	100	ns

TIMING DIAGRAM

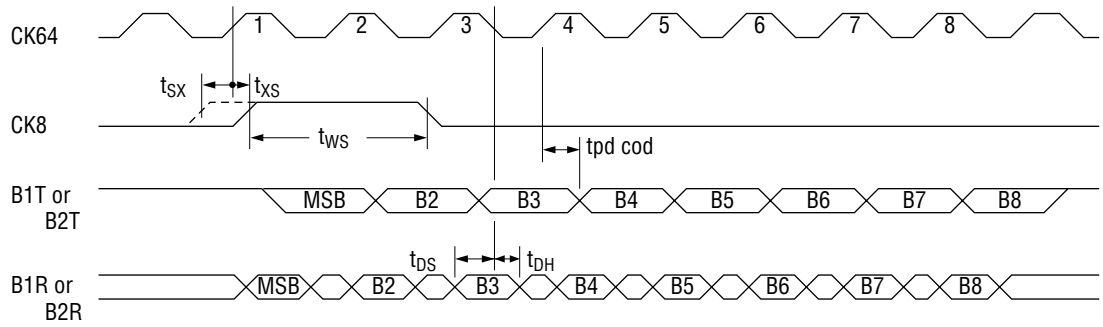


Figure 1 CODEC Timing

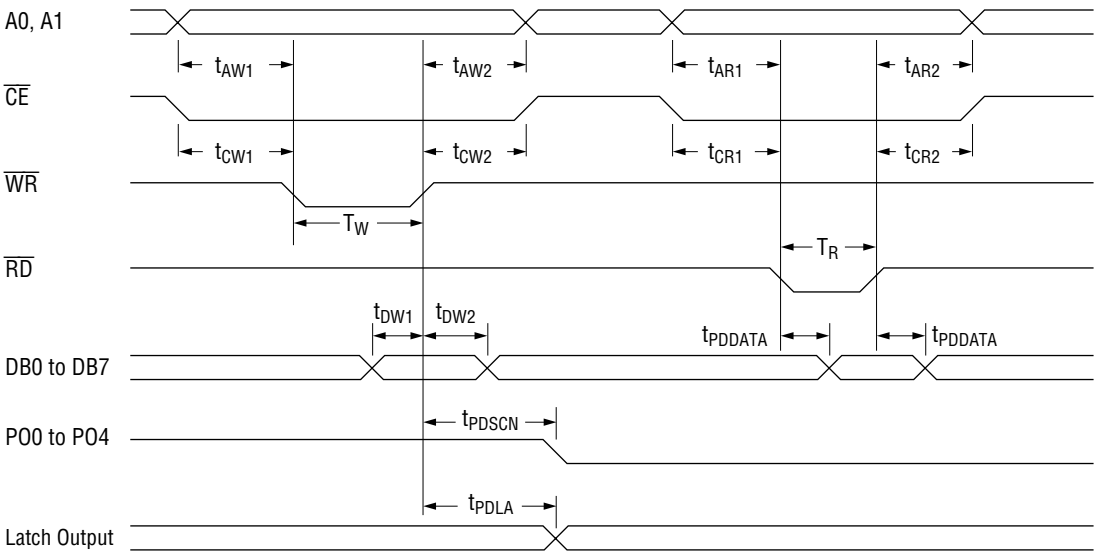


Figure 2 Processor Interface Timing

FUNCTIONAL DESCRIPTION

Control Data Description

Sounder control

WRITE Mode

Address Data AD1 = 0, AD0 = 0

Control Data								Output Tone	Frequency (Hz)	Make/Break Timing *6			Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			Make (Sec)	Break1 (Sec)	Break2 (Sec)	
0	0	1	PDC	0	0	0	0	SPT	1	0.125	0.125	∞	Tone Output:
			*1	0	0	0	1	IR-1	Wamble Tone	1	2	—	SA0, SA1
				0	0	1	0	IR-2	Wamble Tone	0.5	0.5	—	
				0	0	1	1	SIR-1	Wamble Tone	0.25	0.25	2.25	
				0	1	0	0	CR	Wamble Tone	Continuous			
				0	1	0	1	HOW *2	800 or Wamble Tone	Continuous			
				0	1	1	0	SIR-2	Wamble Tone	0.5	1	—	
				0	1	1	1	T1K	1	0.25	0.25	—	
				1	0	0	0	HR	1	0.125	0.125	—	
				1	0	0	0	DT	400	Continuous			
				1	0	1	0	SDT	400	0.125	0.125	—	Tone Output:
				1	0	1	1	RBT	400/16	1	2	—	RPO, Refer to Table 2 and 4.
				1	1	0	0	BT	400	0.5	0.5	—	
				1	1	0	1	PDT	400	0.25	0.25	—	
				1	1	1	0	CRBT	400/16	0.5	∞	—	
		0		X	X	X	X	Suspends the tones above.					

*1. PDC: This bit is used for the CODEC power-down control. For making this bit valid, "0"s must be written to the control data bits described in the later section.
PDC = 1: CODEC is in power-down mode. PDC = 0: CODEC is in operation mode.

*2. When the HOW is indicated, the $\overline{\text{LOSS}}$ output is "1". Otherwise it is "0".

*3. In the above specification, the data contents written later are valid. The signal of sounder path (SA0, SA1) and the signal of receive path (RPO) can not be output simultaneously.

Control of function key acknowledge tone

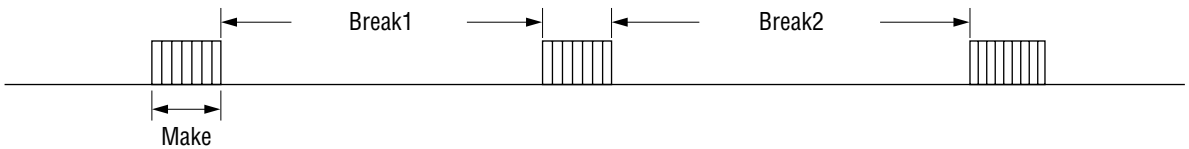
WRITE Mode
Address Data AD1 = 0, AD0 = 0

Control Data								Output Tone	Frequency (Hz)	Make/Break Timing *6			Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			Make (Sec)	Break1 (Sec)	Break2 (Sec)	
0	1	1	X	X	0	0	1	IIT	400	0.25	0.25	2.25	Tone output:
			X	X	0	1	0	T250	250	Continuous			RPO, SPO
			NTTC	X	0	1	1	FTONE (1)	1 k	Continuous			
			*4	X	1	0	0	FTONE (2)	1 k	0.1	∞	—	
		0	0	0	0	0	0	Suspends the all above tones					
		0	0	0	0	0	1	Suspends the IIT tone					
					0	1	0	Suspends the T250 tone					
					0	1	1	Suspends the FTONE					

*4. NTTC = 1 when the initial state is set. NTTC can be set as PBTC when the PB tone is set, but the data written into NTTC in later is valid. When NTTC = 1, the FTONE (1) and FTONE (2) signals are output from SPO. When NTTC = 0, these signals are output from RPO. NTTC = 1 when FTONE and PB tone is stopped.

*5. When two or more signals are specified out of IIT, T250 and FTONE, the output signals are compounded by two or three tones.

*6. The definition of Make/Break Timing is as follows;



PB tone control

WRITE Mode
Address Data AD1 = 0, AD0 = 0

Control Data								Output PB Frequency			Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	PB	Low	High	
1	0	1	PBTC	0	0	0	0	1	697 Hz	1209 Hz	When PBTC = 0, the PB tone is output from the transmit path and the receive path RPO. The conditions of internal control signals are MUTN = 0 and NTTC = 0.
				0	0	0	1	2	697 Hz	1336 Hz	
				0	0	1	0	3	697 Hz	1477 Hz	
				0	0	1	1	A	697 Hz	1633 Hz	
				0	1	0	0	4	770 Hz	1209 Hz	When PBTC = 1, the PB tone is output only from the receive path SPO. The PB signal is not output from the transmit path. The conditions of internal control signals are MUTN = 1 and NTTC = 1.
				0	1	0	1	5	770 Hz	1336 Hz	
				0	1	1	0	6	770 Hz	1477 Hz	
				0	1	1	1	B	770 Hz	1633 Hz	
				1	0	0	0	7	852 Hz	1209 Hz	
				1	0	0	1	8	852 Hz	1336 Hz	When the initial state is set and the PB tone is suspended, the conditions of internal control signals are MUTN = 1 and NTTC = 1.
				1	0	1	0	9	852 Hz	1477 Hz	
				1	0	1	1	C	852 Hz	1633 Hz	
				1	1	0	0	*	941 Hz	1209 Hz	
				1	1	0	1	0	941 Hz	1336 Hz	
				1	1	1	0	#	941 Hz	1477 Hz	
				1	1	1	1	D	941 Hz	1633 Hz	
		0	0	X	X	X	X	Suspends the PB tone			

Latch control and timer reset

WRITE Mode
Address Data AD1 = 0, AD0 = 0

Control data								Latch output	Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	1	1	0	0	0	0	1	LT1 = 1	These latch are for internal control and used for control of speech path.
				0	0	1	0	LML1 = 1	Initially all latch are set to "0". For details of speech path control, refer to Table 1 to 4.
				0	0	1	1	LMX1 = 1	Each latch can be specified independently.
				0	1	0	1	LT2 = 1	
				0	1	1	0	LML2 = 1	The output at the LML pin is in "1" when either LML1, LML2, or LMR is in "1".
				0	1	1	1	LMX2 = 1	
				1	0	0	0	LR = 1	
				1	0	0	1	LS = 1	
				1	0	1	0	LMN = 1	
				1	0	1	1	LMR = 1	
				1	1	0	0	LA = 1	These general latches are for external control. LA, LB, LC, and LD correspond to
				1	1	0	1	LB = 1	the external pin symbols and are set independently. Initially, all latches are set to "0".
				1	1	1	0	LC = 1	
				1	1	1	1	LD = 1	
		0	0	Latch codes described above				Sets the corresponding latches listed above to "0".	
		0	0	0	0	0	0	Sets all latches listed above to "0".	
1	1	1	1	0	0	0	0	Resets the watch dog timer.	

Table 1. Transmit speech path setting list

Status Symbol	Control Symbol								Output Signal at T1O					Output Signal at T2O				
	LML1	LT1	LMX1	LML2	LT2	LMX2	LMN	MUTN	SG	T	TMX1	PBt	Ht	SG	T	TMX2	PBt	Ht
TA-1	0	0	X	—	—	—	X	X	1	—	—	—	—	—	—	—	—	—
TA-2	0	1	0	—	—	—	0	1	—	1	—	—	—	—	—	—	—	—
TA-3	0	1	0	—	—	—	1	1	1	—	—	—	—	—	—	—	—	—
TA-4	0	1	1	—	—	—	0	1	—	1	1	—	—	—	—	—	—	—
TA-5	0	1	1	—	—	—	1	1	—	—	1	—	—	—	—	—	—	—
TA-6	0	1	X	—	—	—	X	0	—	—	—	1	—	—	—	—	—	—
TA-7	1	X	X	—	—	—	X	X	—	—	—	—	1	—	—	—	—	—
TB-1	—	—	—	0	0	X	X	X	—	—	—	—	—	1	—	—	—	—
TB-2	—	—	—	0	1	0	0	1	—	—	—	—	—	—	1	—	—	—
TB-3	—	—	—	0	1	0	1	1	—	—	—	—	—	1	—	—	—	—
TB-4	—	—	—	0	1	1	0	1	—	—	—	—	—	—	1	1	—	—
TB-5	—	—	—	0	1	1	1	1	—	—	—	—	—	—	—	1	—	—
TB-6	—	—	—	0	1	X	X	0	—	—	—	—	—	—	—	—	1	—
TB-7	—	—	—	1	X	X	X	X	—	—	—	—	—	—	—	—	—	1

Notes:
1. MUTN of Control Signal is set by PBTC (DB4).
   MUTN = 1 when the initial state is set. MUTN = 0 when PBTC = 0. MUTN = 1 when PBTC= 1.
2. SG: Signal ground, T: Transmit signal, TMX1: Transmit addition signal 1, TMX2: Transmit addition signal 2, PBt: PB signal, Ht: Hold tone signal
3. The output signals of T1O and T2O are the signals added by the signals indicated in "1"s in each column.

Table 2. Receive speech path setting list (RPO output)

Status Symbol	Control Signal						Output Signal at RPO						
	LS	LT1	LT2	LMN	MUTN	NTTC	R1	R2	Ts	RT0	RT1	FT	PBr
RP-1	0	0	0	X	X	0/1	—	—	—	1	1	1/0	1/0
RP-2	0	1	0	0	1	0/1	1	—	1	1	1	1/0	1/0
RP-3	0	1	0	0	0	0/1	1	—	—	1	1	1/0	1/0
RP-4	0	1	0	1	X	0/1	1	—	—	1	1	1/0	1/0
RP-5	0	0	1	0	1	0/1	—	1	1	1	1	1/0	1/0
RP-6	0	0	1	0	0	0/1	—	1	—	1	1	1/0	1/0
RP-7	0	0	1	1	X	0/1	—	1	—	1	1	1/0	1/0
RP-8	0	1	1	0	1	0/1	1	1	1	1	1	1/0	1/0
RP-9	0	1	1	0	0	0/1	1	1	—	1	1	1/0	1/0
RP-10	0	1	1	1	X	0/1	1	1	—	1	1	1/0	1/0
RP-11	1	0	0	X	X	X	—	—	—	1	1	—	—
RP-12	1	1	0	X	X	X	1	—	—	1	1	—	—
RP-13	1	0	1	X	X	X	—	1	—	1	1	—	—
RP-14	1	1	1	X	X	X	1	1	—	1	1	—	—

Table 3. Control of receive main amplifier

Control Signal	Output signal of
LR	RMO0 and RMO1
0	SG
1	Input signal to RMI

Notes:
4. R1: Receive signal 1, R2: Receive signal 2, Ts: Side tone signal, RT0: DT, PDT, SDT, CRBT, and IIT, RT1: RBT, BT, and T250, FT: FTONE and PBr: PB acknowledge signal.
5. Output Signal RPO is the signal added by the signal indicated in "1"s in each column.
6. "0"s of Control Signal NTTC are equivalent to "1"s of the Output Signals FT and PBr, and "1"s are equivalent to "0"s of Output Signals.
7. Control Signals MUTN and NTTC are the internal control signals. Initially, both signals are in "1"s. MUTN is controlled by PBTC of controlling the PB tone.
   MUTN = 0 when PBTC = 0. MUTN = 1 when PBTC = 1.
   NTTC is controlled by PBTC of controlling the PB tone or NTTC of controlling the function key acknowledge tone, but the NTTC data written later is valid.
   NTTC = 0 when PBTC = 0. NTTC = 1 when PBTC = 1.

Table 4. Receive speech path setting list (SPO)

Status Symbol	Control Signal					Output Signal at SPO							
	LS	LMR	LT1	LT2	NTTC	SG	R1	R2	RT0	RT1	FT	PBr	Hr
RS-1	0	0	X	X	0	1	—	—	—	—	—	—	—
RS-2	0	0	X	X	1	—	—	—	—	—	1	1	—
RS-3	0	1	X	X	0/1	—	—	—	—	—	0/1	0/1	1
RS-4	1	0	0	0	X	—	—	—	1	1	1	1	—
RS-5	1	0	1	0	X	—	1	—	1	1	1	1	—
RS-6	1	0	0	1	X	—	—	1	1	1	1	1	—
RS-7	1	0	1	1	X	—	1	1	1	1	1	1	—
RS-8	1	1	0	0	X	—	—	—	1	1	1	1	1
RS-9	1	1	1	0	X	—	1	—	1	1	1	1	1
RS-10	1	1	0	1	X	—	—	1	1	1	1	1	1
RS-11	1	1	1	1	X	—	1	1	1	1	1	1	1

Notes:
8. SG: Signal ground, R1: Receive signal 1, R2: Receive signal 2, Hr: Hold acknowledge tone, PBr: PB acknowledge tone, FT: FTONE, RT0: DT, PDT, SDT, CRBT, and IIT and RT1: RBT, BT, and T250.
9. An Output Signal at SPO is the signal added by the signal indicated in "1"s in each column.
10. The Control Signal NTTC is defined equally to Notes : 7.

Channel selector control

WRITE Mode
Address Data AD1 = 0, AD0 = 1

Control Data								Status Symbol	Main Connection Status		Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0				
0	0	0	0	0	0	0	0	A1	B1T←"1"	B1R→No connection	Different groups (A, B, C, and D) are set
					0	0	1	A2	B1T←DOUT	B1R→DIN	independently.
					0	1	0	A3	B1T←BT1	B1R→BR1	
					0	1	1	A4	B1T←BT2	B1R→BR2	For setting the same group, the data written later is
					1	0	0	B1	B2T←"1"	B2R→No connection	valid.
					1	0	1	B2	B2T←DOUT	B2R→DIN	
					1	1	0	B3	B2T←BT1	B2R→BR1	Refer to Table 5 and 6 for details.
					1	1	1	B4	B2T←BT2	B2R→BR2	The initial statuses are A1 and B2.
				1	X	X	X	C	B1T←B2R	B2T←B1R	
X	X	X	1	X	X	X	X	D1	B1T←B1R		
X	X	1	X	X	X	X	X	D2	B2T←B2R		
X	1	X	X	X	X	X	X	D3	BT1→BR1		
1	X	X	X	X	X	X	X	D4	BT2→BR2		

Table 5. Output pin connection status by channel selector control

Status Symbol	Output Pin Connection Status					Remarks
	BIT	B2T	DIN	BR1	BR2	
A1	1	—	*1	*1	*1	Initial Setting
A2	DOUT	—	B1R	*1	*1	
A3	BT1	—	*1	B1R	*1	
A4	BT2	—	*1	*1	B1R	
B1	—	1	*1	*1	*1	Initial Setting
B2	—	DOUT	B2R	*1	*1	
B3	—	BT1	*1	B2R	*1	
B4	—	BT2	*1	*1	B2R	
C	B2R	B1R	—	—	—	
D1	B1R	*3	—	*4	*4	
D2	*2	B2R	—	*4	*4	
D3	*2	*3	—	BT1	*4	
D4	*2	*3	—	*4	BT2	

Notes: 11. *1. According to the combination of A and B (Table 6).
*2. One of statuses A1 to A4 is held.
*3. One of statuses B1 to B4 is held.
*4. One of statuses A1 to A4 or one of statuses B1 to B4, whichever is written later, is held.
When the setting of C is performed before the setting of D group, the setting of D must be performed after the setting of the group A and B.

12. The statuses of the pins indicated by "—" is not affected.

13. DIN is connected to the digital input of CODEC and DOUT is connected to the digital output of CODEC.

Table 6. Output pin status by the combination of A and B

Setting of A	Setting of B	Output Pin Connection Status			Remarks
		DIN	BR1	BR2	
A1	B1	1	1	1	Initial Setting
	B2	B2R	1	1	
	B3	1	B2R	1	
	B4	1	1	B2R	
A2	B1	B1R	1	1	
	B2	B1R or B2R	1	1	DIN *5
	B3	B1R	B2R	1	
	B4	B1R	1	B2R	
A3	B1	1	B1R	1	
	B2	B2R	B1R	1	
	B3	1	B1R or B2R	1	BR1 *5
	B4	1	B1R	B2R	
A4	B1	1	1	B1R	
	B2	B2R	1	B1R	
	B3	1	B2R	B1R	
	B4	1	1	B1R or B2R	BR2 *5

*5. When writing is performed in the sequence of setting of A and setting of B, the output status becomes B2R, and when writing is performed in the sequence of setting of B and setting of A, the output status becomes B1R.

key scanning output control and interrupt

WRITE Mode
Address Data AD1 = 1, AD0 = 0

Control Data								Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	Output Data					The data set in DB4 to DB0 is output from output pins PO4 to PO0, respectively. The output statuses are held until the data is rewritten. When the data is "0", the output goes to "0", when the data is "1", the output is left open. Initially, PO4 to PO0 are left open.
1	X	X	X	X	X	X	X	Resets the INTT output and sets to "1". This control data is valid only when written, it is not held.

Sounder, volume, and tone combination

WRITE Mode
Address Data AD1 = 1, AD0 = 1

Control Data								Control	Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
0	0	X	X	X	X	0	0	Volume 1 (High)	The setting of volume and tone combination is performed simultaneously, not independently.
						0	1	Volume 2 (Medium)	
						1	0	Volume 3 (Low1)	
						1	1	Volume 4 (Low2)	
			0	0	0	X	X	Tone combination setting (Initial setting) by external control (SW0, SW1)	
			0	0	1			Tone combination 1 (1.0 kHz and 1.3 kHz, 16 Hz Wamble period)	Initially the high volume is set, and tone combination is set externally.
			0	1	0			Tone combination 2 (0.8 kHz and 1.0 kHz, 16 Hz Wamble period)	
			0	1	1			Tone combination 3 (0.8 kHz and 1.0 kHz, 8 Hz Wamble period)	
			1	0	1			Tone combination 4 (0.5 kHz and 0.65 kHz, 16 Hz Wamble period)	
			1	1	0			Tone combination 5 (0.4 kHz and 0.5 kHz, 16 Hz Wamble period)	
			1	1	1			Tone combination 6 (0.4 kHz and 0.5 kHz, 8 Hz Wamble period)	

CODEC power down control

WRITE Mode
Address Data AD1 = 1, AD0 = 1

Contorol Data								Control	Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
0	1	X	X	X	0	0	0	CODEC power-down is controlled by PDC (DB4) during sounder control. (Initial setting) PDC = 0 CODEC power-on PDC = 1 CODEC power-down	Data written later is valid.
					1	0	1	CODEC Transmit power-down	
					1	1	0	CODEC Receive power-down	
					1	1	1	CODEC Transmit and Receive power-down	
					1	0	0	CODEC power-down release	

Gain control

WRITE Mode
Address Data AD1 = 1, AD0 = 1

DB7								Control	Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	0	X	X	X	X	0	0	Sets the transmit PB tone and hold tone level at the typical value.(Initial setting)	The gain setting of the transmit path and the receive path can be performed simultaneously, not independently.
						0	1	Sets the transmit PB tone and hold tone level by 3 dB below the typical value.	
						1	X	Sets the transmit PB tone and hold tone level by 6 dB below the typical value.	
				0	0	X	X	Sets the receive gain at the typical value. (Initial setting)	
				0	1	X	X	Sets the receive gain by 3 dB above the typical value.	
				1	0	X	X	Sets the receive gain by 6 dB above the typical value.	
				1	1	X	X	Sets the receive gain by 9 dB above the typical value.	

Howler tone color combination

WRITE Mode
Address Data AD1 = 1, AD0 = 0

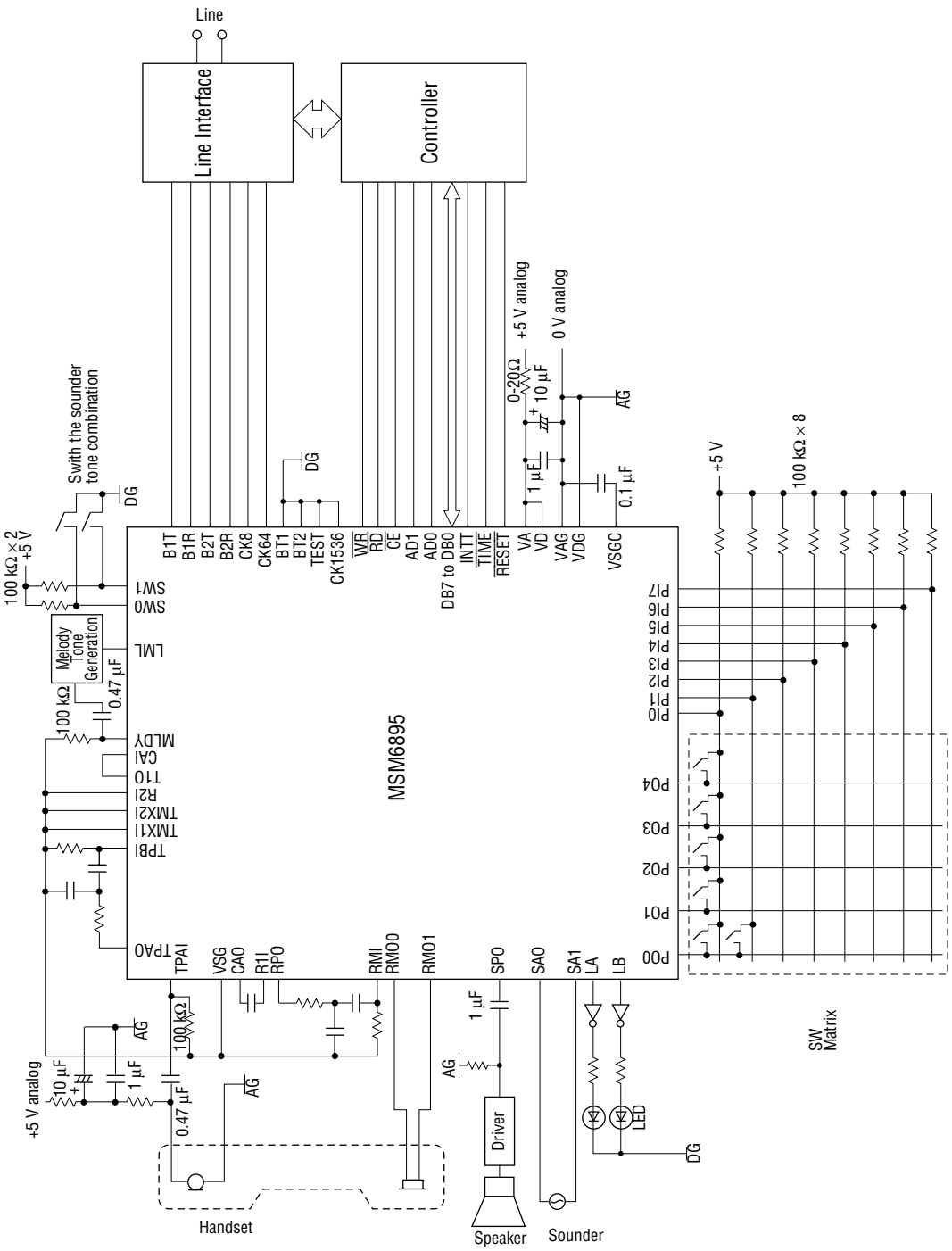
Control Data								Control	Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	1	X	X	X	X	X	0	Howler tone frequency: 0.8 kHz	Initial setting
							1	Howler tone frequency: 1.0 kHz and 1.3 kHz, 16 Hz Wamble period	

Key scanning data read out

READ Mode
Address Data AD1 = 1, AD0 = 0

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Control
PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	The data input to the pins PI7 to PI0 is output from DB7 to DB0, respectively.

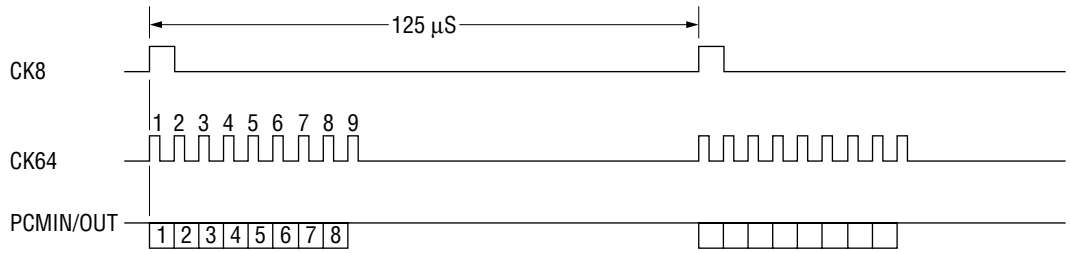
APPLICATION CIRCUIT



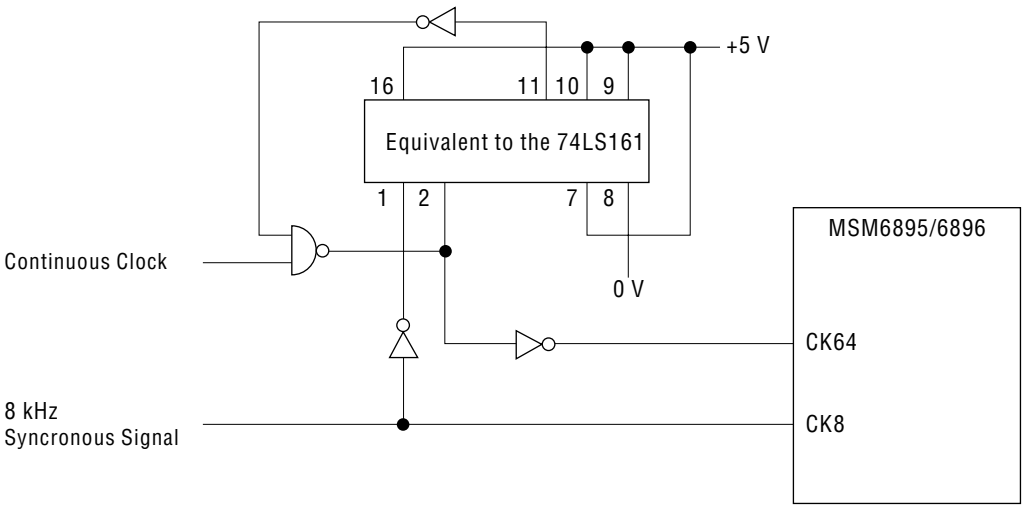
Application circuit at the PCM Signal Data Rate of 192, 384, 768, 1536 and 2048 kbps.

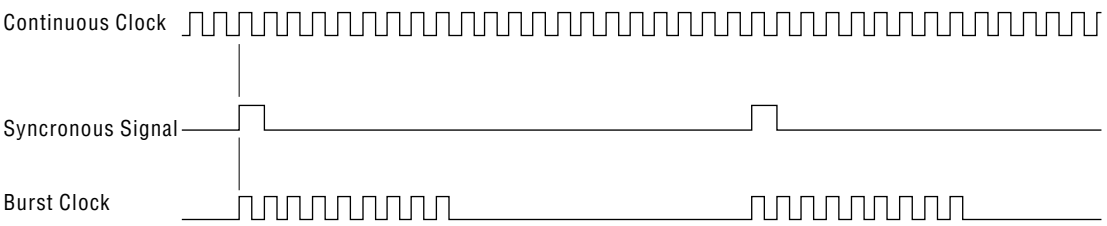
BCLOCK signal

When the PCM signal data rate is one of 192, 384, 768, 1536, and 2048 kbps, input the 9-bit burst clock corresponding to the frequency equivalent to each of the data rates, as CK64 signal.

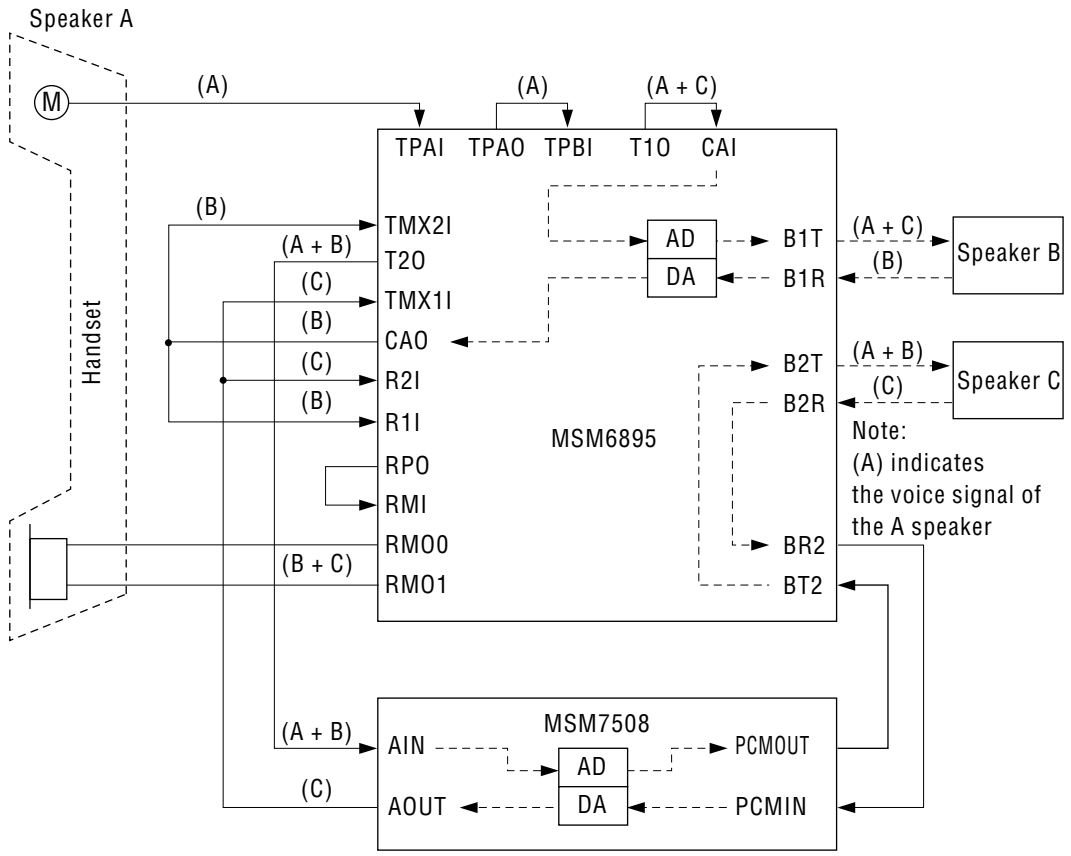


Burst clock generator





Application Circuit of Three-party Speech Path



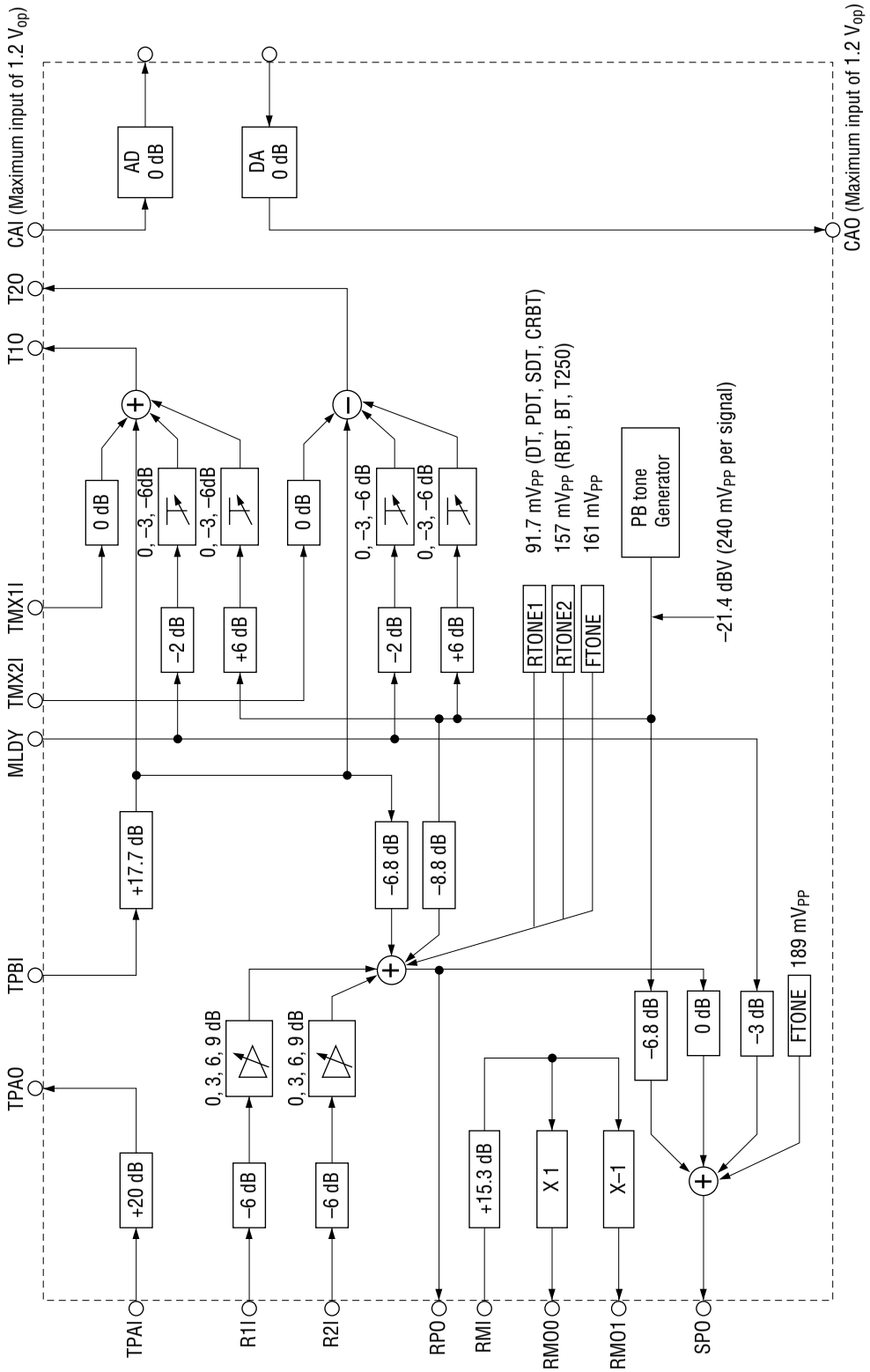
Speech path setting (Speech through a handset)

Transmit:	TA-4 (LT1 = 1, LMX1 = 1, LMN = 0, MUTN = 1)
	TB-4 (LT2 = 1, LMX2 = 1, LMN = 0, MUTN = 1)
Receive:	RP-8 (LT1 = 1, LT2 = 1, LMN = 0, MUTN = 1, LR = 1)

Channel selector control

A2, B4

SPEECH PATH GAIN



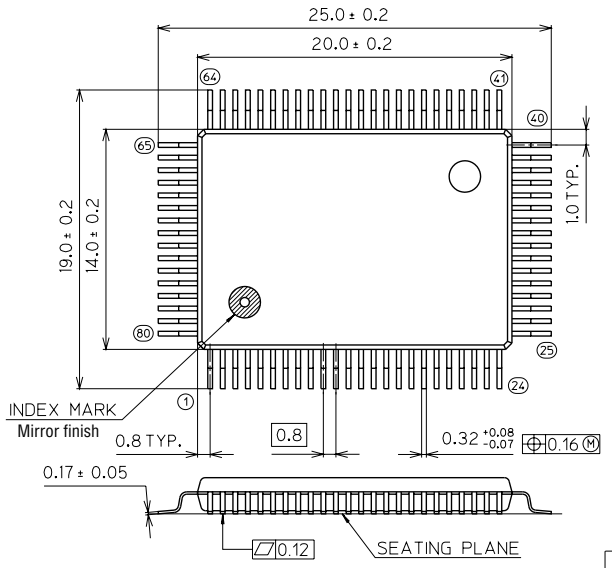
RECOMMENDATIONS FOR ACTUAL DESIGN

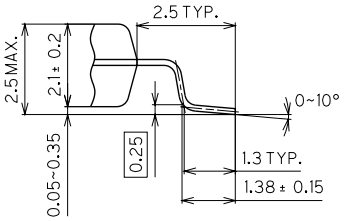
- To assure proper electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.
- Connect the AG pin and the DG pin each other as close as possible. Connect to the system ground with low impedance.
- Mount the device directly on the board when mounted on PCBs. Do not use IC sockets. If an IC socket is unavoidable, use the short lead type socket.
- When mounted on a frame, use electro-magnetic shielding, if any electro-magnetic wave source such as power supply transformers surround the device.
- Keep the voltage on the V_{DD} pin not lower than –0.3 V even instantaneously to avoid latch-up phenomenon when turning the power on.
- Use a low noise (particularly, low level type of high frequency spike noise or pulse noise) power supply to avoid erroneous operation and the degradation of the characteristics of these devices.
- Unused analog input pins must be connected to the VSG pin and unused digital pins must be connected to the GND pin.

PACKAGE DIMENSIONS

(Unit : mm)

QFP80-P-1420-0.80-BK





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	1.27 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).