FEDL2201-02
This version: July 12. 2004

OKI Semiconductor

ML2201-XXX

Speech Synthesizer LSI with on-chip 384K Mask ROM

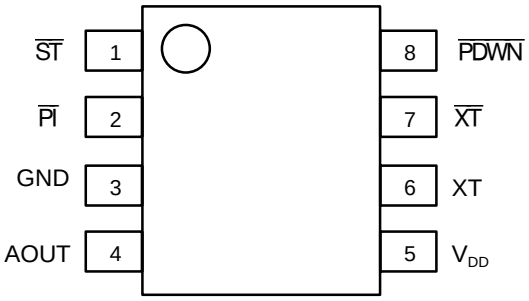
GENERAL DESCRIPTION

The ML2201 is a PCM-based speech synthesizer LSI having an on-chip 384K Mask ROM, D/A Converter and Low Pass Filter. Utilizing the serial interface enables smaller footprint packaging, which makes the chip an ideal choice for a pre-recorded message subsystem used with today's size-critical applications.

FEATURES

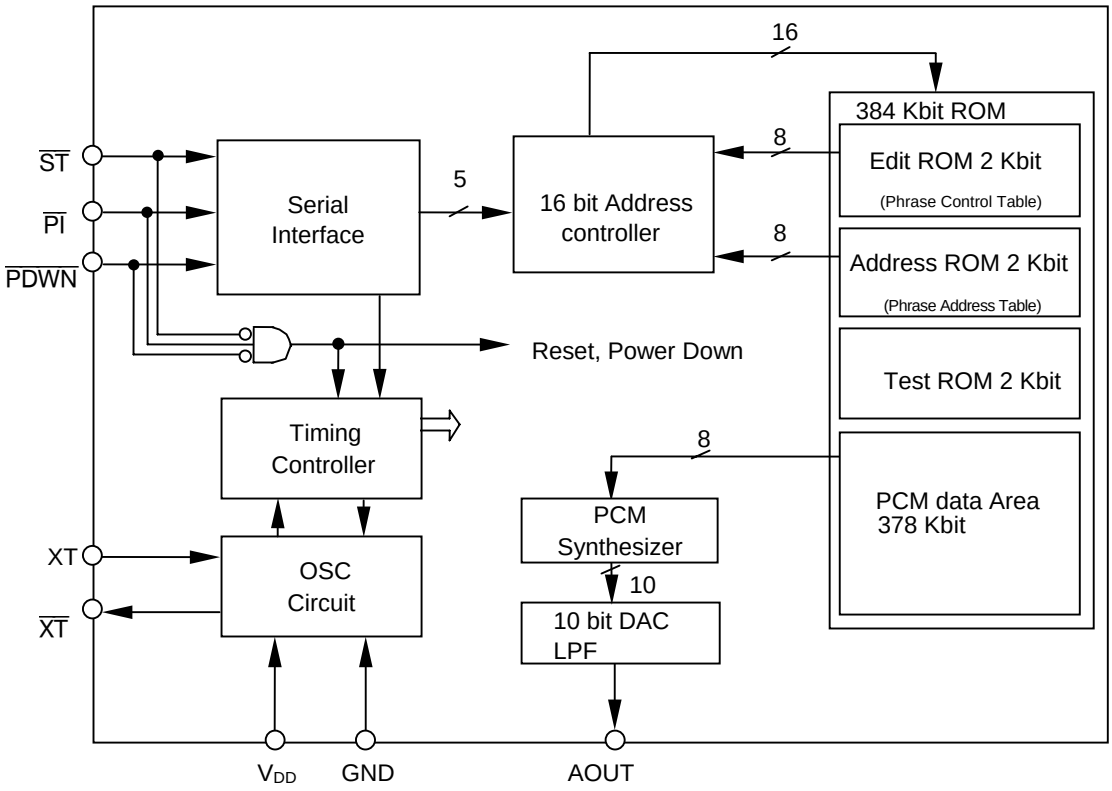
- 8bit Oki Non-Linear PCM
- Sampling Frequency (Selectable for each single phrase)
  4.0/5.3/6.4/8.0/10.6/12.8/16.0 kHz
- On-chip 384 Kbit Mask ROM
- Maximum Playback Time (At f_{OSC} = 4.096 MHz)
  12.0 sec At f_{SAM} = 4.0 kHz
  6.0 sec At f_{SAM} = 8.0 kHz
  3.0 sec At f_{SAM} = 16.0 kHz
- Clock Oscillation
  3.5 to 4.5MHz (Ceramic Oscillation)
  3.5 to 17MHz (External Clock)
- On-chip Phrase Control Table
- Maximum Number of Phrases: 31 Phrases
- Built-in 10-bit Current-Output Type D/A Converter
- Built-in LPF
- Power Supply Voltage: +2.0 to +5.5 V
- Packaging: 8-pin Plastic SSOP (SSOP8-P-44-0.65-K) (ML2201-XXX MBZ060)

PIN LAYOUT (TOP VIEW)



8-Pin Plastic SSOP

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	$\overline{ST}$	I	The playback trigger pin. The number of pulses input to the $\overline{PI}$ pin, while this pin is held "L", determines the Phrase Address for playback. At the $\overline{ST}$'s rising edge, the phrase address data is loaded into the LSI and playback starts. When no pulse input to $\overline{PI}$ occurs while this pin is held "L", the LSI recognizes it as the "Stop Code" that results in stopping playback.
2	$\overline{PI}$	I	The address input pin. The number of pulses input to this pin, while the $\overline{ST}$ pin is held "L", determines the Phrase Address for playback. When 32 pulses are input, the internal counter returns to its initial value, "0".
3	GND	—	The ground pin.
4	AOUT	O	The analog output pin. Configured as N-MOS open drain, analog signal is output in the form of change in output (attraction) current. While the $\overline{PDWN}$ pin being held "H", this pin is sustained at 1/2 level and thus the current keeps on flowing. When shifting to standby state and shifting back to ready state from standby, the pop-noise canceller is put to work.
5	V_{DD}	—	The power supply pin. Insert a 0.1 μF bypass capacitor between this pin and the GND pin.
6	XT	I	Wired to the ceramic oscillator when a ceramic oscillator is in use. Input the clock signal to this pin when the external clock is selected as the timing source. Using a ceramic oscillator or an external clock can be selected with OKI's Analizing and Editing Tool.
7	$\overline{XT}$	O	Wired to the ceramic oscillator when a ceramic is in use. When the external clock is in use, keep this pin open.
8	$\overline{PDWN}$	I	The power down pin. The LSI stays standby state while the pin being held "L".

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +7.0	V
Input Voltage	V_{IN}		–0.3 to V_{DD} +0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Power Supply Voltage	V_{DD}	f_{OSC} = 3.5 to 4.5 MHz	+2.0 to +5.5			V
		f_{OSC} = 3.5 to 13.5 MHz (external clock)	+2.6 to +5.5			V
		f_{OSC} = 3.5 to 17.0 MHz (external clock)	+3.0 to +5.5			V
Master Clock Frequency	f_{OSC}		Min.	Typ.	Max.	MHz
		V_{DD} = 2.0 to 5.5 V	3.5	4.096	4.5	
		V_{DD} = 2.6 to 5.5 V	3.5	—	13.5	
		V_{DD} = 2.7 to 5.5 V	3.5	—	14.5	
		V_{DD} = 3.0 to 5.5 V	3.5	—	17.0	
Operating Temperature	T_{OP}	—	–40 to +85			°C

Note: A ceramic resonator that is usable in this LSI is described in “Functional Description” of this document.
If you want to use a different crystal, it is recommended to evaluate the resonator before using it.

ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{DD} = 2.0 to 5.5 V, GND = 0 V, f_{OSC} = 4.096 MHz, Ta = –40 to +85°C (unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	f_{OSC} > 14.5 MHz (external clock) V_{DD} = 3.0 to 5.5 V		V_{DD} × 0.85	—	—	V
		f_{OSC} ≤ 14.5 MHz (external clock) V_{DD} = 2.7 to 5.5 V		V_{DD} × 0.8	—	—	V
		f_{OSC} ≤ 13.5 MHz (external clock) V_{DD} = 2.6 to 2.7 V		V_{DD} × 0.85	—	—	V
		f_{OSC} ≤ 4.5 MHz V_{DD} = 2.0 to 5.5 V		V_{DD} × 0.8	—	—	V
"L" Input Voltage	V_{IL}	f_{OSC} > 14.5 MHz (external clock) V_{DD} = 3.0 to 5.5 V		—	—	V_{DD} × 0.15	V
		f_{OSC} ≤ 14.5 MHz (external clock) V_{DD} = 2.7 to 5.5 V		—	—	V_{DD} × 0.2	V
		f_{OSC} ≤ 13.5 MHz (external clock) V_{DD} = 2.6 to 2.7 V		—	—	V_{DD} × 0.15	V
		f_{OSC} ≤ 4.5 MHz V_{DD} = 2.0 to 5.5 V		—	—	V_{DD} × 0.2	V
"H" Input Current	I_{IH}	V_{IH} = V_{DD}		—	—	10	μA
"L" Input Current	I_{IL}	V_{IL} = GND		–10	—	—	μA
Supply Current	I_{DD}	Except AOUT output current	V_{DD} = 5.5 V f_{OSC} = 4.096 MHz	—	1.7	3.9	mA
			V_{DD} = 3.0 V f_{OSC} = 4.096 MHz	—	0.9	2.1	mA
			V_{DD} = 2.0 V f_{OSC} = 4.096 MHz	—	0.5	1.4	mA
			V_{DD} = 5.5 V f_{OSC} = 16 MHz	—	4.6	12.0	mA
			V_{DD} = 3.0 V f_{OSC} = 16 MHz	—	1.8	6.5	mA
Standby Current	I_{DS}	Ta = –40 to +70°C		—	—	10	μA
		Ta = –40 to +85°C		—	—	50	μA
AOUT Output Current	I_{AOUT}	At max. output current	V_{DD} = 2.0 to 5.5 V	0.5	—	10.0	mA
			V_{DD} = 5.5 V	4.3	6.8	10.0	mA
			V_{DD} = 3.0 V	1.4	2.7	3.9	mA
			V_{DD} = 2.0 V	0.5	1.2	2.2	mA

AC Characteristics

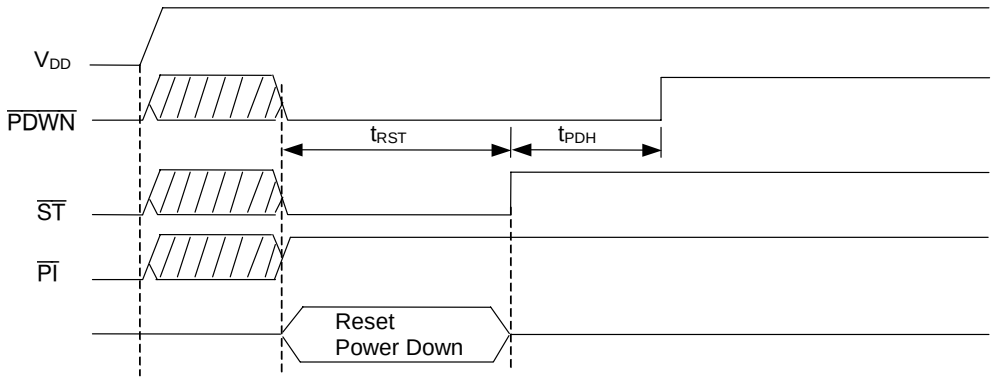
V_{DD} = 2.0 to 5.5 V, GND = 0 V, f_{osc} = 4.096 MHz, Ta = –40 to +85°C (unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock Oscillation Duty Cycle	f_{DUTY}	—	40	50	60	%
Reset Input Time after Powering Up	t_{RST}	—	10	—	—	µs
$\overline{PDWN}$ Hold Time after Reset Input	t_{PDH}	—	10	—	—	µs
D/A Converter Transit Time (Pop-Noise Canceller Work Time) Note *1	t_{DAR}, t_{DAF}	—	60	64	68	ms
$\overline{PDWN}$ – $\overline{ST}$ Setup Time	t_{PDSS}	—	1	—	—	µs
$\overline{ST}$ – $\overline{PI}$ Setup Time	t_{SPS}	—	1	—	—	µs
$\overline{PI}$ Pulse Width	t_{PW}	—	0.35	—	2000	µs
$\overline{PI}$ Cycle Time	t_{PC}	—	0.7	—	4000	µs
$\overline{ST}$ – $\overline{PI}$ Hold Time	t_{SPH}	—	1	—	—	µs
$\overline{ST}$ – AOUT Setup Time Note *2	t_{SAS}	At f_{SAM} = 8.0 kHz		—	1050	µs
Phrase Stop Time Note *2	t_{DPS}	At f_{SAM} = 8.0 kHz		—	700	µs
Silence Time between Phrases Note *2	t_{BLN}	At f_{SAM} = 8.0 kHz		—	700	µs
Stop $\overline{ST}$ Pulse Width	t_{SSW}	—	0.35	—	2000	µs
Phrase $\overline{ST}$ – Phrase $\overline{ST}$ Pulse Duration Note *2	t_{PP}	At f_{SAM} = 8.0 kHz	1050	—	—	µs
Phrase $\overline{ST}$ – Stop $\overline{ST}$ Pulse Duration Note *2	t_{PS}	At f_{SAM} = 8.0 kHz	1050	—	—	µs
Stop $\overline{ST}$ – Phrase $\overline{ST}$ Pulse Duration Note *2	t_{SP}	At f_{SAM} = 8.0 kHz	500	—	—	µs
Sampling Frequency Note *3	f_{SAM}	—	3.9	—	28.0	kHz

Note *1: The value changes in proportion to the external clock frequency, f_{osc}.
Note *2: The value changes in proportion to the sampling frequency, f_{SAM}.
Note *3: The sampling frequency(f_{SAM}) is determined by the oscillation frequency(f_{osc}), and the dividing factor that is selected for each phrase.

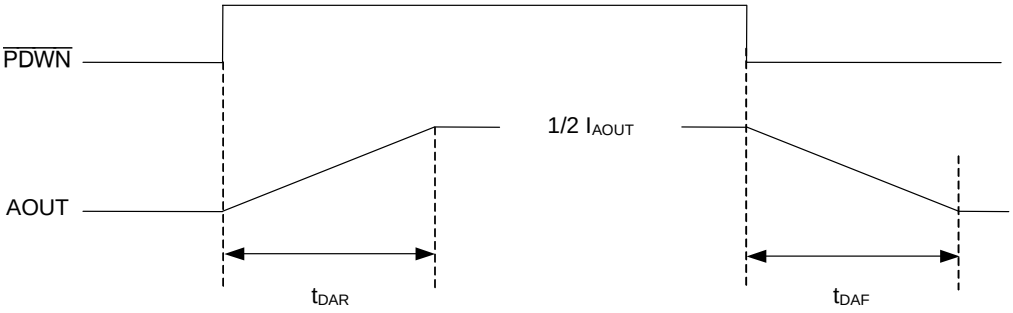
TIMING DIAGRAMS

Timing Diagram at Powering On

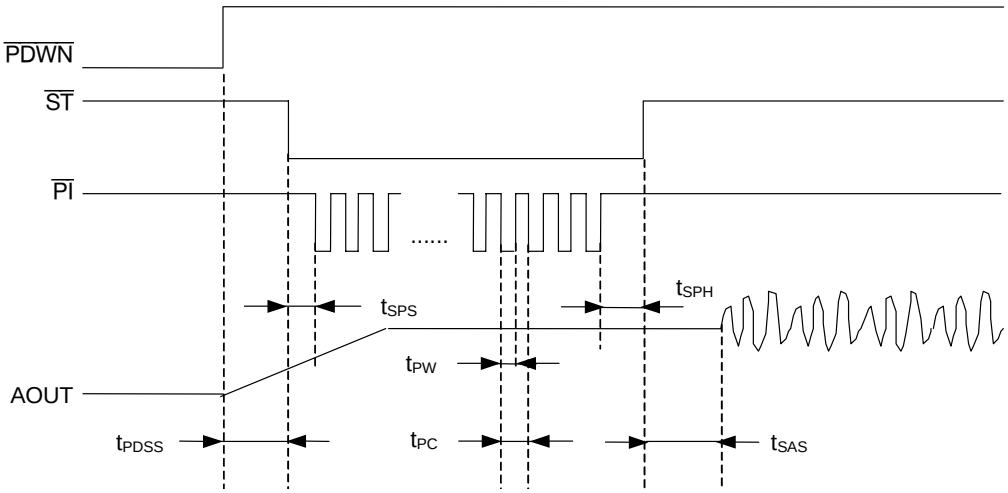


NOTE: The LSI's reset operation can be performed by using a level input combination of $\overline{PDWN}$ = "L", $\overline{ST}$ = "L" and $\overline{PI}$ = "H". After powering on, the initial reset operation is required at the above timing.

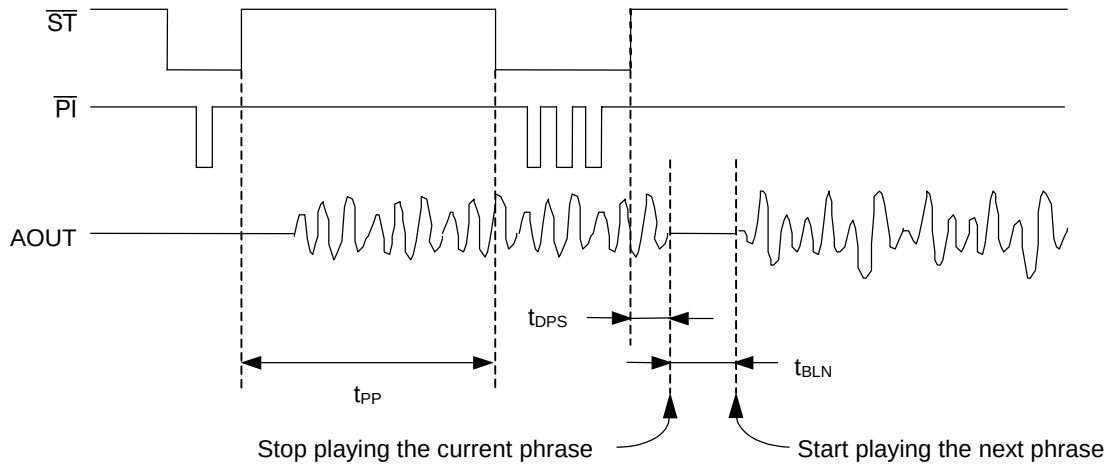
Timing Diagram at Powering Up and Standby State



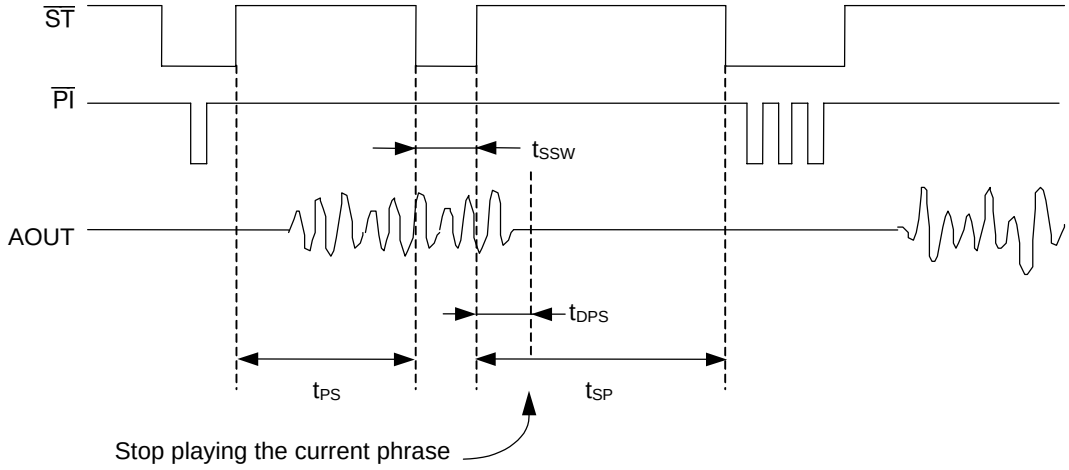
Timing Diagram for Playback



Timing Diagram on Re-addressing while Playing



Timing Diagram on Stop Code Input



FUNCTIONAL DESCRIPTION

Sampling Frequency

You can select a sampling frequency for each phrase address from the following list while you are working on sound data. Select a sampling frequency that satisfies f_{SAM} = 3.9 to 28.0 kHz from the values obtained with the dividing factors as shown in the Table 1 below.

Table 1 Sampling Frequency

Sampling Frequency At f_{OSC} = 4.096 MHz	Dividing Factor
4.0 kHz	$f_{OSC}/1024$
5.3 kHz	$f_{OSC}/768$
6.4 kHz	$f_{OSC}/640$
8.0 kHz	$f_{OSC}/512$
10.6 kHz	$f_{OSC}/384$
12.8 kHz	$f_{OSC}/320$
16.0 kHz	$f_{OSC}/256$

Memory Allocation and Playback Time Length

As shown in the Figure 1, the on-chip Mask ROM of ML2201 is partitioned into four areas, Phrase Control Table, Address Control Table, Test Data area and User's Data area. The actual data area where user's sound data can be stored is 378 Kbit, that is the total on-chip Mask ROM capacity minus 6 Kbit.

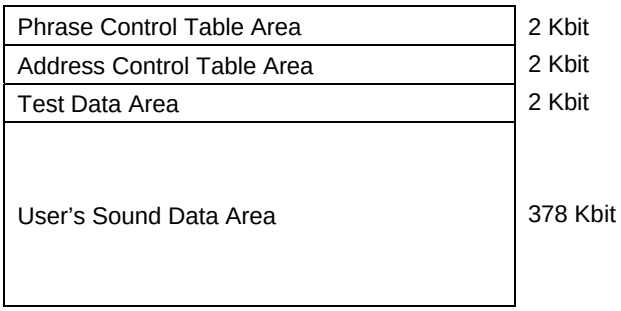


Figure 1 On-chip Mask ROM (384 Kbit) Memory Allocation

You can calculate playback time length with memory size divided by a bit rate. The following formula can be used for 8-bit PCM-based ML2201;

$$\text{Playback Time (sec)} = \frac{\text{Memory Size (Bit)}}{\text{Bit Rate (bps)}} = \frac{\text{Memory Size (Bit)}}{\text{Ext. Clock Frequency (Hz)} \times 8}$$

For example, when you store all phrases at 8.0 kHz Sampling Frequency, the maximum playback time is calculated as follows;

$$\text{Playback Time (sec)} = \frac{(384 - 6) \times 1024 \text{ Bit}}{8000 \text{ (Hz)} \times 8 \text{ Bit}} \cong 6.0 \text{ sec}$$

Playback Algorithm

ML2201 uses OKI Non-Linear PCM algorithm, an advanced variation of PCM.
In mid-range wave-form, this algorithm has precision and quality equivalent to those of 10-bit Straight PCM.

Inserting Silence

In addition to playing normal recorded sound phrases, ML2201 allows you to insert silence (a silent phrase) . You can define time length of silence freely in 32 ms steps, within the range of minimum 32 ms and maximum 992 ms at f_{OSC} = 4.096 MHz. Those time length vary in proportion to the oscillation frequency, f_{OSC}.

Phrase Control Table

The user-definable on-chip Phrase Control Table feature enables you to play back multiple phrases in a single continuous session with just the same simple control as in a regular single phrase playback. You can assign up to 8 phrases including a silent phrase (s) to a single address. This allows you to get the most out of limited memory space because you can eliminate duplicate sound data.

As an example, let's assume you want to create several similar phrases like "It will be xxxxx today". "xxxxx" can be "sunny", "rainy" or "cloudy". The common words such as "It", "will be" and "today" are created separately as an independent phrase, and phrasing order information is stored in the Phrase Control Table, as shown in the Table 2 and Figure 2.1. From the external control, simply selecting an X address causes the LSI to play multiple phrases continuously. In this example shown in the Table 2, selecting [01] address starts to play "It will be fine today, while selecting [02] "It will be rainy today".

You can also insert a silent phrase to the Phrase Control Table without consuming any memory space.

Minimum Time Length of Silence	32 ms
Maximum Time length of Silence	992 ms
Incremental Step	32 ms

Table 2 Phrase Control Table Data

No.	X Address (HEX)	Y Address (Phrasing Order) (Up to 8 phrases)								Playback
1	01	[01]	[02]	Silence	[04]	[03]				It will be (Silence) fine today.
2	02	[01]	[02]	Silence	[05]	[03]				It will be (Silence) rainy today.
3	03	[01]	[02]	[04]	[09]	[06]	[0A]	[05]	[03]	It will be fine, later cloudy, occasionally rainy.
:	:									:
30	1 E									
31	1 F									

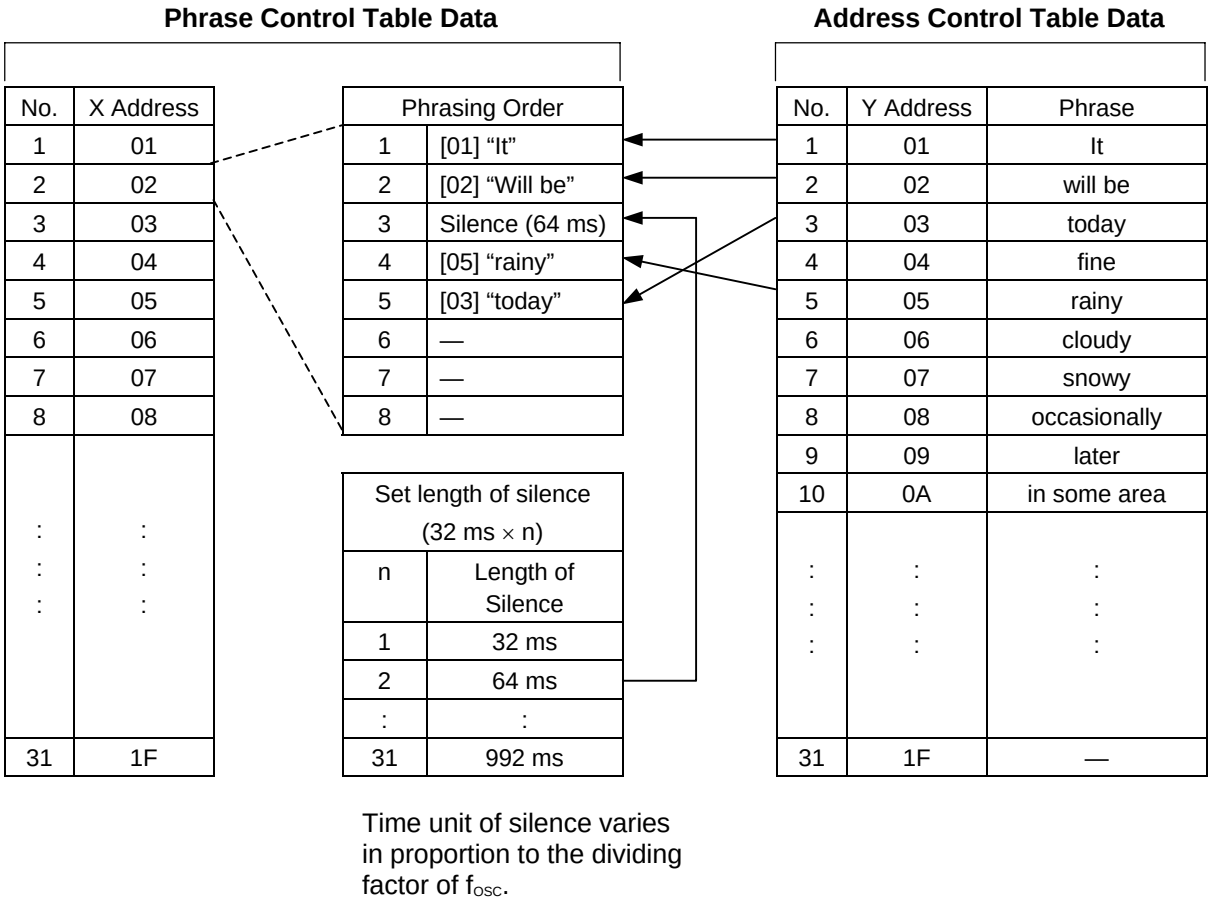


Figure 2.1 Phrase Data Combination for Use with Phrase Control Table

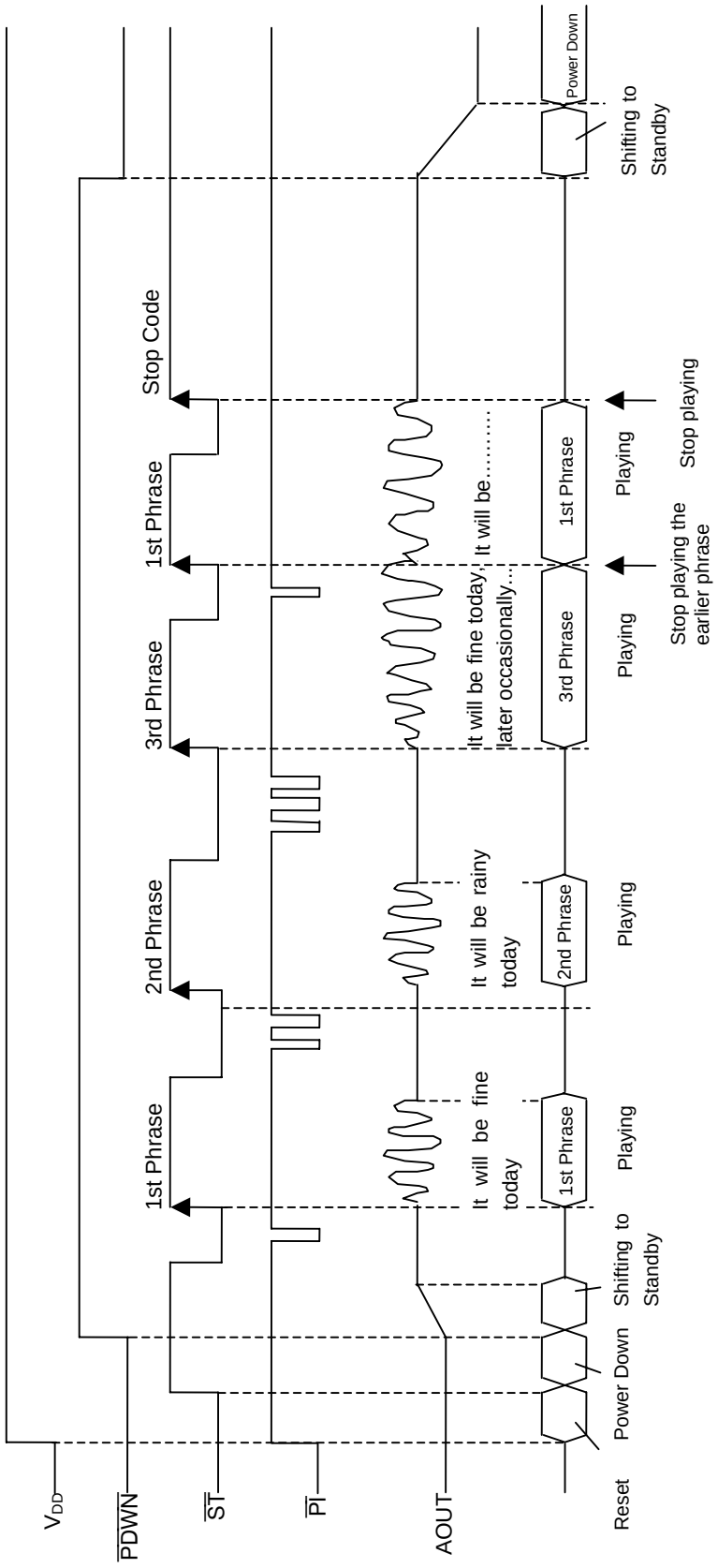


Figure 2.2 Timing Diagram for Playback with Phrase Control Table Function

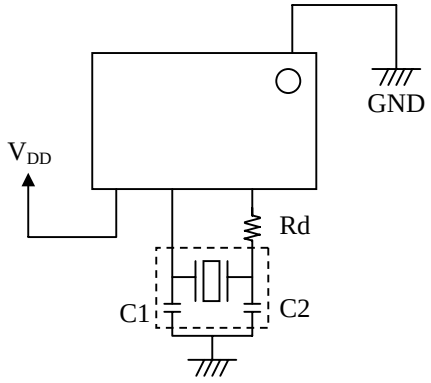
Oscillation, Clock Signal Input

The optimal load capacities when connecting ceramic resonators from KYOCERA CORPORATION, TDK CORPORATION and MURATA MFG., are shown below for reference.

KYOCERA

Freq [Hz]	Type	Optimal load capacity				Supply Voltage Range[V]	Operating Temperature Range[°C]
		C1 [pF]	C2 [pF]	Rf [Ohm]	Rd [Ohm]		
4.0M	KBR-4.0MKC	33 (internal)		---	1.5k	2.1 to 5.5	-40 to +85
	KBR-4.0MSB	33	33				
	PBRC4.00H	33 (internal)					
	PBRC4.00G	33	33				

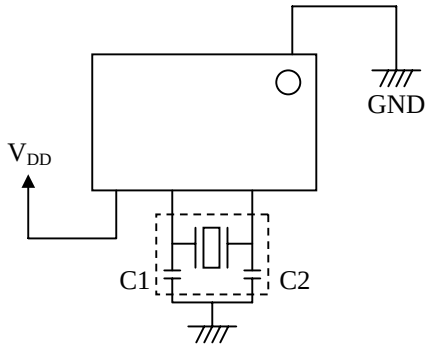
Oscillation circuit diagram using a Ceramic resonator



TDK CORPORATION

Freq [Hz]	Type	Optimal load capacity				Supply Voltage Range[V]	Operating Temperature Range[°C]
		C1 [pF]	C2 [pF]	Rf [Ohm]	Rd [Ohm]		
4.0M	FCR4.0MC5	30 (internal)		---	---	2.0 to 5.5	-40 to +85

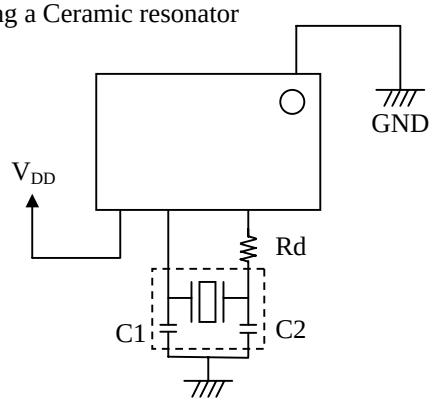
Oscillation circuit diagram using a Ceramic resonator



MURATA MFG.,

Freq [Hz]	Type	Optimal load capacity				Supply Voltage Range[V]	Operating Temperature Range[°C]
		C1 [pF]	C2 [pF]	Rf [Ohm]	Rd [Ohm]		
4.0M	CSTS0400MG06	47 (internal)		---	220	2.2 to 5.5	-40 to +85
	CSTCR4M00G55-R0	39 (internal)					

Oscillation circuit diagram using a Ceramic resonator



External Clock Input

The Figure 3 shows wiring of an external timing source.
(A type of the external clock should be determined at selecting chip options.)

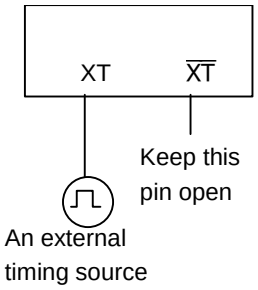


Figure 3 External Clock Input

Low Pass Filter

ML2201's analog output goes through the built-in Low Pass Filter. The Figure 4 below shows Frequency Characteristics and the Table 3 shows Cut-Off Frequency of the LPF.
The LPF's Frequency Characteristics and Cut-Off Frequency change in proportion to the sampling frequency. No analog output directly from the D/A converter is unavailable on this chip.

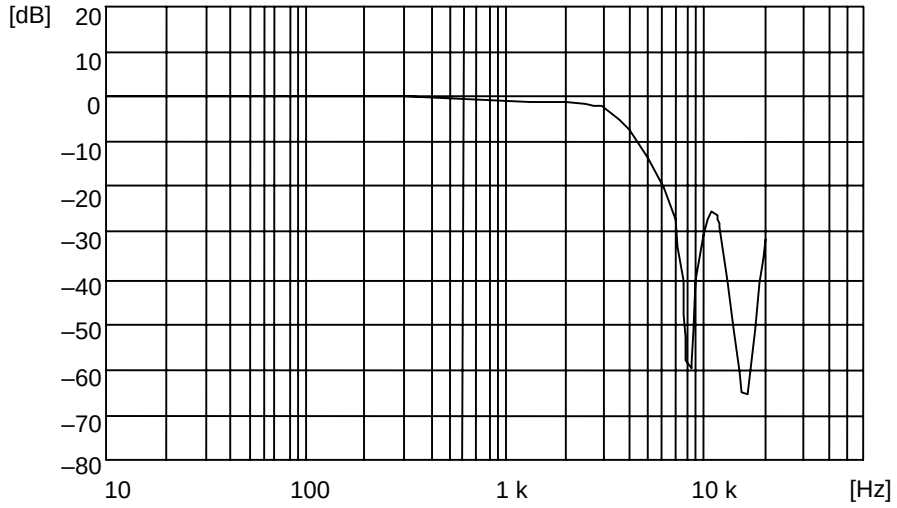


Figure 4 LPF Frequency Characteristics (f_{SAM} = 8.0 kHz)

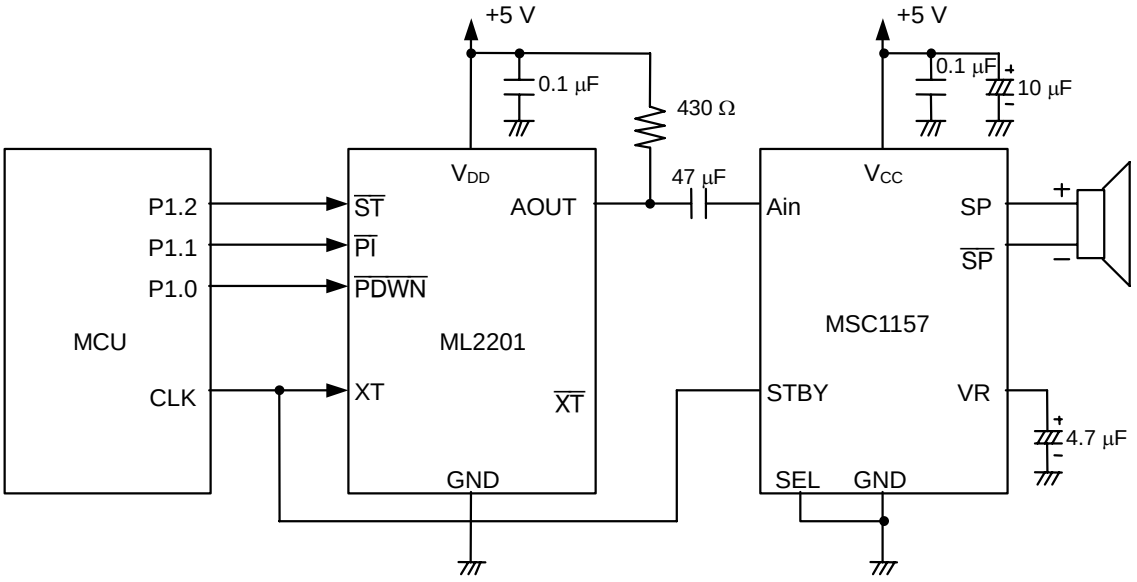
Table 3 LPF Cut-Off Frequency

Sampling Frequency (kHz) (f_{SAM})	Cut-Off Frequency (kHz) (f_{CUT})
4.0	1.2
5.3	1.6
6.4	2.0
8.0	2.5
10.6	3.2
12.8	4.0
16.0	5.0

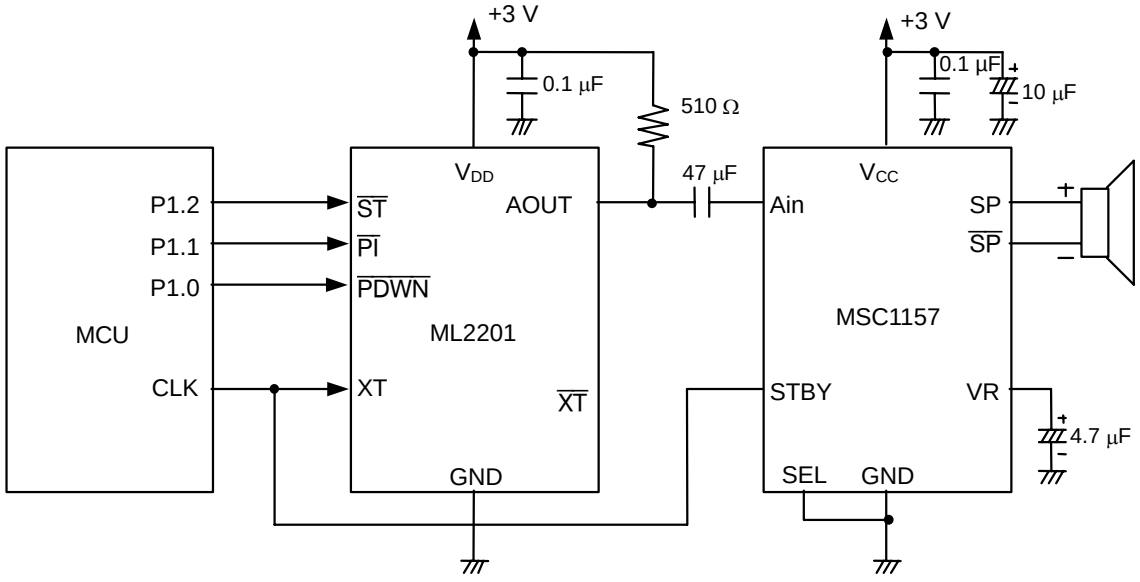
CONNECTING ML2201 TO A SPEAKER DRIVER

ML2201 uses a D/A converter of current-output type.
To connect ML2201 to a voltage-input type speaker driver, you should convert "Changes in Current" output to "Changes in Voltage" signal. The following samples show connections of ML2201 and MSC1157 (OKI Speaker Driver Amplifier) using a resistor (RL) for conversion.

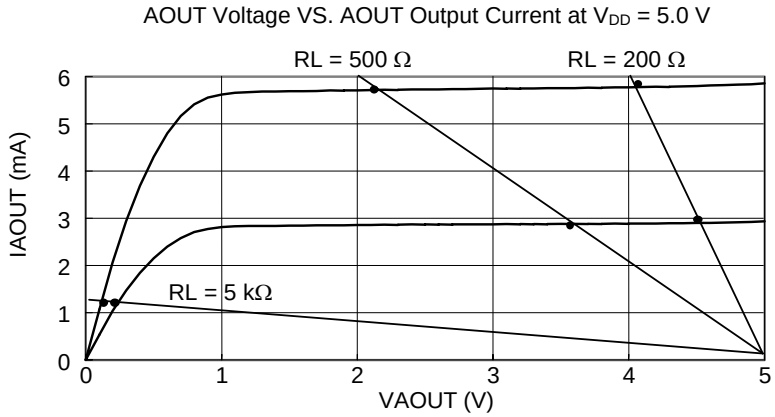
SAMPLE CIRCUIT 1: AT V_{DD} = 5.0 V, MSC1157'S Ain AMPLIFICATION = 2.5 V_{P-P}

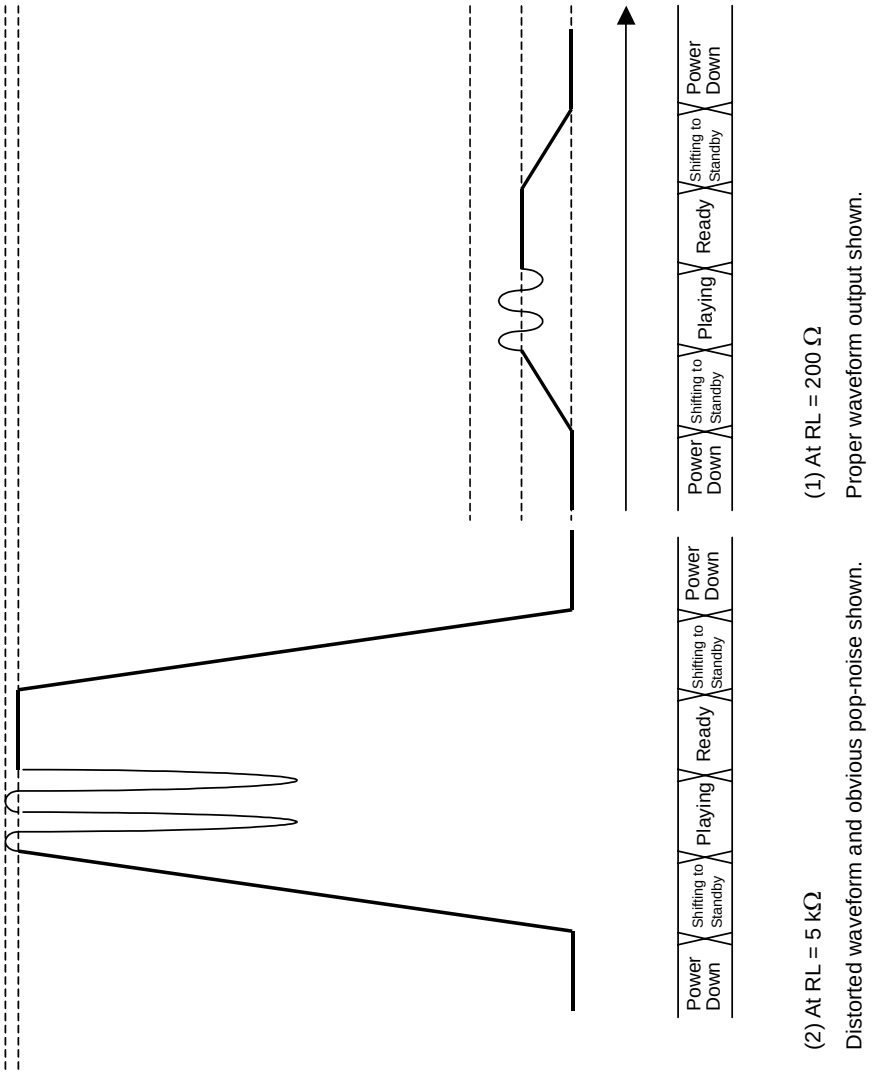


SAMPLE CIRCUIT 2: AT V_{DD} = 3.0 V, MSC1157'S Ain AMPLIFICATION = 1.5 V_{P-P}



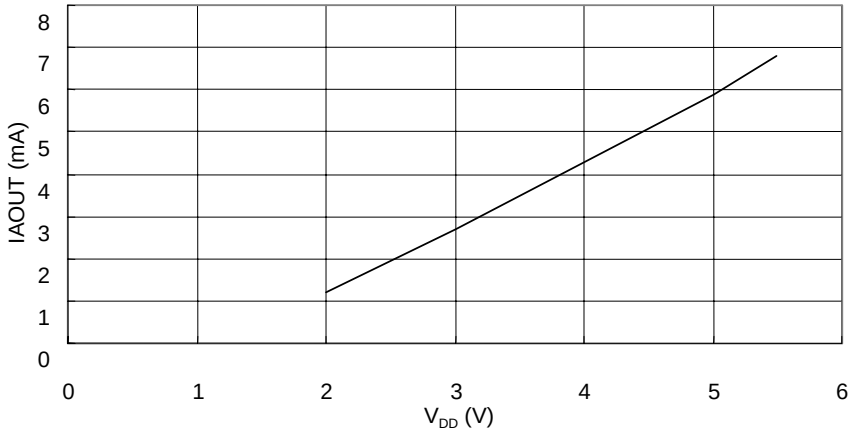
Co-relationship between output voltage and the value of a resistor for current-voltage conversion is shown in the figure below. You may want to use the figure as a reference in determining a proper value for the resistor.



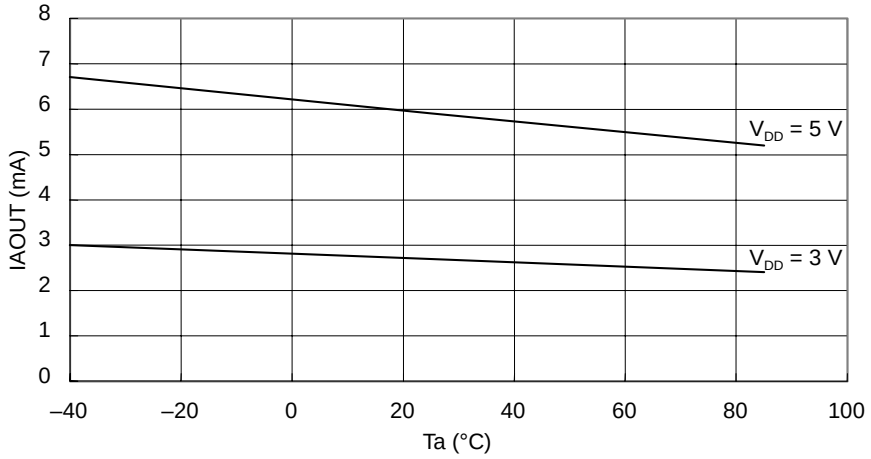


A SAMPLE CHARACTERISTICS OF D/A CONVERTER OUTPUT CURRENT

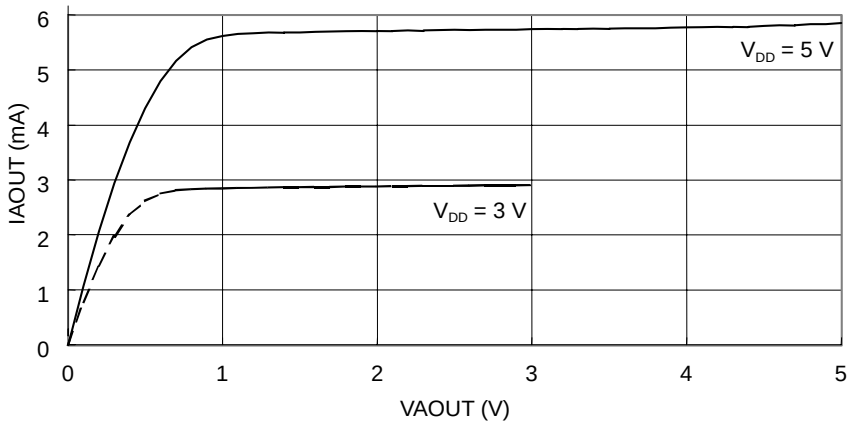
A Sample Characteristics : Power Supply Voltage VS. AOUT Output Current
(Ta = 25°C, VAOUT = V_{DD}, PCM at Max. level)



A Sample Characteristics : Operating Temperature VS. AOUT Output Current
(VAOUT = V_{DD}, PCM at Max. level)



A Sample Characteristics: Voltage on AOUT Pin VS. AOUT Output Current
(Ta = 25°C, PCM at Max. level)

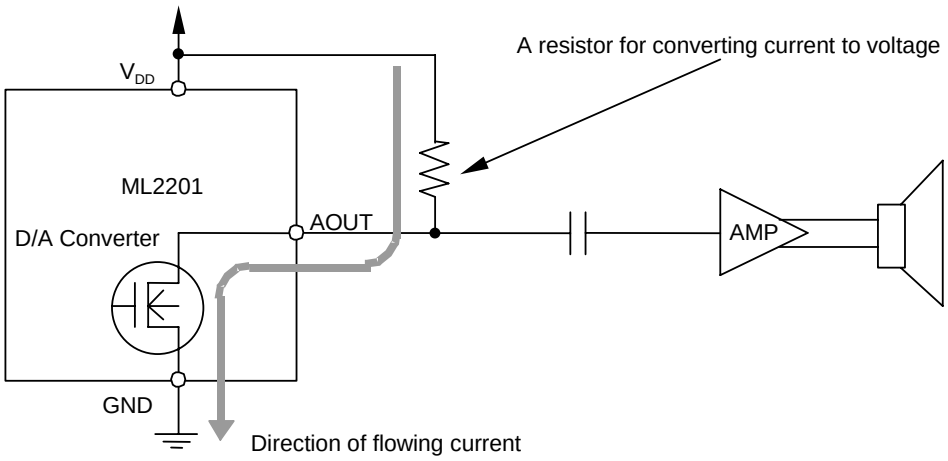


NOTES ON USAGE

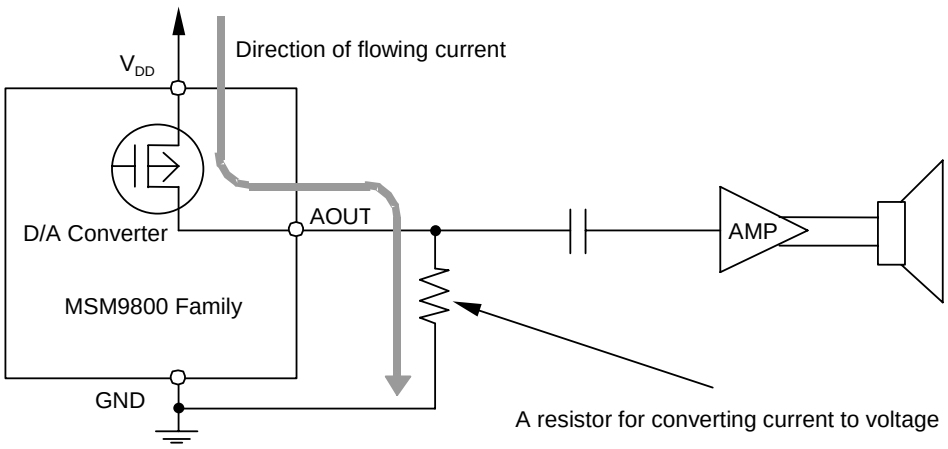
Type of the Built-in D/A Converter
ML2201 has the built-in current-output type D/A converter and thus the design of analog output circuit is different from the one with a voltage-output type D/A converter (e.g. MSM6650 family).
ML2201's D/A converter is designed as current attraction type with the same circuit configuration with the one used on MSM9831. So, the analog output circuit is different from MSM9800 family that uses a current discharge type D/A converter. (See the table below)

Product	D/A Converter Type	D/A Converter Output Circuit
ML2201	Current Output (flowing-in) type	N-MOS Open Drain
MSM9831	Current Output (flowing-in) type	N-MOS Open Drain
MSM9800 Family	Current Output (flowing-out) type	P-MOS Open Drain
MSM6650 Family	Voltage Output type	—

A sample circuit of connecting ML2201 and an amplifier chip



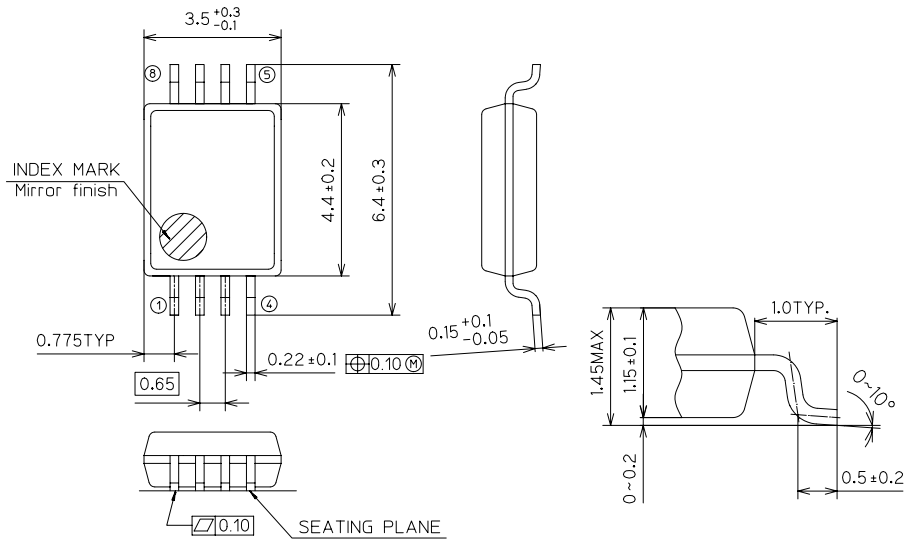
A sample circuit of connecting MSM9800 family and an amplifier chip



PACKAGE DIMENSIONS

(Unit: mm)

SSOP8-P-44-0.65-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.044 TYP.
Rev. No./Last Revised	1/May.12,1999

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Packages

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL2201-01	March, 2000	-	20	Final Edition 1
FEDL2201-02	July. 12, 2004	-	-	Added mentioned about Ceramic Oscillation.

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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