

## General Description

The ML5401 is a voltage regulator IC consisting of two voltage regulators, both of which have their own output voltage identifier pins. The minimum output capacitance requirement is 33uF. Reference voltage is a trimmed band gap within 1% accuracy.

Under voltage lockout circuitry protects against unregulated output voltages when the input voltage is below specification.

Current limit protects against short circuit current, and on chip over temperature circuitry limits the maximum die temperature.

The current delivery capability of this device is directly dependent on the thermal management implementation by the board designer and the package selection. High power packages may have a significant impact on the average unit price of this product.

## Features

- Two independent outputs
- Line regulation: 0.5% Maximum
- Load regulation: 0.8% Maximum
- Under-voltage lockout
- Over Temperature protection
- Selectable output voltages individually
- Current limit protection
- 8-pin WSON Package(P-WSON8-0605-1.27-M)

## Applications

- Hard Disk Drives, CD-ROMs
- Set-top Boxes
- Motherboards with multiple supplies
- Printers
- Cellular phones
- Cordless phones

### Block Diagram

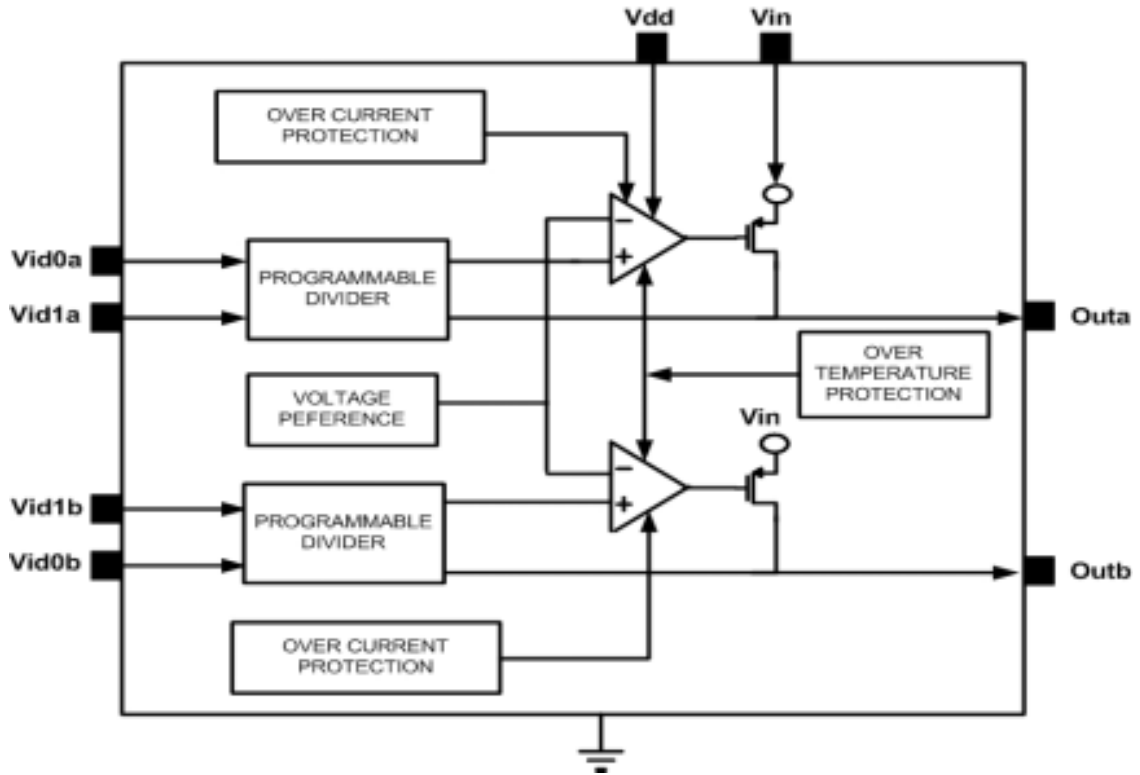


Figure 1: Block diagram of ML5401

## PIN DESCRIPTION

Pin Name	Pin Number	Pin Function
Vid0a	1	Output voltage identifier, see Table 1
Vid1a	2	Output voltage identifier, see Table 1
Vid0b	3	Output voltage identifier, see Table 1
Vid1b	4	Output voltage identifier, see Table 1
Vdd	5	Power supply
Outb	6	Channel B output
Vin	7	Input voltage
Outa	8	Channel A output
Gnd	9	Ground (Exposed Pad)

Vid1	Vid0	Output Voltage
1	0	1.2V
1	1	1.5V
1	F	1.8V
F	F	2.5V

**Float is open condition.**

Table 1: Output Voltage Selection Codes (F = Floating condition, 1 = Vdd, and 0 = Gnd)

## Absolute maximum rating

Parameter	Symbol	Conditions	Range	Units
Power Supply	VIN, VDD	Ta=25°C, GND=0V	-0.3 to 6.5	V
Input Voltage	Vid		-0.3 to VDD + 0.3	V
Output Voltage	Vout		-0.3 to VIN + 0.3 < VDD + 0.3V	V
Input Current	Ii		-1 to +1	mA
Output Current	Io		TBD	mA
Maximum Power Dissipation		-	TBD	W
Junction Temperature	Tj	-	150	°C
Storage Temperature	TSTG	-	-65 to 150	°C

## Recommended Operating Conditions

GND=0.0V

Parameter	Conditions	Min	Typ.	Max	Units
Power Supply (VIN)		3.0	3.3	3.6	V
Power Supply (VDD)		4.5	5.0	5.5	V
Output Current *			750		mA
Operating Junction Temperature		0		125	°C

\*: The total Current of Outa pin and Outb pin must be less than 750mA.

## Electrical Specifications

Typicals and limits appearing in normal type apply for TJ = 25°C. Limits appearing in **Boldface** type apply over the entire junction temperature range of operation, 0°C to 125°C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
<i>Vid Pins interface *</i>						
H level Input Voltage	VIH		<b>0.8*VDD</b>			V
L level Input Voltage	VIL				<b>0.2*VDD</b>	V
H level Leak Current	IIH	Vi=VDD			<b>50</b>	µA
L level Leak Current	IIL	Vi=GND	<b>- 50</b>			µA
Quiescent current	IDDS	Vid1A=Vid0A=Vid1B=Vid0=GND, OUTA=OUTB=open			<b>6.0</b>	mA

\*: Vid pins are vid1a,vid0a,vid1b and vid0b .

## Electrical Specifications

Typicals and limits appearing in normal type apply for  $T_J = 25^\circ\text{C}$ . Limits appearing in **Boldface** type apply over the entire junction temperature range of operation,  $0^\circ\text{C}$  to  $125^\circ\text{C}$ .

Parameter	Conditions	Min.	Typ.	Max.	Units
Reference voltage		<b>0.891</b>	0.9	<b>0.909</b>	V
Output Voltage (note 2)					
Vout 1.2V	$0 < I_{out} < 750\text{mA}$ , $3 < V_{in} < 3.6$	<b>1.176</b>	1.2	<b>1.224</b>	V
Vout 1.5V	$0 < I_{out} < 750\text{mA}$ , $3 < V_{in} < 3.6$	<b>1.470</b>	1.5	<b>1.530</b>	V
Vout 1.8V	$0 < I_{out} < 750\text{mA}$ , $3 < V_{in} < 3.6$	<b>1.764</b>	1.8	<b>1.836</b>	V
Vout 2.5V	$0 < I_{out} < 750\text{mA}$ , $3 < V_{in} < 3.6$	<b>2.450</b>	2.5	<b>2.550</b>	V
Line Regulation	$I_{out} = 1\text{mA}$			<b>0.5</b>	%
$\Delta V_{out}$	$V_{out} = 1.2\text{V}$ , $I_{out} = 1\text{mA}$ , $3 < V_{in} < 3.6$			<b>6.0</b>	mV
$\Delta V_{out}$	$V_{out} = 1.5\text{V}$ , $I_{out} = 1\text{mA}$ , $3 < V_{in} < 3.6$			<b>7.5</b>	mV
$\Delta V_{out}$	$V_{out} = 1.8\text{V}$ , $I_{out} = 1\text{mA}$ , $3 < V_{in} < 3.6$			<b>9.0</b>	mV
$\Delta V_{out}$	$V_{out} = 2.5\text{V}$ , $I_{out} = 1\text{mA}$ , $3 < V_{in} < 3.6$			<b>125</b>	mV
Load Regulation				<b>0.8</b>	%
$\Delta V_{out}$	$V_{out} = 1.2\text{V}$ , $0 < I_{out} < 750\text{mA}$ , $V_{in} = 3.3$			<b>9.6</b>	mV
$\Delta V_{out}$	$V_{out} = 1.5\text{V}$ , $0 < I_{out} < 750\text{mA}$ , $V_{in} = 3.3$			<b>12.0</b>	mV
$\Delta V_{out}$	$V_{out} = 1.8\text{V}$ , $0 < I_{out} < 750\text{mA}$ , $V_{in} = 3.3$			<b>14.4</b>	mV
$\Delta V_{out}$	$V_{out} = 2.5\text{V}$ , $0 < I_{out} < 750\text{mA}$ , $V_{in} = 3.3$			<b>20.0</b>	mV
Current Limit	Short circuit	<b>0.8</b>	1	<b>1.3</b>	A
Thermal resistance Junction-to-Ambient	(No air flow)		<b>32</b>		$^\circ\text{C}/\text{W}$
Thermal resistance Junction-to-case			<b>1.8</b>		$^\circ\text{C}/\text{W}$
UVLO Levels					
Vdd Rising threshold		<b>3.9</b>	4.35	<b>4.5</b>	V
Vdd falling threshold		<b>3.8</b>	4.15	<b>4.40</b>	V
Thermal Shutdown					
Shutdown temperature			160		$^\circ\text{C}$
Thermal hysteresis			20		$^\circ\text{C}$

**Note 1:** The  $I_{out}$  range of 750mA across the four output voltages is dependent upon thermal management of the device, which includes but not limited to proper mounting of the back side of the package to the ground plane of a minimum of 4LM board, and no less than five vias under the device and a package with adequate PD capabilities.

**Note 2:** The chip has two outputs that use the same band gap reference. The band gap can be trimmed within 1%, but the offset of only one channel cancels out during trimming procedure at one output voltage. Therefore another 0.9% initial voltage error may occur between the two channels at different outputs.

## ML5401 Pinout

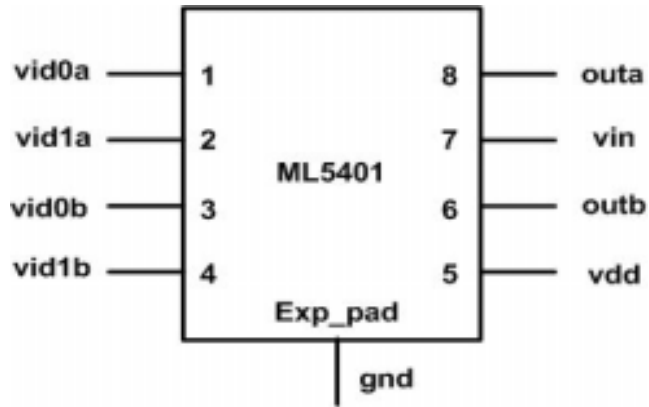


Figure 2: ML5401 pinout

## Application Note

### 1) Typical Application Circuit

Figure 3 shows the typical application circuit of ML5401. Outa is set to 1.2V and Outb to 2.5V by Vid pin setting.

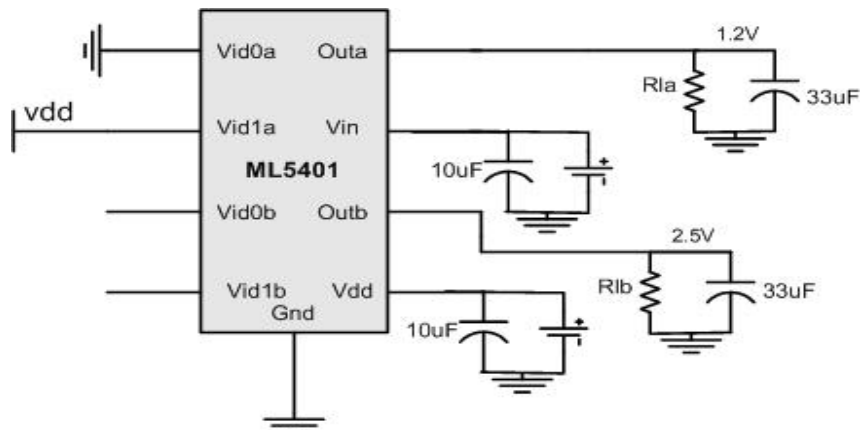


Figure 3: Typical application

### 2) Input Bypass Capacitor

An input capacitor is recommended. A 10µF on the Vdd and Vin pins is a suitable input bypass for most applications.

### 3) Output Capacitor

The output capacitor is critical in maintaining regulator stability. The minimum output capacitance required by the ML5401 is 33 $\mu$ F and it can be increased to 1000 $\mu$ F. Any increase of the output capacitance will merely improve the loop stability and transient response. Also the capacitor ESR range of capacitor is as following:

Capacitor value ( $\mu$ F)	ESR(min)	ESR(max)
33	5m	50m
220 or 330 or 1000	1m	1000m

### 4) Output Voltage selection

The ML5401 is a voltage regulator IC consisting of two voltage regulators, both of which have their own output voltage identifier pins. The ML5401 has nine different output voltage settings according to below table. In printer applications, only the boldface voltages in Table 2 are used.

Vid1	Vid0	Output Voltage
0	0	0.9V
0	1	1.0V
0	F	1.1V
<b>1</b>	<b>0</b>	<b>1.2V</b>
<b>1</b>	<b>1</b>	<b>1.5V</b>
<b>1</b>	<b>F</b>	<b>1.8V</b>
F	0	1.9V
F	1	2.0V
<b>F</b>	<b>F</b>	<b>2.5V</b>

Table 2: Output Voltage Selection Codes (F = Float, 1 = Vdd, and 0 = Gnd)

### 5) Load Regulation

The ML5401 regulates the voltage that appears between its output and ground pins. In some cases, line resistances can introduce errors to the voltage across the load. To obtain the best load regulation, a few precautions are needed.

The following figure shows a typical application with Rt1 & Rt2 as line resistances. It is obvious that the Vload is less than the Vouta by the sum of the voltage drops along the line resistances. In this case, the load regulation seen at the Rla would be degraded from the data sheet specification. To improve this, the load should be tied directly to the output terminal on the positive side and directly tied to the ground terminal on the negative side with short & wide traces.

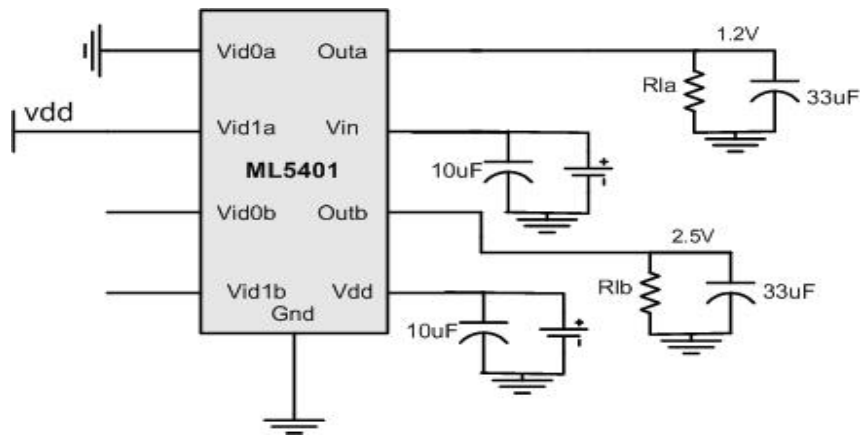


Figure 4: Load regulation precaution

**6) Thermal Management**

When an integrated circuit operates with an appreciable current, its junction temperature is elevated. It is important to quantify its thermal limits in order to achieve acceptable performance and reliability. This limit is determined by summing the individual parts consisting of a series of temperature rises from the semiconductor junction to the operating environment. A one-dimensional steady-state model of conduction heat transfer is demonstrated in Figure 5. The heat generated at the device junction flows through the die to the die attach pad, through the lead frame to the surrounding case material, to the printed circuit board, and eventually to the ambient environment. Below is a list of variables that may affect the thermal resistance.

**$\theta_{JC}$  (Component Variables)**

- Leadframe Size & Material
- No. of Conduction Pins
- Die Size
- Die Attach Material
- Molding Compound Size and Material

**$\theta_{CA}$  (Application Variables)**

- Mounting Pad Size, Material & Location
- PCB Size & Material
- Traces Length, Width & thickness
- Ambient Temperature

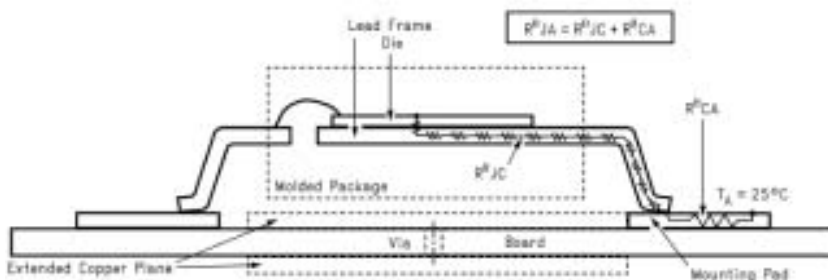


Figure 5: Cross-sectional view of Integrated Circuit Mounted on a printed circuit board. Note that the case temperature is measured at the point where the leads contact with the mounting pad surface

The ML5401 regulator has internal thermal shutdown to protect the device from over-heating. Under all possible operating conditions, the junction temperature of the ML5401 must be within the range of 0°C to 125°C. The power dissipated by the regulator,  $P_D$ , is:

$$P_D = (V_{IN} - V_{OUT}) * I_L + V_{dd} * I_{dd}, \quad \text{Thus: } T_J(\text{max}) = P_D * \theta_{JA} + T_A(\text{max})$$

Where  $T_J(\text{max})$  is the maximum allowable junction temperature (125°C), and  $T_A(\text{max})$  is the maximum ambient temperature used in the application.



For printer applications a heatsink is required since the package alone will not dissipate enough heat to satisfy these requirements ( $T_J(\max) \leq 125^\circ\text{C}$ ). This heatsink is the combination of the mounting pad directly below the chip and at least one ground plane at the bottom side of PCB. At least nine vias (12 is preferable) with 0.3-0.33mm diameter and 1.2mm pitch must be used for connecting the mounting pad to bottom plate. Using a 4-layer board according to JESD51-7 is highly recommended (Figure 6). By using this structure a  $\theta_{JA}$  of  $32^\circ\text{C/W}$  is achievable.

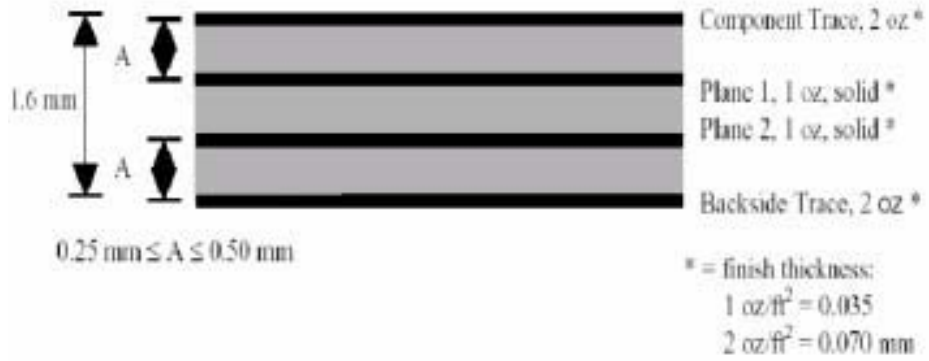


Figure 6: PCB dimensions according to JESD51-7

## ML5401 Datasheet Revision History

<b>Version</b>	<b>Changes/Revision</b>	<b>Date</b>
0.0	<ul style="list-style-type: none"> <li>▪ Initial Datasheet</li> </ul>	(02/2005)
0.1	<ul style="list-style-type: none"> <li>▪ Added Absolute Maximum rating</li> <li>▪ Vid pins interface level</li> </ul>	(03/2005)
0.2	<ul style="list-style-type: none"> <li>▪ Added Capacitor Value Table</li> <li>▪ Remove Output Voltage Characteristics at VIN=3.3V, Iout=10mA</li> <li>▪ Changed Leak Current (IIH from 40uA to 50uA, IIL from -40uA to -50uA)</li> <li>▪ Changed IDDQ ( from TYP 3.9mA to MAX 6.0mA)</li> </ul>	(06/2005)
1.0	<ul style="list-style-type: none"> <li>▪ Data sheet opening to the public</li> </ul>	(09/2005)

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