

# OKI Semiconductor MR27V25603L

 $\underline{16M-Word \times 16-Bit \text{ or } 32M-Word \times 8-Bit P2ROM}$ 

# **FEATURES**

 ·16,777,216-word × 16-bit/33,554,432-word × 8-bit electrically switchable configuration

 · 3.0 V to 3.6 V power supply
 · Access time 100 ns MAX (MR27V25603L-xxxTM) 120 ns MAX (MR27V25603L-xxxTME)
 · Operating current 35 mA MAX(5MHz)
 · Standby current 10 μA MAX

- Input/Output TTL compatible
- · Three-state output

# PACKAGES

· MR27V25603L-xxxTM, MR27V25603L-xxxTME 50-pin plastic TSOP (TSOP(2)50-P-400-0.80-K)

· MR27V25603L-xxxMB, MR27V25603L-xxxMBE 70-pin plastic SSOP (SSOP70-P-500-0.80-K)

## P2ROM ADVANCED TECHNOLOGY

P2ROM stands for Production Programmed ROM. This exclusive Oki technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing. Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

- **Short lead time**, since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
- No mask charge, since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
- No additional programming charge, unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
- Custom Marking is available at no additional charge.

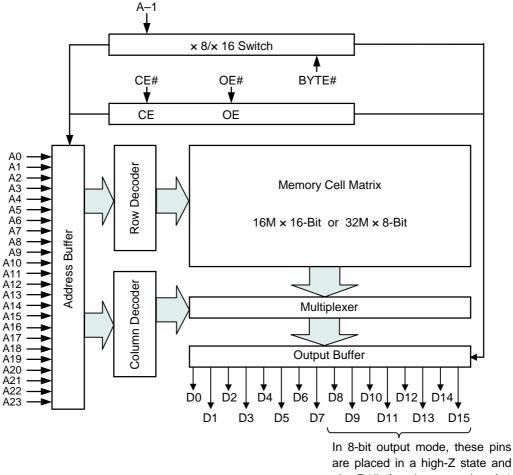
Oki, /Network Solutions for a Global Society

FEDR27V25603L-02-02

Issue Date: Jun. 8, 2004

| PIN CONFIGURATION (TOP VIEW)   |  |                   |   |  |  |  |  |
|--|--|-------------------|---|--|--|--|--|
| A11<br>A10<br>A9<br>A8<br>A7<br>A6<br>A5<br>A4<br>A3<br>A2<br>A1<br>A23<br>GND<br>BYTE#<br>A0<br>D0<br>BYTE#<br>A0<br>D1<br>D1<br>D1<br>D1<br>D1<br>D1<br>D1<br>D1<br>D1<br>D1<br>D1<br>D1<br>D1 | $\begin{array}{c} 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \\ 8 \\ 9 \\ 10 \\ 11 \\ 12 \\ 13 \\ 14 \\ 15 \\ 16 \\ 17 \\ 18 \\ 19 \\ 20 \\ 21 \\ 22 \\ 23 \\ 24 \\ 25 \\ \end{array}$                              | Sotsop<br>(Type2) | 49         48         47         46         44         43         42         41         40         93         38         37         36         55         34         33         32         33         30         29         28         27 | CE#<br>A12<br>A13<br>A14<br>A15<br>Vcc<br>A16<br>A17<br>A18<br>A19<br>A20<br>A21<br>GND<br>A22<br>NC<br>OE#<br>D15/A-1<br>D7<br>D15/A-1<br>D7<br>D15/A-1<br>D7<br>D15/A-1<br>D7<br>D14<br>D6<br>D13<br>D5<br>D12<br>D12<br>D4<br>Vcc |  |  |  |
| A23<br>NC<br>NC<br>NC<br>NC<br>GND<br>NC<br>NC   | 5     6     7     8     9     10     11     12     13     14     15     16     17     18     19     20     21     22     23     24     25     26     27     28     29     30     31     32     33     34 | 0<br>70SSOP       | 8 8 6 6 6 6 6 6 8 8 8 5 6 6 5 6 5 5 8 8 8 5 6 5 5 5 5   | CE#<br>A12<br>A13<br>A14<br>A15<br>Vcc<br>A16<br>A17<br>A18<br>A19<br>A20<br>A21<br>NC<br>NC<br>NC<br>NC<br>NC<br>NC<br>NC<br>NC<br>NC<br>NC<br>NC<br>NC<br>NC   |  |  |  |

## **BLOCK DIAGRAM**



are placed in a high-Z state and pin D15 functions as the A-1 address pin.

## **PIN DESCRIPTIONS**

| Pin name        | Functions                   |  |  |  |
|-----------------|-----------------------------|--|--|--|
| D15 / A–1       | Data output / Address input |  |  |  |
| A0 to A23       | Address inputs              |  |  |  |
| D0 to D14       | Data outputs                |  |  |  |
| CE#             | Chip enable input           |  |  |  |
| OE#             | Output enable input         |  |  |  |
| BYTE#           | Word / Byte select input    |  |  |  |
| Vcc             | Power supply voltage        |  |  |  |
| V <sub>SS</sub> | Ground                      |  |  |  |

# **FUNCTION TABLE**

| Mode             | CE# | OE# | BYTE# | Vcc         | D0 to D7         | D8 to D14        | D15/A-1 |
|------------------|-----|-----|-------|-------------|------------------|------------------|---------|
| Read (16-Bit)    | L   | L   | Н     |             |                  | D <sub>OUT</sub> |         |
| Read (8-Bit)     | L   | L   | L     | 2.0.1/      | D <sub>OUT</sub> | Hi–Z             | L/H     |
| Output disable   |     | Н   | Н     | 3.0 V       |                  |                  |         |
| Output disable L | L   | п   | L     | to<br>3.6 V |                  | Hi–Z             | *       |
| Standby          | Ц   |     | Н     | 3.0 V       | 11: 7            |                  |         |
| Standby          | Н   | *   | L     |             |                  | Hi–Z             | *       |

\*: Don't Care (H or L)

#### **ABSOLUTE MAXIMUM RATINGS**

| Parameter                        | Symbol          | Condition                   | Value                        | Unit |
|----------------------------------|-----------------|-----------------------------|------------------------------|------|
| Operating temperature under bias | Та              |                             | 0 to 70                      | °C   |
| Storage temperature              | Tstg            | —                           | -55 to 125                   | °C   |
| Input voltage                    | VI              |                             | –0.5 to V <sub>CC</sub> +0.5 | V    |
| Output voltage                   | Vo              | relative to V <sub>SS</sub> | –0.5 to $V_{CC}$ +0.5        | V    |
| Power supply voltage             | V <sub>cc</sub> |                             | –0.5 to 5                    | V    |
| Power dissipation per package    | PD              | _                           | 1.0                          | W    |

# **RECOMMENDED OPERATING CONDITIONS**

 $(Ta = 0 \text{ to } 70^{\circ}C)$ 

| Parameter                            | Symbol          | Condition               | Min.   | Тур. | Max.                  | Unit |
|--------------------------------------|-----------------|-------------------------|--------|------|-----------------------|------|
| V <sub>CC</sub> power supply voltage | V <sub>cc</sub> |                         | 3.0    | —    | 3.6                   | V    |
| Input "H" level                      | V <sub>IH</sub> | $V_{CC}$ = 3.0 to 3.6 V | 2.2    | —    | V <sub>CC</sub> +0.5* | V    |
| Input "L" level                      | VIL             |                         | -0.5** | —    | 0.6                   | V    |

Voltage is relative to V<sub>SS</sub>.

\* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.

\*\*: -1.5V(Min.) when pulse width of undershoot is less than 10ns.

## **PIN CAPACITANCE**

|           |                  |               |      | $(V_{CC} = 3.$ | $3 \text{ V}, 1a = 25^{\circ}$ | C, T = T MHZ) |
|-----------|------------------|---------------|------|----------------|--------------------------------|---------------|
| Parameter | Symbol           | Condition     | Min. | Тур.           | Max.                           | Unit          |
| Input     | C <sub>IN1</sub> | $V_1 = 0 V$   | _    | _              | 10                             |               |
| BYTE#     | C <sub>IN2</sub> | $v_1 = 0 v$   | _    | _              | 200                            | pF            |
| Output    | C <sub>OUT</sub> | $V_{O} = 0 V$ | _    | _              | 10                             |               |

 $(V_{00} - 3.3)$  Ta - 25°C f - 1 MHz

# **ELECTRICAL CHARACTERISTICS**

#### **DC Characteristics**

|   |                   |                                       |        |      | (Ta                   | = 0 to 70°C) |
|---|-------------------|---------------------------------------|--------|------|-----------------------|--------------|
| Parameter                                   | Symbol            | Condition                             | Min.   | Тур. | Max.                  | Unit         |
| Input leakage current                       | ILI               | $V_I = 0$ to $V_{CC}$                 | _      |      | 5                     | μA           |
| Output leakage current                      | I <sub>LO</sub>   | $V_{O} = 0$ to $V_{CC}$               | _      |      | 5                     | μA           |
| V <sub>CC</sub> power supply current        | I <sub>ccsc</sub> | $CE\# = V_{CC}$                       | _      |      | 10                    | μA           |
| (Standby)                                   | ICCST             | CE# = V <sub>IH</sub>                 | _      |      | 1                     | mA           |
| V <sub>CC</sub> power supply current (Read) | I <sub>CCA</sub>  | $CE\# = V_{IL}, OE\# = V_{IH}$ f=5MHz |        |      | 35                    | mA           |
| Input "H" level                             | V <sub>IH</sub>   | —                                     | 2.2    | _    | V <sub>CC</sub> +0.5* | V            |
| Input "L" level                             | V <sub>IL</sub>   | —                                     | -0.5** |      | 0.6                   | V            |
| Output "H" level                            | V <sub>OH</sub>   | I <sub>ОН</sub> = –1 mA               | 2.4    |      | _                     | V            |
| Output "L" level                            | V <sub>OL</sub>   | I <sub>OL</sub> = 2 mA                | —      |      | 0.4                   | V            |

Voltage is relative to V<sub>SS</sub>.

\* : Vcc+1.5V(Max.) when pulse width of overshoot is less than 10ns.

\*\* : -1.5V(Min.) when pulse width of undershoot is less than 10ns.

#### **AC Characteristics**

| ( | Vcc = | 3.0 | to 3 | 6 V  | Ta = | 0 to | 70°C) |
|---|-------|-----|------|------|------|------|-------|
|   | vuu – | 0.0 | 10 0 | .0 v | 1a – | 0.0  | 100)  |

| Parameter           | Symbol           | Condition              | Min.  | Max.  | Unit |  |
|---------------------|------------------|------------------------|-------|-------|------|--|
| Address such time   |                  |                        | 100*  |       |      |  |
| Address cycle time  | t <sub>C</sub>   | —                      | 120** |       | ns   |  |
|                     |                  |                        |       | 100*  |      |  |
| Address access time | t <sub>ACC</sub> | $CE\# = OE\# = V_{IL}$ | _     | 120** | ns   |  |
| 05"                 |                  | 05" )/                 |       | 100*  |      |  |
| CE# access time     | t <sub>CE</sub>  | $OE\# = V_{IL}$        | _     | 120** | ns   |  |
| OE# access time     | t <sub>OE</sub>  | $CE\# = V_{IL}$        | —     | 30    | ns   |  |
| Output disable time | t <sub>CHZ</sub> | $OE\# = V_{IL}$        | 0     | 20    | ns   |  |
| Output disable time | t <sub>OHZ</sub> | $CE\# = V_{IL}$        | 0     | 20    | ns   |  |
| Output hold time    | t <sub>OH</sub>  | $CE\# = OE\# = V_{IL}$ | 0     |       | ns   |  |

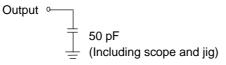
\* : MR27V25603L-xxxTM, MR27V25603L-xxxMB

\*\* : MR27V25603L-xxxTME, MR27V25603L-xxxMBE

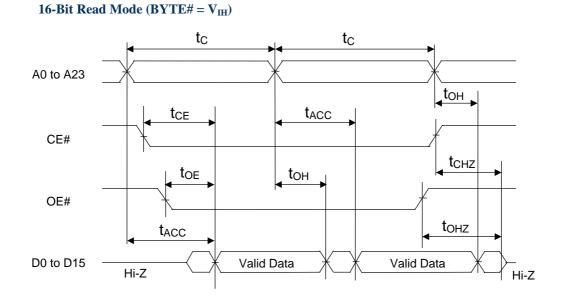
#### Measurement conditions

| Input signal level            | -0 V/3 V |
|-------------------------------|----------|
| Input timing reference level  |          |
| Output load                   |          |
| Output timing reference level | 1/2Vcc   |

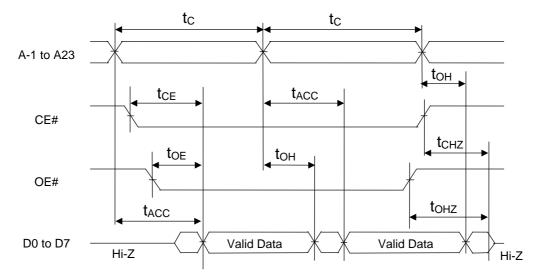
Output load



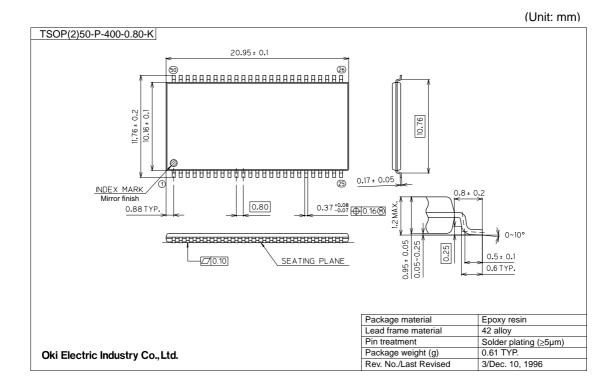
## TIMING CHART (READ CYCLE)



8-Bit Read Mode (BYTE# = V<sub>IL</sub>)



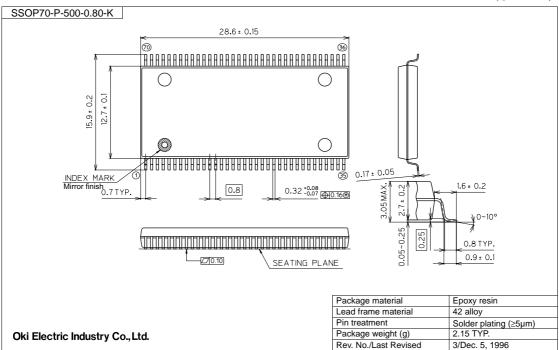
# PACKAGE DIMENSIONS



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).



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(Unit: mm)

# **REVISION HISTORY**

| Document            |              | Page                |                    |                                 |  |
|---------------------|--------------|---------------------|--------------------|---------------------------------|--|
| No.                 | Date         | Previous<br>Edition | Current<br>Edition | Description                     |  |
| FEDR27V25603L-02-01 | Apr. 1, 2004 | -                   | -                  | Final edition 1                 |  |
| FEDR27V25603L-02-02 | Jun. 8, 2004 | 3                   | 3                  | Change C <sub>IN1</sub> to 10pF |  |

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