OKI Semiconductor

PEDL60842-02
Issue Date: Oct. 31, 2003

ML60842

Preliminary

USB OTG Controller IC

1. GENERAL DESCRIPTION

The ML60842 is a single-chip LSI that can implement a dual-role device complying with Universal Serial Bus (USB) 2.0 and On-The-Go (OTG) Supplement Revision 1.0a

The common block can perform the Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) control, and can switch between the host controller function and the peripheral controller function.

The host controller block and the peripheral controller block support four data transfer modes; control transfer, interrupt transfer, bulk transfer, and isochronous transfer.

The host controller block supports the 1-port USB transceiver function. It can also be connected to a USB transceiver LSI. Moreover, it complies with OpenHCI Specification 1.0a.

The peripheral controller block complies with the ML60852A specification. To use it as a peripheral controller, refer to the "ML60825A Data Sheet" and the "ML60852A USB Device Controller Application Manual" in addition to this manual.

2. FEATURES

- Complies with USB2.0 and On-The-Go (OTG) Supplement Revision 1.0a

<Common block>

- Can control Session Request Protocol (SRP) and Host Negotiation Protocol (HNP).
  - · VBUS pulsing control
  - · Data-line pulsing control
  - · VBUS pulsing detection control
- Can switch between the host and the peripheral.
- Supports the power down function.
- Can switch between 16- and 8-bit buses.
- Supports address/data multiplexing
- Can switch between little endian and big endian.
- Occupies an 8-Kbyte space from 0000h to 1FFFh (register: 0000h to 0FFFh, embedded RAM: 1000h to 1FFFh)
- Supports the DMA function.
  - · Host mode supports 1 channel and the peripheral mode supports 2 channels.
  - · Supports the following DMA transfer modes.
    1) Dual address mode
    2) Transfer size per DREQ: 16 bits/8 bits
       (The same specification as the transfer size of the DMA controller on the microcontroller side is required.)

<Host controller block>

- Complies with OpenHCI (Open Host Controller Interface) 1.0a.
- Supports four data transfer types (control transfer, bulk transfer, interrupt transfer, and isochronous transfer)
- Reduces software load by using the DMA slave function (1 CH) and can make PIO transfer (except isochronous transfer).
- Supports one USB port [compatible with full-speed (12 Mbps)/low-speed (1.5 Mbps)]
- Supports the SOF generation and CRC5/16 generation functions.

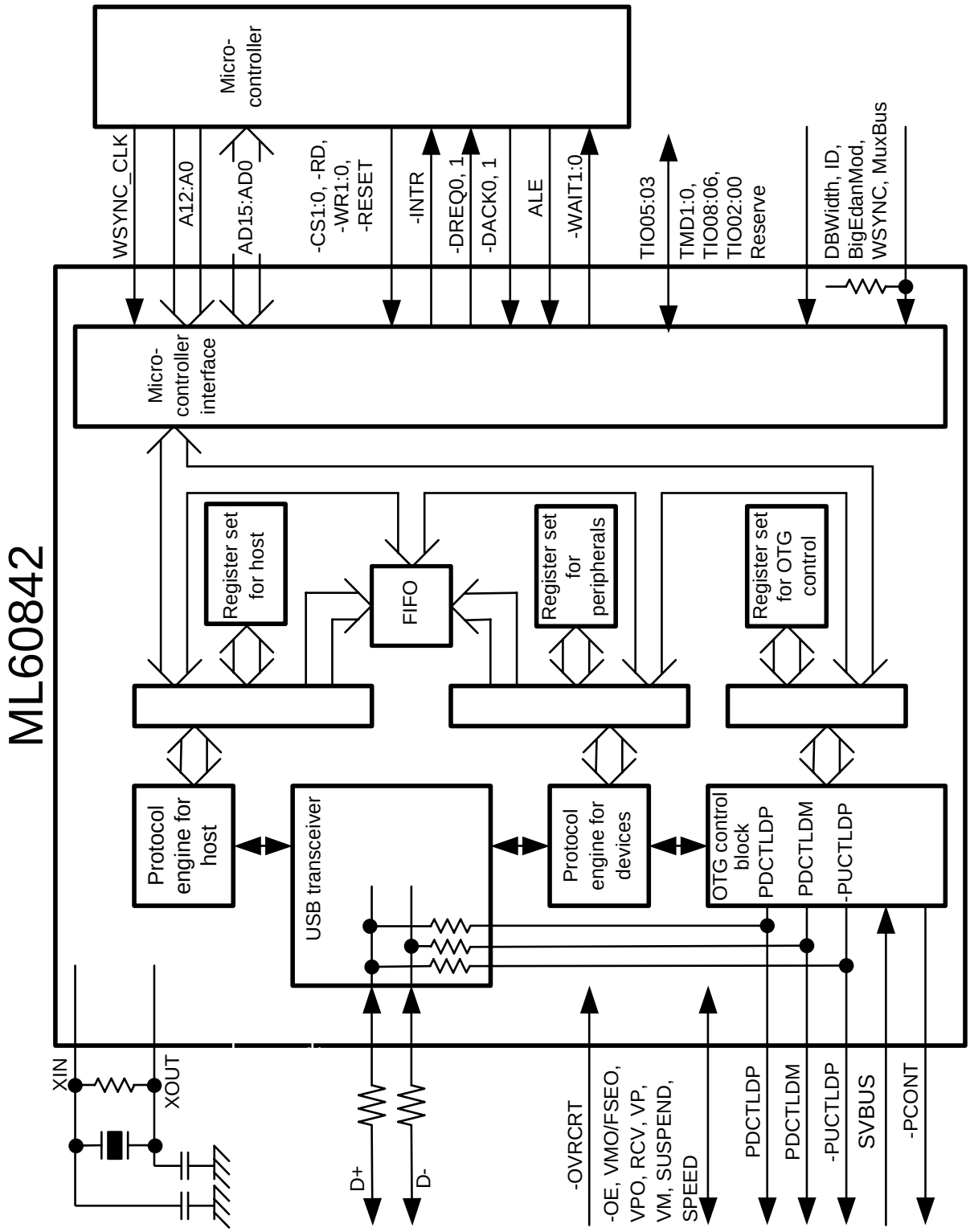
<Peripheral controller block>

- Supports full-speed (12 Mbps)
- Supports four data transfer types (control transfer, bulk transfer, interrupt transfer, and isochronous transfer)
- Endpoints (EP): 5 or 6
  - · Control EP : 1
  - · Bulk/interrupt EP : 3
  - · Isochronous/bulk/interrupt EP : 1 or 2
- Built-in FIFO for data storage
- Double-sided FIFO configuration for EP1, EP2, EP4, and EP5
- DMA slave function (2 CH, EP1, EP2, EP4, EP5 supported), PIO transfer possible
- Supports the suspend and wakeup functions

<Others>

- Can connect the USB port with a USB transceiver LSI
- 48 MHz oscillator
- 3.3 V single power supply
- 100-pin TQFP, 120-pin BGA, 96-pin WCSP

3. BLOCK DIAGRAM



4. PIN CONNECTIONS

The following shows the pin placement of the ML60842.

<ML60842 pin placement>

Pin No.	I/O type	Signal name	Pin No.	I/O type	Signal name	Pin No.	I/O type	Signal name
1	*1	-RESET	35	*4	A11	69	*3	AD1
2	*4	TIO07	36	*4	A10	70	*3	AD0
3	*4	TIO06	37	*4	A9	71	—	DVDD
4	*3	TIO05	38	*4	A8	72	—	DGND
5	*5	VPO	39	*4	A7	73	*4	-CS1
6	*5	VMO/FSEO	40	*4	A6	74	*4	-CS0
7	*5	-OE	41	*4	A5	75	*4	ALE
8	*5	SPEED	42	*4	A4	76	*4	-WR1
9	*4	VP	43	*4	A3	77	*4	-WR0
10	*4	VM	44	*4	A2	78	*4	-RD
11	*4	RCV	45	*4	A1	79	*4	TIO01
12	*5	SUSPEND	46	*4	A0	80	*6	-WAIT1
13	*2	ID	47	*4	TMD1	81	*6	-WAIT0
14	*5	-PCONT	48	*4	TMD0	82	*5	-INTR
15	*5	-PUCTLDP	49	*3	TIO03	83	*5	-DREQ0
16	*5	PDCTLDP	50	*4	TIO02	84	*4	-DACK0
17	*5	PDCTLDM	51	—	DVDD	85	*5	-DREQ1
18	—	DVDD	52	—	DGND	86	*4	-DACK1
19	*4	Reserve	53	*3	AD15	87	—	DVDD
20	*4	Reserve	54	*3	AD14	88	—	XIN
21	—	DGND	55	*3	AD13	89	—	XOUT
22	—	A1VDD	56	*3	AD12	90	—	DGND
23	—	D+	57	*3	AD11	91	*4	WSYNC_CLK
24	—	D-	58	*3	AD10	92	*4	TIO00
25	—	A1GND	59	*3	AD9	93	*2	BigEdanMod
26	—	SVBUS	60	*3	AD8	94	*2	DBWidth
27	—	A2GND	61	—	DVDD	95	*2	MuxBus
28	—	A2VDD	62	—	DGND	96	*2	WSYNC
29	—	TIO08	63	*3	AD7	97	—	NC
30	—	DVDD	64	*3	AD6	98	—	NC
31	—	DGND	65	*3	AD5	99	—	NC
32	*4	-OVRCRT	66	*3	AD4	100	—	NC
33	*3	TIO04	67	*3	AD3			
34	*4	A12	68	*3	AD2			

[Note] I/O types
*1: TTL Schmitt Input Buffer with 4X Drive (SITS4A)
*2: TTL Input Buffer with 4X Drive/50K Pull-up (SIT4U)
*3: I/O Buffer with TTL Input/4 mA Output (SBT4)
*4: TTL Input Buffer with 4X Drive (SIT4A)
*5: Push Pull Output Buffer with 4 mA Drive (SOP4A)
*6: Tri-State Output Buffer with 4 mA Drive (SOT4A)

5. PIN DESCRIPTIONS

The following tables list the descriptions of pins used in the ML60842.
Pin names prefixed with "-" indicate "active low" pins and pin names without "-" indicate "active high" pins.

The "initial state" column shows the state of each pin under the conditions where resetting is enabled (-RESET = "L") and a stable 48 MHz clock is supplied.
It means that if a signal at the level ("H," "L" or "open-circuited") specified in the initial state column is input to a pin indicating [Input] in the initial state column, then a signal at the level ("H," "L" or "undefined") specified in the initial state column is output to a pin indicating [Output] in the initial state column, or the pin is placed in the Hi-Z (high impedance) state.

5.1 Microcontroller Interface Signals

Pin name	Number of pins	I/O	Description	Initial state
AD15:AD8	8	I/O	I/O pins for address/data bus Note that AD15 to AD13 are ignored at address input. If the MuxBus pin is "H," these pins are configured as the I/O pins for address/data bus (multiplex bus). Input is fixed when DBWidth = 8-bit mode. If not used, pull-up or pull-down is required. If the MuxBus pin is "L," these pins are configured as the I/O pins for data bus (separate bus). Input is fixed when DBWidth = 8-bit mode. If not used, pull-up or pull-down is required.	[Input] "H" or "L"
AD7:AD0	8	I/O	I/O pins for address/data bus If the MuxBus pin is "H," these pins are configured as the I/O pins for address/data bus (multiplex bus). If the MuxBus pin is "L," these pins are configured as the I/O pins for data bus (separate bus).	[Input] "H" or "L"
A12:A0	13	I	Input pins for address bus (for accessing internal register and embedded 4 KB RAM) If the MuxBus pin is "H" (multiplex bus), these pins are disabled. Fix the input level at "H" or "L." If the MuxBus pin is "L" (separate bus), these pins are enabled.	[Input] "H" or "L"
-CS1:0	2	I	Chip select signal input pins from the microcontroller If both the -CS1 and -CS0 pins are "L," access to the ML60842 is enabled.	[Input] "H"
ALE	1	I	Address latch enable signal input pin from the microcontroller This pin is enabled only if the MuxBus pin is "H" (multiplex bus). If the MuxBus pin is "L" (separate bus), fix the pin at "L."	[Input] "L"
-WR1:-WR0	2	I	Write signal input pins from the microcontroller When -WR1 is active, the data of the higher bytes (AD15:AD8) is written into the ML60842. When -WR0 is active, the data of the lower bytes (AD7:AD0) is written into the ML60842. When DBWidth = 8-bit mode and -WR1 is not used, fix the pin at "H."	[Input] "H"
-RD	1	I	Read signal input pin from the microcontroller	[Input] "H"

Pin name	Number of pins	I/O	Description	Initial state
-DREQ0(*)	1	O	Pin for outputting a request to the DMA master (used when the host/peripheral are in operation)	[Output] "H"
-DACK0(*)	1	I	Pin for inputting a DMA request reception response from the DMA master (used when the host/peripheral are in operation) This input negates the -DREQ0 signal. (This is not an input to indicate the execution of a DMA cycle.) The DMA cycle is executed by an access to the request generating source address. If not used, fix the input level at an inactive level.	[Input] "H"
-DREQ1(*)	1	O	Pin for outputting a request to the DMA master (used when the peripherals are in operation)	[Output] "H"
-DACK1(*)	1	I	Pin for inputting a DMA request reception response from the DMA master (used when the peripherals are in operation) This input negates the -DREQ1 signal. (This is not an input to indicate the execution of a DMA cycle.) The DMA cycle is executed by an access to the request generating source address. If not used, fix the input level at an inactive level.	[Input] "H"
-WAIT1	1	O	Pin for outputting a wait request to the microcontroller If both the -CS1 and -CS0 pins are "L," the following operation is performed: If the WSYNC pin is "H," the assert operation performs output asynchronous with WSYNC_CLK while the negate operation performs output synchronous with WSYNC_CLK. Set the microcontroller in such a way that it samples at the rising edge of the WSYNC_CLK signal. If the WSYNC pin is "L," both assert and negate operations perform asynchronous output. If either the -CS1 or -CS0 pin, or both pins are "H," this pin is placed in a Hi-Z state. Pull this pin up to the "H" level regardless of whether or not it is used.	Hi-Z
-WAIT0	1	O	Pin for outputting a wait request to the microcontroller If both the -CS1 and -CS0 pins are "L," the following operation is performed: If the WSYNC pin is "H," both the assert and negate operations perform output synchronous with WSYNC_CLK. Set the microcontroller in such a way that it samples at the rising edge of the WSYNC_CLK signal. If the WSYNC pin is "L," this pin is fixed at "H" output. If either the -CS1 or -CS0 pin, or both pins are "H," this pin is placed in a Hi-Z state. Pull this pin up to the "H" level regardless of whether or not it is used.	Hi-Z
-INTR(*)	1	O	Pin for outputting a wait request to the microcontroller	[Output] "H"

(*): The active level can be changed via register setting.

5.2 USB Interface Signals

Pin name	Number of pins	I/O	Description	Initial state
-PCONT	1	O	Output pin for USB interface power supply control (ON/OFF) "L": ON, "H": OFF	[Output] "H"
SVBUS	1	I	Pin for inputting the voltage level sense of the USB interface power supply (VBUS signal) The voltage supplied to the VBUS is detected at the following two types of levels via register setting. (For more information, see Section 6.1.4, "OTGCtl Register" and Section 6.1.5, "OTGIntStt Register.") (1) 4.0 V to 4.5 V < VBUS (2) 0.8 V to 2.0 V < VBUS Also, a pull-up/pull-down resistor is connected to this pin via a switch. VBUS pulsing is executed by setting this switch to ON/OFF via register setting. (For more information, see Section 6.1.4, "OTGCtl Register" and Section 7.1, "Session Request Protocol (SRP).") *If no power is supplied to the ML60842, it is necessary to control with an external switch in such a way that the VBUS signal will not be supplied to this pin.*	[Input] "H" or "L"
-OVRCRT	1	I	Input pin for notifying a USB interface power supply abnormality (overcurrent, etc.) when in host mode "L": Abnormal, "H": Normal	[Input] "H"
D+, D-	2	I/O	USB interface I/O pin If an external USB transceiver is used (EXBUFENB bit of ChipConfig register = "1"), fix the input level at "H" or "L."	[Input] "H" or "L," or "open-circuited"
-PUCTLDP	1	O	Pin for controlling the pull-up resistor of an external USB transceiver If an external USB transceiver is used (EXBUFENB bit of ChipConfig register = "1"), this pin is enabled. This pin is used for the pull-up control of the USB interface D+ I/O pin for an external USB transceiver. "L": Enables pull-up control, "H": Disables pull-up control	[Output] "H"
PDCTLDP	1	O	Pin for controlling the pull-down resistor of an external USB transceiver If an external USB transceiver is used (EXBUFENB bit of ChipConfig register = "1"), this pin is enabled. This pin is used for the pull-up control of the USB interface D+ I/O pin for an external USB transceiver. "L": Disables pull-down control, "H": Enables pull-down control	[Output] "L"
PDCTLDM	1	O	Pin for controlling the pull-down resistor of an external USB transceiver If an external USB transceiver is used (EXBUFENB bit of ChipConfig register = "1"), this pin is enabled. This pin is used for the pull-up control of the USB interface D- I/O pin for an external USB transceiver. "L": Disables pull-down control, "H": Enables pull-down control	[Output] "L"

Pin name	Number of pins	I/O	Description	Initial state
-OE(**)	1	O	Output pin for switching inputs of an external USB transceiver If an external USB transceiver is used (EXBUFENB bit of ChipConfig register = "1"), this pin is enabled. "L": Transmit mode (ML60842 → USB), "H": Receive mode (USB → ML60842)	[Output] "H"
VPO(**), VMO/FSEO(**)	2	O	Output pin to an external USB transceiver If an external USB transceiver is used (EXBUFENB bit of ChipConfig register = "1"), this pin is enabled. The ML60842 outputs the states shown in the "Result" column below using a combination of the TRMODE bit of the ChipConfig register, VPO and VMO/FSEO: MODE VPO VMO/FSEO Result 0 0 0 Logic "0" 0 0 1 SE0# 0 1 0 Logic "1" 0 1 1 SE0# 1 0 0 SE0# 1 0 1 Logic "0" 1 1 0 Logic "1" 1 1 1 Illegal Code	[Output] ·VPO: Undefined ·VMO/FSE0: Undefined
RCV(**)	1	I	Input pin for data received from an external USB transceiver If an external USB transceiver is used (EXBUFENB bit of ChipConfig register = "1"), this pin is enabled. If not used, fix the input level at "H" or "L."	[Input] "H" or "L"
VP(**), VM(**)	2	I	Input pin from an external USB transceiver If an external USB transceiver is used (EXBUFENB bit of ChipConfig register = "1"), this pin is enabled. The ML60842 makes judgment and operates according to the states shown in the "Result" column below using a combination of these two signal lines: VP VM Result 0 0 SE0# 0 1 Low Speed 1 0 Full Speed 1 1 Error If not used, fix the input level at "H" or "L."	[Input] "H" or "L"
SUSPEND(**)	1	O	Output pin for instructing an external USB transceiver to be in the suspend state when a USB interface is not used. If an external USB transceiver is used (EXBUFENB bit of ChipConfig register = "1"), this pin is enabled. "L": Specifies not to be in the suspend state. "H": Specifies to be in the suspend state.	[Output] "H"
SPEED(**)	1	O	Output pin for instructing an external USB transceiver as to the USB interface speed. If an external USB transceiver is used (EXBUFENB bit of ChipConfig register = "1"), this pin is enabled. "L": Low speed, "H": Full speed	[Output] "H"

(**): A signal line for connecting the USB port shared by the host and peripheral with an external USB transceiver.

5.3 Other Signals

Pin name	Number of pins	I/O	Description	Initial state
-RESET	1	I	Reset input pin	[Input] "L"
XIN, XOUT	2	—	I/O pin for an external crystal oscillator	[Input] 48 MHz clock supply
WSYNC_CLK	1	I	Synchronous clock input pin for making the -WAIT1:0 signals synchronous outputs Connect the bus clock of the microcontroller. The maximum frequency is TBD (33 MHz). This pin is enabled only if the WSYNC pin is "H." If the WSYNC pin is "L," fix this pin at "L."	[Input] "L"
BigEdanMod	1	I	Input pin for specifying the conversion of big endian data of microcontroller interface "L": Big endian mode 1 "H": Big endian mode 0 For more information about the data conversion operations of big endian modes 1 and 0, see Section 7.5, "Data Alignment (Endian Conversion)."	[Input] "H" or "L"
DBWidth	1	I	Input pin for selecting a data bus width DBWidth Data bus width L 16 bits H 8 bits The state of this pin is loaded into the ML60842 during resetting. If the state of this pin changes during resetting, correct operation cannot be guaranteed. Even if the state of the pin is changed after resetting, the state of this pin does not affect the operations of the ML60842.	[Input] "H" or "L"
MuxBus	1	I	Input pin for specifying the address/data bus of a microcontroller interface "H": Uses AD15:AD0 as the address/data bus (multiplex bus) "L": Uses A12:A0 as the address bus, and uses AD15:AD0 as the data bus (separate bus) The state of this pin is loaded into the ML60842 during resetting. If the state of this pin changes during resetting, correct operation cannot be guaranteed. Even if the state of the pin is changed after resetting, the state of this pin does not affect the operations of the ML60842.	[Input] "H" or "L"
WSYNC	1	I	Input pin for specifying the output specification of the -WAIT0/1 signals "H": Outputs the -WAIT0/1 signals synchronously with the WSYNC_CLK signal. "L": Outputs the -WAIT1 signal asynchronously with the WSYNC_CLK signal, and disables the -WAIT0 signal output. The state of this pin is loaded into the ML60842 during resetting. If the state of this pin changes during resetting, correct operation cannot be guaranteed. Even if the state of the pin is changed after resetting, the state of this pin does not affect the operations of the ML60842.	[Input] "H" or "L"

Pin name	Number of pins	I/O	Description	Initial state
ID	1	I	Input pin for identifying device A/B This pin has an internal 50 kΩ pull-up resistor. The following function is set depending on the level of this signal when hardware is reset: "L": Device A (or normal host function) "H": Device B (or normal peripheral function) Note that the host and peripheral functions are not switched even if the state of this pin changes after resetting hardware (if the ML60842 is used as a USB On-The-Go device, function switching is controlled by the MODE bit of the HostPeriSel register after resetting hardware). Set this input pin to "L" if the LM60842 is used as a normal host without using the functions of a USB On-The-Go device. Set this input pin to "H" if the ML60842 is used as a normal peripheral device.	[Input] "H" or "L"
TMD1:0	2	I	Input pins for setting test mode (usually connected to GND).	[Input] "L"
TIO07:06, 02:00	5	I	I/O pins for test (usually connected to GND)	[Input] "L"
TIO05:03	3	I/O	I/O pins for testing (usually connected to GND)	[Input] "L"
TIO8	1	I	I/O pin for testing (usually open-circuited)	[Input] "Open-circuited"
A1VDD	1	—	VDD for analog 1	VDD connection
A1GND	1	—	GND for analog 1	GND connection
A2VDD	1	—	VDD for analog 2	VDD connection
A2GND	1	—	GND for analog 2	GND connection
DVDD	6	—	VDD for digital	VDD connection
DGND	6	—	GND for digital	GND connection
Reserve	2	I	Reserved pins (usually connected to GND)	[Input] "L"
NC	4	—	Unconnected pins	—
Total	100			—

6. REGISTER DESCRIPTIONS

The registers of the ML60842 can largely be classified into common block registers, host controller block registers, and peripheral controller block registers.
The common block registers are used to control the OTG functions (Session Request Protocol and Host Negotiation Protocol) as well as to set the basic specifications (polarity of pins, mode of the external USB transceiver, etc.) of the ML60842.
The host controller block registers are based on registers conforming to the OHCI (Open Host Controller Interface).
The peripheral controller block registers are based on the ML60852A specification. The setup registers, in which setup data transferred from the host via the control pipe is stored, are also mapped to the addresses of these register files. Registers containing information about data phase in control transfer and transmit/receive data in other transfer modes are also mapped to the addresses of these register files.

The general mapping of addresses of each category is as follows:

Category	Offset	Remarks
Common block	000h-0FFh	
Host controller (register) block	100h-2FFh	Including the OHCI operation register
Peripheral controller block	300h-4FFh	
Host controller (memory) block	1000h-1FFFh	Embedded 4 KB RAM

The mapping of each register is described in Section 6.1.
Note that "R," "W" and "R/W" are defined as follows in the subsequent descriptions of the registers.

- R: Only read operations are valid. Unless specifically noted in the description of each register, writing "1" or "0" to the relevant register does not affect operations.
- W: Only write operations are valid. Unless specifically noted in the description of each register, undefined data is read if the relevant register is read.
- R/W: Both read and write operations are valid.

Correct operation cannot be guaranteed if addresses not defined are accessed. Therefore, make sure to avoid accessing such addresses.
Also, correct operation cannot be guaranteed if "1" is written to fields not defined in the registers defined below. Write "0" to fields not defined if it is necessary to write to other fields.
Moreover, if any of the peripheral controller block registers (registers at 200h to 3FFh) are accessed while the ML60842 is in operation as a host controller, or if any of the host controller block registers (registers at 100h to 2FFh) or host controller block memory (memory at 1000h to 1FFFh) is accessed while the ML60842 is in operation as a peripheral device, correct operation of the function currently running (the host function in the case of the former and the peripheral function in the case of the latter) cannot be guaranteed. Perform control so as to avoid such accesses.
"Don't Care" and "X" mean the following:

- When writing: Writing "0" or "1" does not affect the operations of the ML60842.
- When reading: Undefined data is read.

6.1 Types and Configuration of Common Registers

Offset	Symbol	Name
000h	HostPeriSel	Host/peripheral switching register
004h	ChipConfig	Chip configuration register
008h	Endian	Endian register
010h	OTGCtl	On-The-Go control register
014h	OTGIntStt	On-The-Go interrupt status register
018h	OTGIntMask	On-The-Go interrupt mask register
01Ch	RstClkCtl	Reset clock control register

Except for the CRST, HRST, and PRST bits of the RrsClkCtl register, the common registers listed above can be accessed even if the clock is stopped (the CLKSTOP or XSTOP bit of the RstClkCtl register is "1").
Note that the -WAIT1:0 signals are not asserted for access while the power is down.

6.1.1 HostPeriSel Register (000h)

Bits	Symbol	Description	Reset	R/W
31:16	CHIPREV	Indicates the chip revision.	FE01	R
15:03	—	Don't care	X	X
02	HWSW MODE	Indicates whether the host/peripheral function will be specified by hardware control (by the ID pin) or software control (by the MODE bit). 0: No writing to the MODE bit 1: Writing to the MODE bit	0b	R
01	BUSY	Indicates that the internal processing of the ML60842 is being executed when switching the MODE bit setting value or resetting. 0: Internal processing is not being executed. 1: Internal processing is being executed.	0b	R
00	MODE	Specifies the host or peripheral function. Indicates the currently active function (Host/Peripheral) regardless of the state of the ID pin. 0: HOST 1: Peripheral	Note	R/W

Note: Determined by the state of the ID pin.

[Description]

The host and peripheral functions can be switched by writing to the MODE bit. For example, the ML60842 can be operated as a host by writing "0000h" to this register.

If the setting value of the MODE bit is changed (a different value is written), the ML60842 resets both of its internal host and peripheral bocks. The BUSY bit is set to "1" during reset processing and to "0" when the reset processing completes and the ML60842 becomes operable.

If the same value is written to the MODE bit, the HWSWMODE bit is set to "1" but no other operations are affected (the host and peripheral blocks inside the ML60842 are not reset and the BUSY bit is not set to "1" either). Therefore, the microcontroller must execute initialization processing on the host or peripheral block after a setting change (writing a different value). Start initialization processing after the BUSY bit has been set to "0." For more information about the timing to start initialization processing, see Section 7.4, "Host/Peripheral Setting Control."

Note that the state of the block not selected by this bit (for example, the peripheral block when this bit is "0" and the host block when this bit is "1") is set as being reset.

The BUSY bit indicates whether or not the ML60842 is executing internal processing. If the ML60842 is accessed (excluding the read operation of this bit) while this bit is "1" (internal processing is being executed), correct operation cannot be guaranteed.

The execution of internal processing reflected in this bit specifically occurs in the following cases:

- When switching between the host and peripheral operating modes by setting the MODE bit (writing a different value to the MODE bit)
- When the hardware reset (-RESET) signal is input
- When "1" is written to the CREST bit of the RstClkCtl register
- When "1" is written to the HREST bit of the RstClkCtl register
- When "1" is written to the PREST bit of the RstClkCtl register

6.1.2 ChipConfig Register (004h)

Bits	Symbol	Description	Reset	R/W
31:08	—	Don't care	X	X
07	TRMODE	Sets the mode that has been set in an external USB transceiver. 0: MODE0 1: MODE1 Be sure to specify the same mode as that of the mode pin of the external USB transceiver. By setting this bit, the ML60842 operates as explained in the descriptions of the VPO, VMO/FSEO pins in Section 5.2, "USB Interface Signals."	0b	R/W
06:04	DREQITVL	Sets the minimum interval time from the negate to assert operations of the DREQ signal. Minimum interval time / Bit 10 / Bit 09 / Bit 08 (21 × 1) ns 0 0 0 (21 × 2) ns 0 0 1 (21 × 3) ns 0 1 0 (21 × 4) ns 0 1 1 (21 × 5) ns 1 0 0 (21 × 6) ns 1 0 1 (21 × 7) ns 1 1 0 (21 × 8) ns 1 1 1	111b	R/W
03	EXBUFENB	Sets whether or not to use an external USB transceiver. 0: Does not use an external USB transceiver (uses the embedded USB transceiver). 1: Uses an external USB transceiver (does not use the embedded USB transceiver).	0b	R/W
02	POLINTR	Sets the polarity of the INTR signal. 0: Active low 1: Active high	0b	R/W
01	POLDACK	Sets the polarity of the DACK signal. 0: Active Low 1: Active High	0b	R/W
00	POLDREQ	Sets the polarity of the DREQ signal. 0: Active Low 1: Active High	0b	R/W

[Description]
In the TRMODE bit, set the same mode as that of the MODE pin of an external USB transceiver for the purpose of conforming the operation of the external USB transceiver to the operation of the ML60842.
The POLINTR, POLDACK, and POLDREQ bits set the active level of the corresponding pins (-INTR, DACK0/1, and DREQ0/1).
The active level becomes "active low" if "0" is set and "active high" if "1" is set.
There are two DACK0/1 and DREQ0/1 pins each for every DMA channel, and both pins are set to the same active level when this ChipConfig register is set.

6.1.3 Endian Register (008h)

Bits	Symbol	Description	Reset	R/W
31:25	—	Don't care	X	X
24	ENDIAN3	Sets the data bus specification (little endian/big endian) of the microcontroller. 0: Little endian 1: Big endian	0b	R/W
23:17	—	Don't care	X	X
16	ENDIAN2	Sets the data bus specification (little endian/big endian) of the microcontroller. 0: Little endian 1: Big endian	0b	R/W
15:09	—	Don't care	X	X
08	ENDIAN1	Sets the data bus specification (little endian/big endian) of the microcontroller. 0: Little endian 1: Big endian	0b	R/W
07:01	—	Don't care	X	X
00	ENDIAN0	Sets the data bus specification (little endian/big endian) of the microcontroller. 0: Little endian 1: Big endian	0b	R/W

[Description]
The endian register can be used to set the operation of the ML60842 according to the data bus specification (little endian/big endian) of the microcontroller.
When this register is read, the same value is read from all of the ENDIAN3, 2, 1, and 0 bits. All of the ENDIAN3, 2, 1, and 0 bits are set to "0" if the ML60821 is set to little endian and to "1" if the ML60842 is set to big endian.
In order to change the setting from little endian to big endian, it is necessary to write "1" to all of the ENDIAN3, 2, 1, and 0 bits. In order to change the setting from big endian to little endian, it is necessary to write "0" to all of the ENDIAN3, 2, 1, and 0 bits.
For more information about conversion operations when the ML60842 is set to little endian or big endian, see Section 7.5, "Data Alignment (Endian Conversion)."

6.1.4 OTGCtl Register (010h)

Bits	Symbol	Description	Reset	R/W
31:15	—	Don't care	X	X
14	BSE0SRPDETENB	Enables a timer used to detect that the SE0 state continues at least 2 ms. 0: Disable 1: Enable If the CLKSTOP bit of the RstClkCtl register is set to "1," counting of 2 ms is not executed even if this bit is set to "1" (timer enable). In order to fully enable this function, it is necessary to set the CLKSTOP bit of the RstClkCtl register to "0."	0b	R/W
13	USBRCVENB	Enables the receiver unit of the embedded USB transceiver when the EXTBUFENB bit of the ChipConfig register is "0." 0: Disable 1: Enable	1b	R/W
12	ABSESSVLDENB	Enables the AB_SESS_VALID comparator. 0: Disable 1: Enable If this bit is changed from "1" to "0" while the voltage applied to the SVBUS pin is higher than the detected voltage (the ABSESSVLDST bit of the OTGIntStt register is "1"), the ABSESSVLDST bit of the OTGIntStt register is set to "0" and an ABSESSVLDCHG interrupt occurs.	0b	R/W
11	AVBUSVLDENB	Enables the A_VBUS_VALID comparator. 0: Disable 1: Enable If this bit is changed while the CLKSTOP bit of the RstClkCtl register is "1," the value of this bit does not go valid until the CLKSTOP bit of the RstClkCtl register is set to "0." For example, a comparison is not executed even if "1" is written to this bit while the CLKSTOP bit of the RstClkCtl register is "1." Instead, a comparison starts as soon as the value of the CLKSTOP bit of the RstClkCtl register is set to "0." In order to fully enable this function, it is necessary to set the CLKSTOP bit of the RstClkCtl register to "0." Moreover, if this bit is changed from "1" to "0" while the voltage applied to the SVBUS pin is higher than the detected voltage (the AVBUSVLDST bit of the OTGIntStt register is "1"), the AVBUSVLDST bit of the OTGIntStt register is set to "0" and an AVBUSVLDCHG interrupt occurs.	0b	R/W
10:08	SELSV	Bits for setting the detected voltage of the A_VBUS_VALID comparator Detected voltage / Bit 10 / Bit 09 / Bit 08 4.0 V / 0 / 0 / 0 4.1 V / 0 / 0 / 1 4.2 V / 0 / 1 / 0 4.3 V / 0 / 1 / 1 4.4 V / 1 / 0 / 0 4.5 V / 1 / 0 / 1 Note that it is prohibited to set values other than the above. Correct operation cannot be guaranteed if values other than these are set.	000b	R/W

Bits	Symbol	Description	Reset	R/W
07	PUCTL DP	D+ pull-up control 0: Disable 1: Enable If the EXBUFENB bit of the ChipConfig register is "1," the -PUCTLDP pin is set as follows according to the value of this bit: If this bit is "0," the -PUCTLDP pin is set to "H." If this bit is "1," the -PUCTLDP pin is set to "L." Also, if the EXBUFENB bit of the ChipConfig register is "0," the -PUCTLDP pin is set to "H" regardless of the value of this bit.	0b	R/W
06	PDCTL DM	D- pull-down control 0: Disable 1: Enable If the EXBUFENB bit of the ChipConfig register is "1," the PDCTLDM pin is set as follows according to the value of this bit: If this bit is "0," the PDCTLDM pin is set to "L." If this bit is "1," the PDCTLDM pin is set to "H." Also, if the EXBUFENB bit of the ChipConfig register is "0," the PDCTLDM pin is set to "L" regardless of the value of this bit.	1b	R/W
05	PDCTL DP	D+ pull-down control 0: Disable 1: Enable If the EXBUFENB bit of the ChipConfig register is "1," the PDCTLDP pin is set as follows according to the value of this bit: If this bit is "0," the PDCTLDP pin is set to "L." If this bit is "1," the PDCTLDP pin is set to "H." Also, if the EXBUFENB bit of the ChipConfig register is "0," the PDCTLDP pin is set to "L" regardless of the value of this bit.	1b	R/W
04	DISCHRG VBUS	Performs the discharge control of the VBUS (valid only when the VBUSMODE bits are "11b"). 0: VBUS discharge OFF, 1: VBUS discharge ON	0b	R/W
03	CHRG VBUS	Performs the charge control of the VBUS (valid only when the VBUSMODE bits are "11b"). 0: VBUS charge OFF, 1: VBUS charge ON	0b	R/W
02	DRV VBUS	Bit for setting the VBUS state (valid only when the VBUSMODE bits are "10b") 0: -PCONT (VBUS drive) pin "H" output 1: -PCONT (VBUS drive) pin "L" output	0b	R/W
01:00	VBUS MODE	Bits for specifying the VBUS control method Sets the control method of the -PCONT pin. Bit 01 Bit 00 Operation 0 x The -PCONT (VBUS drive) pin always outputs at "H" level in peripheral mode. In host mode, it is in accordance with the PPS (Port Power State) bit in the HcRhPortState register. 1 0 In accordance with the DRVVBUS bit. 1 1 In accordance the DISCHRGVBUS and CHRGVBUS bits. The -PCONT (VBUS drive) pin always outputs at "H" level.	00b	R/W

[Description]
The USBRCVENB bit specifies whether or not to enable the receiver unit of the embedded USB transceiver when the EXTBUFENB bit of the ChipConfig register is "0."
The ML60842 enables the USB transceiver (including the receiver unit) regardless of the value of this bit when the VBUS is active (for instance, while USB communication is being carried out or suspended), except for the following case. (This ML60842's enable operation is the same as when this bit is "1")

- When the CLKSTOP bit of the RstClkCtl register is "1"

Also, the ML60842 disables the USB transceiver (including the receiver unit) regardless of the value of this bit when the VBUS is inactive, except for the following case. (This ML60842's disable operation is the same as when this bit is "0").

- When the VBUS is inactive while device B (the IDSELST bit of the OTGIntStt register is "1") is operating as a peripheral (the MODE bit of the HostPeriSel register is "1")

Therefore, it is necessary to set this bit as follows under the two conditions above (when the CLKSTOP bit of the RstClkCtl register is "1," and when the VBUS is inactive while device B (the IDSELST bit of the OTGIntStt register is "1") is operating as a peripheral (the MODE bit of the HostPeriSel register is "1")), depending on whether the D+/D- pin of the USB transceiver is open-circuited (e.g., the USB interface cable is not connected).

- When the D+/D- pin of the USB transceiver is open-circuited: This bit is "0."
- When the D+/D- pin of the USB transceiver is not open-circuited: This bit is "1."

The following shows a summary of the descriptions above.

State of ML60842	IDSELST bit = "0" (device A)		IDSELST bit = "1" (device B)		Priority
	MODE bit = "0" (host)	MODE bit = "1" (peripheral)	MODE bit = "0" (host)	MODE bit = "1" (peripheral)	
CLKSTOP bit = "1"	Using this bit	Using this bit	Using this bit	Using this bit	High
VBUS inactive	Disable	Disable	Disable	Using this bit	↓
VBUS active	Enable	Enable	Enable	Enable	Low

Note: The priority indicates which state will be selected when multiple states listed in the "State of ML60842" column occur.
For example, if the VBUS inactive state occurs at the same time as the CLKSTOP bit = "1" state, this bit determines whether the receiver unit of the embedded USB transceiver is enabled or disabled because CLKSTOP bit = "1" has higher priority.

When the microcontroller detects a state with a description of "using this bit" in the table above, it must set this bit to "0" or "1" according to whether or not the D+/D- pin of the USB transceiver is open-circuited.

6.1.5 OTGIntStt Register (014h)

Bits	Symbol	Description	Reset	R/W
31:29	—	Don't care	X	X
28:27	USBIFST	Indicates the state of the USB interface. Bit 28 Bit 27 State 0 0 SE0 0 1 K state 1 0 J state 1 1 SE1 These bits are valid even if the power is down. Note that these bits indicate "10" (J state) when the USBRCVENB bit of the OTGCtl register is "0."	Note 1	R
26	BSE0SRPDETST	Indicates that the SE0 state has continued 2 ms or longer from immediately after writing "1" to the BSE0SRPDETENB bit of the OTGCtl register. 0: The state is not detected 1: The state is detected This bit can be cleared to "0" by writing "1" to this bit. The state of this bit is undefined when the power is down.	0b	R/W
25:19	—	Don't care	X	X
18	AVBUSVLDST	Indicates the state of the A_VBUS_VALID comparator. 0: Voltage of VBUS < A_VBUS_VALID_LOW threshold voltage 1: Voltage of VBUS > A_VBUS_VALID_LOW threshold voltage The state of this bit is undefined when the power is down.	0	R
17	ABSESSVLDST	Indicates the state of the AB_SESSION_VALID comparator. 0: Voltage of VBUS < AB_SESSION_VALID threshold voltage 1: Voltage of VBUS > AB_SESSION_VALID threshold voltage This bit is valid even when the power is down when ABSESSVLDENB bit = 1 (enable).	0	R
16	IDSELST	Indicates the state of the ID pin. 0:Device A 1: Device B This bit is valid even if the power is down.	Note 2	R
15	USBIFCHG	Indicates that the USB interface signal has changed from J state to either K state, SE0, or SE1 after the suspend state is detected while operating in peripheral mode. 0: No state change from J state. 1: State has changed from J state. This bit can be cleared to "0" by writing "1" to this bit. However, it takes a maximum of TBD (20 μs) from writing "1" to this bit and clearing it to "0." This bit is valid even if the power is down.	0	R/W
14:03	—	Don't care	X	X
02	AVBUSVLDCHG	Indicates the state change of the A_VBUS_VALID comparator. 0: No change 1: Changed This bit can be cleared to "0" by writing "1" to this bit. However, it takes a maximum of TBD (250 ns) from writing "1" to this bit and clearing it to "0." The state of this bit is undefined when the power is down.	0b	R/W
01	ABSESSVLDCHG	Indicates the state change of the AB_SESSION_VALID comparator. 0: No change 1: Changed This bit can be cleared to "0" by writing "1" to this bit. However, it takes a maximum of TBD (20 μs) from writing "1" to this bit and clearing it to "0." This bit is valid even if the power is down.	0b	R/W
00	IDSELCHG	Indicates the state change of the ID pin. 0: No change 1: Changed This bit can be cleared to "0" by writing "1" to this bit. However, it takes a maximum of TBD (20 μs) from writing "1" to this bit and clearing it to "0." This bit is valid even if the power is down.	0b	R/W

Note 1: Transits to the state of the USB interface pin.
Note 2: Transits to the state of the ID pin.

[Description]
The USBIFST bits reflect the state of the USB interface.
The contents of these bits indicate J state when the embedded transceiver, which is explained in the description of the USBRCVENB bit of the OTGCtl register, is disabled.
The BSE0SRPDETST bit monitors the state of the USB interface from immediately after writing "1" to the BSE0SRPDETENB bit of the OTGCtl register, and is set to "1" if the SE0 state has continued 2 ms or longer. If the BSE0SRPDETINT bit of the OTGIntMask register is "1," an interrupt is generated.
The microcontroller can use this bit to detect the initial state when starting the SRP as device B (for more information, see Section 7.1, "Session Request Protocol (SRP) Control"). The state of this bit is undefined when the power is down.
The AVBUSVLDST and ABSESSVLDST bits reflect the state of the SVBUS pin.
The IDSELST bit reflects the state of the ID pin.
The USBIFCHG bit is set to "1" if the USB interface signal has changed from J state to either K state, SE0 or SE1 after the suspend state is detected while operating in peripheral mode. If the USBIFCHGINT bit of the OTGIntMask register is "1," an interrupt is generated.
The microcontroller must set the CLKSTOP bit of the RstClkCtl register to "0" so as to set the clock supply state if this bit has been set to "1" (when the clock has been stopped (the CLKSTOP bit of the RstClkCtl register is "1") while peripheral mode has been suspended)).
This bit can be cleared to "0" by writing "1" to this bit.
Also, it takes a maximum of TBD (20 μs) from writing "1" to the USBIFCHG bit and clearing it to "0." The microcontroller must mask an interrupt with the USBIFCHGINT bit of the OTGIntMask register, write "1" to this bit, and then clear the interrupt mask by using the USBIFCHGINT bit of the OTGIntMask register after a minimum time of TBD (20 μs) has elapsed.
The AVBUSVLDCHG and ABSESSVLDCHG bits are set to "1" if the state of the SVBUS pin changes. An interrupt is generated if the AVBUSVLDCHGINT and ABSESSVLDCHGINT bits of the OTGIntMask register are "1." These bits can be cleared to "0" by writing "1" to them. If the state of the SVBUS pin changes before clearing these bits (i.e., this interrupt source occurs several times), all the interrupt sources will be cleared by writing "1" to these bits (the interrupt sources will not be queued).
For example, if the state of the SVBUS pin changes several times before clearing these bits, the values of the AVBUSVLDST and ABSESSVLDST bits before and after an interrupt may become the same.
Therefore, the microcontroller must read the AVBUSVLDST and ABSESSVLDST bits to confirm the state of the SVBUS pin.
Also, it takes a maximum of TBD (250 ns) from writing "1" to the AVBUSVLDCHG bit and clearing it to "0." The microcontroller must mask an interrupt with the AVBUSVLDCHG INT bit of the OTGIntMask register, write "1" to this bit, and then clear the interrupt mask by using the ABSESSVLDCHGINT bit of the OTGIntMask register after a minimum of TBD (250 ns) has elapsed.
It takes a maximum of TBD (20 μs) from writing "1" to the ABSESSVLDCHG bit and clearing it to "0." The microcontroller must mask an interrupt with the ABSESSVLDCHGINT bit of the OTGIntMask register, write "1" to this bit, and then clear the interrupt mask by using the ABSESSVLDCHGINT bit of the OTGIntMask register after a minimum of TBD (20 μs) has elapsed.
The IDSELCHG bit is set to "1" if the state of the ID pin changes. An interrupt is generated if the IDSELCHGINT bit of the OTGIntMask register is "1." This bit can be cleared to "0" by writing "1." If the state of the ID pin changes before clearing this bit (i.e., this interrupt source occurs several times), all the interrupt sources will be cleared by writing "1" to this bit (the interrupt sources will not be queued).
For example, if the state of the ID pin changes several times before clearing this bit, the values of the IDSELST bit before and after an interrupt may become the same. Therefore, the microcontroller must read the IDSELST bit to confirm the state of the ID pin.
Also, it takes a maximum of TBD (20 μs) from writing "1" to the IDSELCHG bit and clearing it to "0." The microcontroller must mask an interrupt with the IDSELCHGINT bit of the OTGIntMask register, write "1" to this bit, and then clear the interrupt mask by the ABSESSVLDCHGINT bit of the OTGIntMask register after a minimum of TBD (20 μs) has elapsed.

6.1.6 OTGIntMask Register (018h)

Bits	Symbol	Description	Reset	R/W
31:27	—	Don't care	X	X
26	BSE0SRPDETINT	Specifies whether or not to generate an interrupt indicating that the SE0 state has continued 2 ms or longer. 0: Interrupt disable 1: Interrupt enable	0b	R/W
23:16	—	Don't care	X	X
15	USBIFCHGINT	Specifies whether or not to generate an interrupt when the USB interface signal detects state change from J state to either K state, SE0, or SE1 after the suspend state is detected while operating in peripheral mode. 0: Interrupt disable 1: Interrupt enable	0b	R/W
14:03	—	Don't care	X	X
02	AVBUSVLDCHGINT	Specifies whether or not to generate an interrupt when the state of the A_VBUS_VALID comparator changes. 0: Interrupt disable 1: Interrupt enable	0b	R/W
01	ABSESSVLDCHGINT	Specifies whether or not to generate an interrupt when the state of the AB_ SESSION _VALID comparator changes. 0: Interrupt disable 1: Interrupt enable	0b	R/W
00	IDSELCHGINT	Specifies whether or not to generate an interrupt when the state of the ID pin changes. 0: Interrupt disabl 1: Interrupt enable	0b	R/W

[Description]
The BSE0SRPDETINT bit sets whether or not an interrupt is generated if the BSE0SRPDETST bit of the OTGIntStt register has changed to "1."
The USBIFCHGINT bit sets whether or not an interrupt is generated if the USBIFCHG bit of the OTGIntStt register has changed to "1."
The AVBUSVLDCHGINT bit sets whether or not an interrupt is generated if the AVBUSVLDCHG bit of the OTGIntStt register has changed to "1."
The ABSESSVLDCHGINT bit sets whether or not an interrupt is generated if the ABSESSVLDCHG bit of the OTGIntStt register has changed to "1."
The IDSELCHGINT bit sets whether or not an interrupt is generated if the IDSELCHG bit of the OTGIntStt register has changed to "1."

6.1.7 RstClkCtl Register (01Ch)

Bits	Symbol	Description	Reset	R/W
31:07	—	Don't care	X	X
06	CRST	Specifies to reset the entire ML60842. The entire ML60842 is reset if "1" is written to this bit. Its function is the same as the -RESET input. The microcontroller must execute initialization processing after the BUSY bit of the HostPeriSel register is set to "0" upon elapsing at least 100 μs subsequent to writing "1" to this bit. It is necessary to set the clock supply state (the CLKSTOP bit is "0") before writing "1" to this bit. Correct operation cannot be guaranteed if "1" is written to this bit in the clock supply stop state (the CLKSTOP bit is "1"). Note that writing "0" to this bit does not affect operations.	0b	W
05	HRST	Specifies to reset the entire host block (including the host core). The entire host block (including the host core) is reset if "1" is written to this bit in host mode. The BUSY bit of the HostPeriSel register is set to "1" during reset processing and to "0" upon completion of the reset processing. It is necessary to set the clock supply state (the CLKSTOP bit is "0") before writing "1" to this bit. Correct operation cannot be guaranteed if "1" is written to this bit in the clock supply stop state (the CLKSTOP bit is "1"). Note that writing "0" to this bit does not affect operations. Also note that writing "1" to this bit in peripheral mode does not affect operations, either.	0b	W
04	PRST	Specifies to reset the entire peripheral block. The entire peripheral block is reset if "1" is written to this bit in peripheral mode. The BUSY bit of the HostPeriSel register is set to "1" during reset processing and to "0" upon completion of the reset processing. It is necessary to set the clock supply state (the CLKSTOP bit is "0") before writing "1" to this bit. Correct operation cannot be guaranteed if "1" is written to this bit in the clock supply stop state (the CLKSTOP bit is "1"). Note that writing "0" to this bit does not affect operations. Also note that writing "1" to this bit in host mode does not affect operations, either.	0b	W

Bits	Symbol	Description	Reset	R/W
03	—	Don't care	X	X
02	SLCLKSTOP	[Write operation to this bit] Specifies to operate or stop the slow clock oscillation circuit inside the ML60842. 0: Operates the slow clock oscillation circuit. 1: Stops the slow clock oscillation circuit. If "1" is written when the reading value of this bit is "0," the ML60842 executes internal processing and sets the slow clock oscillation circuit stop state after a maximum of TBD (XX μs). If "0" is written when the reading value of this bit is "1," the ML60842 executes internal processing and sets the slow clock oscillation circuit operating state after a maximum of TBD (XX μs). [Read operation to this bit] Specifies to operate or stop the slow clock oscillation circuit inside the ML60842. 0: Operating the slow clock oscillation circuit 1: Stopping the slow clock oscillation circuit	0b	R/W
01	CLKSTOP	[Write operation to this bit] Specifies to supply or stop clocks to the ML60842. 0: Supplies clocks. 1: Stops supplying clocks. If "1" is written when the reading value of this bit is "0," the ML60842 executes internal processing and sets the clock supply stopped state after a maximum of TBD (XX ns). If "0" is written when the reading value of this bit is "1," the ML60842 executes internal processing and sets the clock supply state after a maximum of TBD (XX ns). Note that the oscillation circuit is not placed in the stop state even if the clock supply stopped state is set by writing "1" to this bit. To stop the oscillation circuit, it is necessary to write "1" to the XSTOP bit. [Read operation to this bit] Indicates the clock supply or stop state to the ML60842. 0: Supplying clocks 1: Stopping clock supply	0b	R/W
00	XSTOP	[Write operation to this bit] Specifies to operate or stop the oscillation circuit inside the ML60842. 0: Operates the oscillation circuit. 1: Stops the oscillation circuit. If "1" is written when the reading value of this bit is "0," the ML60842 immediately stops the operation of the oscillation circuit. If "0" is written when the reading value of this bit is "1," the ML60842 immediately starts the operation of the oscillation circuit. To write "1" to this bit and stop the operation of the oscillation circuit, it is necessary to write "1" to the CLKSTOP bit so as to set the clock supply stopped state in advance. [Read operation to this bit] Indicates the operation or stop state of the oscillation circuit inside the ML60842. 0: Operating the oscillation circuit 1: Stopping the oscillation circuit	0b	R/W

[Description]
If "1" is written to the CRST bit, the entire ML60842 (including the host core) is reset.
Its function is the same as the -RESET input. Specifically, all the registers in the common, host controller, and peripheral controller blocks are cleared and set to the initial values.
The microcontroller must execute initialization processing after the BUSY bit of the HostPeriSel register is set to "0" upon elapsing at least 100 μs subsequent to writing "1" to this bit.
In addition, the ML60842 places the USB interface in the reset state by resetting this bit. Therefore, the microcontroller must also execute initialization processing for devices being connected to the USB interface.
It is necessary to set the clock supply state (the CLKSTOP bit is "0") before writing "1" to this bit.
Correct operation cannot be guaranteed if "1" is written to this bit in the clock supply stop state (the CLKSTOP bit is "1"). Note that writing "0" to this bit does not affect operations.
If "1" is written to the HRST bit, the ML60842 resets the entire host block (including the host core) it contains.
Specifically, all the registers of the host controller block are cleared and set to their initial values. The common block and peripheral block are not reset.
The BUSY bit is set to "1" during reset processing and to "0" when the reset processing completes and the ML60842 becomes operable. Therefore, the microcontroller must execute initialization processing after the BUSY bit has been set to "0."
Also, the ML60842 places the USB interface in the reset state by resetting this bit. Therefore, the microcontroller must also execute initialization processing for devices being connected to the USB interface.
It is necessary to set the clock supply state (the CLKSTOP bit is "0") before writing "1" to this bit.
Correct operation cannot be guaranteed if "1" is written to this bit in the clock supply stop state (the CLKSTOP bit is "1"). Note that writing "0" to this bit does not affect operations.
If "1" is written to the PRST bit, the ML60842 resets the entire peripheral block it contains.
Specifically, all the registers of the peripheral controller block are cleared and set to their initial values. The common block and host block are not reset.
The BUSY bit is set to "1" during reset processing and to "0" when the reset processing completes and the ML60842 becomes operable. Therefore, the microcontroller must execute initialization processing after the BUSY bit has been set to "0."
It is necessary to set the clock supply state (the CLKSTOP bit is "0") before writing "1" to this bit.
Correct operation cannot be guaranteed if "1" is written to this bit in the clock supply stop state (the CLKSTOP bit is "1").

If "1" is written when the reading value of the SLCLKSTOP bit is "0," the ML60842 executes internal processing so as to stop the slow clock oscillation circuit upon completion of a write access cycle and is placed in the slow clock stop state after a maximum of TBD (xx μs) has elapsed. In the slow clock stop state, the following processes are performed:

- Slow clock oscillation is stopped.
- The A_VBUS_VALID comparator is disabled. In other words, it is the same state as when the AVBUSVLDENB bit of the OTGCtl register is "0." However, the value of the AVBUSVLDENB bit of the OTGCtl register itself does not change (Note).
- The AB_SESS_VALID comparator is disabled. In other words, it is the same state as when the ABSESSVLDENB bit of the OTGCtl register is "0." However, the value of the ABSESSVLDENB bit of the OTGCtl register itself does not change.
- The ID pin switching detect circuit is disabled.
- The USB transceiver (including the receiver unit) is disabled (changes in the USB interface cannot be detected).
- The suspend state signal is output to the external USB transceiver ("H" is output to the SUSPEND pin).

Note that the reading value of this bit indicates "0" (the slow clock oscillation circuit is in operation) during the execution of internal processing, and "1" (the slow clock oscillation circuit is not in operation) when the internal processing completes.
Do not access the ML60842, except for the purpose of reading this register, until the internal processing completes (i.e., the reading value of this bit is "1").
If it is accessed, correct operation cannot be guaranteed.
Also, it is necessary to write "1" to the CLKSTOP bit and complete clock stop processing prior to writing "1" to this bit. Correct operation cannot be guaranteed if "1" is written to this bit when the clock stop processing has not been completed.
Writing "0" when the reading value of this bit is "0" does not affect operations.
If "0" is written when the reading value of this bit is "1," the ML60842 executes internal processing so as to resume the slow clock oscillation circuit upon completion of a write access cycle and is placed in the slow clock resume state after a maximum of TBD (xx μs) has elapsed.
In the slow clock resume state, the following processes are performed:

- Slow clock oscillation is resumed.
- The enable/disable state of the AB_SESS_VALID comparator is reverted to the state before the slow clock oscillation stopped.
- The ID pin switching detect circuit is enabled.
- The enable/disable state of the USB transceiver (including the receiver unit) is reverted to the state before the slow clock oscillation stopped.
- The output of the suspend state signal to the external USB transceiver is reverted to the status before the slow clock oscillation stopped.

Note that the reading value of this bit indicates "1" (the slow clock oscillation circuit is in operation) during the execution of internal processing, and "0" (the slow clock oscillation circuit is not in operation) when the internal processing completes.
Do not access the ML60842, except for the purpose of reading this register, until the internal processing completes (i.e., the reading value of this bit is "0").
If it is accessed, correct operation cannot be guaranteed.
Writing "1" when the reading value of this bit is "1" does not affect operations.
Since changes in the ID pin and the USB interface signal state cannot be recognized while the slow clock oscillation circuit is stopped by writing "1" to this bit, there is a possibility that the ML60842 cannot match the operation of an remote device. Therefore, use this bit only when it is all right to completely stop the operation of a remote device, such as when it is not connected, and specifically when the operator makes a conscious choice to stop the slow clock oscillation circuit.

[Note] The purpose of the function of the SCLKSTOP bit is to completely stop the operation of the ML60842 so as to minimize the supply current of the slow clock oscillation circuit. Therefore, it forcefully disables the A_VBUS_VALID comparator.
To resume operation by writing "0" to the SCLKSTOP bit when the SCLKSTOP bit is "1," make sure to write "0" to the AVBUSVLDENB bit of the OTGCtl register before writing "1" to the CLKSTOP bit, prior to writing "1" to the

SCLKSTOP bit. If this operation is not performed, correct operation after resuming by writing "0" to the SCLKSTOP bit cannot be guaranteed.
To resume operation by writing "L" to the -RESET pin or "1" to the CRST bit when the SCLKSTOP bit is "1," it is not necessary to write "0" to the AVBUSVLDENB bit of the OTGCtl register prior to writing "1" to the SCLKSTOP bit.

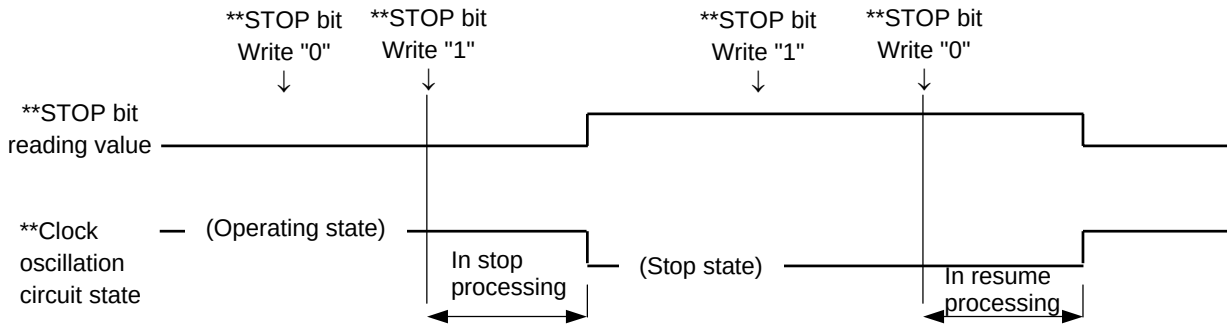
If "1" is written when the reading value of the CLKSTOP bit is "0," the ML60842 executes internal processing so as to stop the clock supply upon completion of a write access cycle and is placed in the clock supply stop state after a maximum of TBD (xx us) has elapsed. In the clock supply stop state, the following processes are performed:

- The clock supply to the internal circuits of the ML60842 is stopped (the oscillation circuit continues to operate, however).
- The clock for synchronizing the WAIT signal (WSYNC_CLK pin) is disabled.
- The USB transceiver, excluding the receiver unit, is disabled (the operation of the receiver unit depends on the setting of the USBRCVENB bit of the OTGCtl register).
- The suspend state signal is output to the external USB transceiver ("H" is output to the SUSPEND pin).
- Only the registers in the common blocks can be accessed; it is not possible to access other blocks (host controller block (registers/memory) and peripheral controller block).
- The -WAIT0/1 pin is fixed at "H" output.

Note that the reading value of this bit indicates "0" (clock is being supplied) during the execution of internal processing, and "1" (clock supply is being stopped) when the internal processing completes.
Do not access the ML60842, except for the purpose of reading this register, until the internal processing completes (i.e., the reading value of this bit is "1").
If it is accessed, correct operation cannot be guaranteed.
Writing "1" to this bit does not stop the oscillation circuit. To stop the oscillation circuit, it is necessary to write "1" to the XSTOP bit.
Also, if "1" is written to this bit while the ML60842 is in operation (such as during USB communication or DMA transfer), the subsequent operation cannot be guaranteed.
Writing "0" when the reading value of this bit is "0" does not affect operations.
To return to the clock supply state from the clock supply stop state (the reading value of this bit is "1"), write "0" to this bit. The ML60842 internally executes clock supply processing upon completion of a write access cycle and is placed in the clock supply state after a maximum of TBD (xx ns) has elapsed.
Note that the reading value of this bit indicates "1" (clock supply is being stopped) during the execution of internal processing and "0" (clock is being supplied) when the internal processing completes.
Do not access the ML60842, except for the purpose of reading this register, until the internal processing completes (i.e., the reading value of this bit is "0").
If it is accessed, correct operation cannot be guaranteed.
Write "0" to this bit when the output of the oscillation circuit is stable (the oscillation frequency and amplitude satisfy the specifications) after writing "0" to the XSTOP bit. Correct operation cannot be guaranteed if "1" is written to this bit while the output of the oscillation circuit is unstable. For more information, see Section 7.3, "Power Down Control."
Writing "1" when the reading value of this bit is "1" does not affect operations.

If "1" is written when the reading value of the XSTOP bit is "0," the ML60842 disables the oscillation circuit immediately upon completion of a write access cycle and stops operating.
Prior to writing "1" to this bit, be sure to write "1" to the CLKSTOP bit and execute clock supply stop processing. Correct operation cannot be guaranteed if "1" is written to this bit when the CLKSTOP bit is "0."
Writing "0" when the reading value of this bit is "0" does not affect operations.
To resume the operation of the oscillation circuit from the oscillation circuit operation stop state (reading value of this bit is "1"), write "0" to this bit. The oscillation circuit is enabled immediately upon completion of a write access cycle, and resumes operation.
Writing "1" when the reading value of this bit is "1" does not affect operations.

The following illustration shows the reading and writing values of the SLCLKSTOP, CLKSTOP, and XSTOP bits, and the operating state of the clock oscillation circuit.



**STOP bit represents all of the SLCLKSTOP, CLKSTOP, and XSTOP bits.

6.2 Types and Configuration of Registers for Host Controller - 1

Offset	Symbol	Name
200h	HostCtl	Host control register
204h	SttTrnsCnt	Status and RD/WR FIFO transfer length register
208h	HostDataTrnsReq	Host data transfer request register
20Ch	RamAdr	Embedded RAM address setup register
24Xh	FifoAcc	FIFO access register

For more information about the registers described below, see Section 7.7, "Precautions for Host Control" as well.

6.2.1 HostCtl Register (200h)

Bits	Symbol	Description	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:08	—	Don't care	X	X	X
07	TRNSTERM	Instructs to terminate a transfer request from the host protocol engine. Writing "1" to this bit instructs the host protocol engine to terminate transfer. Note that writing "0" to this bit does not affect operations.	0b	W	R
06:04	—	Don't care	X	X	X
03	DREQMSK	Specifies DMA transfer/PIO transfer. 0: DMA transfer (DREQ signal output) 1: PIO transfer (DREQ signal masked)	1b	R/W	R
02	—	Don't care	X	X	X
01	OHCIIRQ MASK	Host Core Interrupt Mask 0: Enable (OHCI core interrupt allowed) 1: Mask (OHCI core interrupt prohibited)	1b	R/W	R
00	DMAIRQ MASK	Host data transfer interrupt mask 0: Enable (DMA transfer request interrupt allowed) 1: Mask (DMA transfer request interrupt prohibited)	1b	R/W	R

[Description]
If "1" is written to the TRNSTERM bit during the ML60842's data transfer request period--more specifically, the period from the time an interrupt occurs when "1" is written to the DMAIRQ bit of the SttTrnsCnt register to the time of the completion of the transfer of data equal to the number of double words requested to be transferred, which is indicated by the WRCNT bit of the SttTrnsCnt register or the WRCNT bit, during this interrupt--the host controller immediately instructs the host protocol engine to execute transfer termination processing. If "1" is written to this bit other than during the ML60842's data transfer request period, transfer termination processing is executed as soon as a data transfer request is made.
If "1" is written to the TRNSTERM bit except during the ML60842's data transfer request period (i.e., other than the period from the time an interrupt occurs when "1" is written to the DMAIRQ bit of the SttTrnsCnt register to the time of the completion of the transfer of data equal to the number of double words requested to be transferred, which is indicated by the WRCNT bit of the SttTrnsCnt register or the WRCNT bit, during this interrupt), the host controller immediately executes transfer termination processing when a transfer request is made from the host protocol engine.
When the transfer termination processing completes, the ML60842 sets the UE bit of the HcInterruptStatus register to "1," generates an interrupt, and notifies the termination of transfer. The microcontroller must set the HCR bit of the HcCommandStatus register to "1" and clear the interrupt.

After that, the microcontroller must access the FifoAcc register once. Note that the data accessed at this point does not have any significance (Undefined data is read if the register is read. Written data is discarded inside the ML60842 if the register is written).

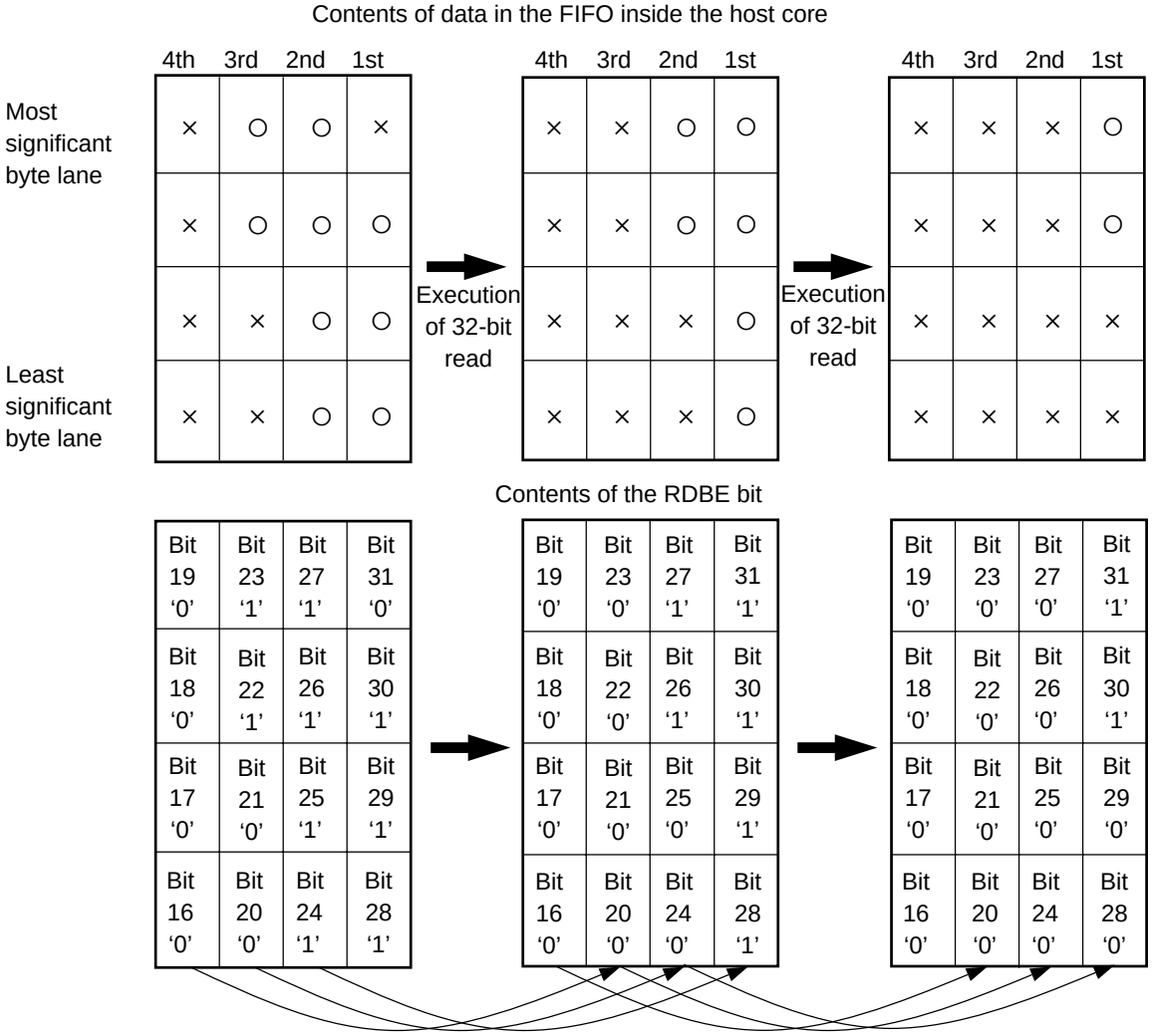
6.2.2 SttTrnsCnt Register (204h)

Bits	Symbol	Description	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:16	RDBE	Indicates a valid byte lane of the data stored in the FIFO inside the host core when reading (ML60842 → microcontroller) in 32-bit units. 0: Byte lane is disabled. 1: Byte lane is enabled. The byte lanes indicated by bits 31:16 are as follows: Bit 31: Most significant byte lane of the 1st data : Bit 28: Least significant byte lane of the 1st data Bit 27: Most significant byte lane of the 2nd data : Bit 24: Least significant byte lane of the 2nd data Bit 23: Most significant byte lane of the 3rd data : Bit 20: Least significant byte lane of the 3rd data Bit 19: Most significant byte lane of the 4th data : Bit 16: Least significant byte lane of the 4th data Also, the contents are updated every time 32 bits are read by the microcontroller, and bits 31:28 always indicate a valid byte lane of the 1st data.	0b	R	R/W
15	—	Don't care	X	X	X
14:12	WRCNT	Indicates the number of double words (1 to 40 double words) of the data to be written into the FIFO inside the host core when writing (microcontroller → ML60842).	0b	R	R/W
11	—	Don't care	X	X	X
10:08	RDCNT	Indicates the number of double words (1 to 40 DW) of the data to be read from the FIFO inside the host core when reading (ML60842 → microcontroller).	0b	R	R/W
07:02		Don't care	X	X	X
01(*)	OHCIIRQ	OpenHCI core interrupt Indicates an interrupt request from the OpenHCI core. Cleared when 1 is written. No effect when 0 is written. 0= No OpenHCI core interrupt requested 1= OpenHCI core interrupt requested	0b	R/W	R/W
00(*) (**)	DMAIRQ	DMA transfer request interrupt Indicates a DMA transfer request. Cleared when 1 is written, DREQ0 signal is asserted, and DMA transfer becomes possible. No effect when 0 is written. 0= No DMA transfer request interrupt 1=DMA transfer request interrupt	0b	R/W	R/W

(*): Cleared when "1" is written from the microcontroller.

(**): When the DREQMSK bit of the HostCtl register is "0 (DMA)," a DREQ is generated using interrupt clear as a trigger.

[Description]
The RDBE bits indicate valid byte lanes of the data stored in the FIFO inside the host core when reading (ML60842 → microcontroller) in 32-bit units. The following shows an example:



○: Indicates a byte lane storing valid data.
×: Indicates a byte lane not storing valid data.

The top middle diagram in the illustration above shows the contents of the FIFO as a result of reading the 32-bit data shown in the top left diagram once, and the bottom middle diagram shows the contents of the RDBE bits.
By reading the 32 bits shown in the top left diagram, the contents of the FIFO in the top middle diagram are shifted one step to the right. In other words, the data in the "2nd" column in the top left diagram shifts to the "1st" column in the top middle diagram. Accordingly, the contents of the RDBE bits are also shifted one step to the right in the bottom middle diagram, in relation to the top left diagram. Similarly, the contents of the "3rd" and "4th" columns in the top left diagram are shifted one step to the right to the "2nd" and "3rd" columns in the top middle diagram, respectively. Consequently, the data in the "4th" column of the bottom middle diagram becomes invalid; thus, "0" is displayed in the corresponding column of the RDBE bits as well.
The top right diagram shows the result of reading the 32 bits from the top middle diagram. Similarly, the contents of the FIFO are shifted one step further to the right and, accordingly, the contents of the RDBE bits are also shifted one step further to the right as indicated in the bottom right diagram, in relation to the bottom middle diagram.
Therefore, the microcontroller can calculate addresses in byte units by checking the contents of the RDBE bits.

6.2.3 HostDataTrnsReq Register (208h)

Bits	Symbol	Description	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:02	DMASTART	DMA transfer start address Indicates the upper 30 bits of the transfer start address when a DMA transfer request is generated. Be sure that the DMA transfer start address of the ML60842 has a 4-byte boundary.	0h	R	R/W
01	—	Don't care	X	X	X
00	DMADIR	DMA transfer direction Indicates the transfer direction when a DMA transfer request is generated. 1= Write (Microcontroller → ML60841) 0= Read (ML60841 → Microcontroller)	0b	R	R/W

See "DMA Transfer" for instructions on DMA transfer control.

6.2.4 RamAdr Register (20Ch)

Bits	Symbol	Description	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:12	IRAMBASE	Internal RAM physical address Sets the first physical address for the internal RAM in the system. Indicates the address to which ML60842 internal RAM has been mapped in the system. This register becomes valid with a write from the microcontroller. When there is no write from the microcontroller, it is judged that all transfer request addresses from the host core are outside the internal RAM address range. (This becomes a cause for host data transfer interrupts.)	0	R/W	R
11:01	—	Don't care	X	X	X
00	IRAMBASE ACT	Indicates whether or not there is write access to this register. 0: There is no write access to this register. 1: There is write access to this register. The microcontroller can judge that the setting contents of the IRAMBASE bits are valid if this bit is "1."	X	R	R/W

[Description]
The physical address to which ED, TD and HCCA are mapped depends on the value of the internal RAM address register. If no value is assigned to this register, then the OpenHCI core will not operate.
Be sure to set this register when using the host function of the ML60841.
The IRAMBASE bits go valid when a write operation is performed from the microcontroller. If no write operation is executed from the microcontroller, it is judged that all transfer request addresses from the host core are outside the embedded RAM address range (it will be a source of an interrupt pertaining to host data transfer).
Therefore, it is necessary to intentionally write "0" even if all of these bits are used as "0" (i.e., the same value as their initial values).

The IRAMBASEACT bit indicates whether or not the IRAMBASE bits are valid by write operation from the microcontroller.
If this bit is "0," it is judged that all transfer request addresses from the host core are outside the embedded RAM address range, as described above.

6.2.5 FifoAcc Register (24Xh)

Bits	Symbol	Description	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:00	DMAFIFO	FIFO access data Target address of the ML60842 during DMA transfer.	X	R/W	R/W

[Description]
The least significant 4 bits of the address are ignored when the FifoAcc register is accessed. Therefore, this register can be accessed in the address range of 240h to 24Fh.
Access to this register is valid only during the period when a transfer is requested from the host core. If this register is accessed during a period other than the transfer request period described above, data is discarded inside the ML60842 at the time of writing and undefined data is output at the time of reading.
Also, this register must be accessed in pairs of access operations so that each access can be made in 32-bit units, as described below:

- For 16 bits: Access address 24Xh twice in pairs in 16-bit width.
- For 8 bits: Access address 24Xh four times in pairs in 8-bit width.

6.3 Types and Configuration of Registers for Host Controller -2

Offset	Register Name	Offset	Register Name
100h	HcRevision	12Ch	HcBulkCurrentED
104h	HcControl	130h	HcDoneHead
108h	HcCommandStatus	134h	HcFmInterval
10Ch	HcInterruptStatus	138h	HcFmRemaining
110h	HcInterruptEnable	13Ch	HcFmNumber
114h	HcInterruptDisable	140h	HcPeriodicStart
118h	HcHCCA	144h	HcLSThreshold
11Ch	HcPeriodCurrentED	148h	HcRhDescriptorA
120h	HcControlHeadED	14Ch	HcRhDescriptorB
124h	HcControlCurrentED	150h	HcRhStatus
128h	HcBulkHeadED	154h	HcRhPortStatus

A brief description is given below. For more information, see "OpenHCI (Release: 1.0a)."
It should be noted that, when writing to the registers described in this section, they must be accessed in pairs of access operations so that each access can be made in 32-bit units.

- For 16 bits: Access each of the addresses listed in the table above and another address incremented by 2 (total of two addresses) in pairs in 16-bit width.
  For example, in the case of the HcHCCA register, it is necessary to write twice, i.e., to both 118h and 11Ah.
- For 8 bits: Access each of the addresses listed in the table above and other addresses incremented by 1, 2, and 3 each (total of four addresses) in pairs in 8-bit width.
  For example, in the case of the HcHCCA register, it is necessary to write four times, i.e., to 118h, 119h, 11Ah, and 11Bh.

6.3.1 HcRevision Register (100h)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
7:0	Revision (REV) This field shows the HCI specification version. (BCD representation)	10h	R	R

6.3.2 HcControl Register (104h)

The HcControl register defines the operating modes for the host controller.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
10	Remote Wakeup Enable (RWE) The ML60842 does not support Remote Wakeup Enable. This is always 0.	0b	R/W	R
9	Remote Wakeup Connected (WC) The ML60842 does not support Remote Wakeup Connected. This is always 0.	0b	R/W	R/W
8	Interrupt Routing (IR) The ML60842 does not support Interrupt Routing. This is always 0.	0b	R/W	R
7:6	Host Controller Functional State (HCFS) This field specifies the USB status. 00b: UsbReset	00b	R/W	R/W

<table>
<tr><td></td><td>01b: UsbResume
10b: UsbOperational
11b: UsbSuspend
If the host controller receives a resume signal from the downstream port when in the USBSUSPEND state, it will go to the USBRESUME state.</td><td></td><td></td><td></td></tr>
<tr><td>5</td><td>Bulk List Enable (BLE)
This bit enables processing of the bulk transfer list. When 1 is written, bulk transfer list processing starts after the next SOF. When 0 is written, bulk transfer list processing stops after the next SOF. When a list is processed, the host controller checks this bit. It will only be possible to modify the list the host controller stops list processing. When HcBulkCurrentED indicates the ED to be deleted, HcBulkCurrentED must be updated before the host controller driver reallows list processing.</td><td>0b</td><td>R/W</td><td>R</td></tr>
<tr><td>4</td><td>Control List Enable (CLE)
This bit enables processing of the control transfer list. When 1 is written, control transfer list processing will start after the next SOF. When 0 is written, control transfer list processing will stop after the next SOF. When list processing stops, the list can be modified. If HcControlCurrentED is pointing to an ED to be removed, HcControlCurrentED must be updated before the host controller driver re-enables list processing.</td><td>0b</td><td>R/W</td><td>R</td></tr>
<tr><td>3</td><td>Isochronous Enable (IE)
This bit enables isochronous transfer ED processing. If the isochronous transfer ED (F=1) is found when the periodic transfer list in a frame is being processed, the host controller will check the status of this bit. When it is 1, the host controller will continue to process ED. When it is 0, the host controller will stop processing of the periodic transfer list, and start processing of bulk transfer and the control transfer list. This bit is effective from the frame following the frame in which it is set.</td><td>0b</td><td>R/W</td><td>R</td></tr>
<tr><td>2</td><td>Periodic List Enable (PLE)
This bit enables processing of the periodic transfer list. When 1 is written, processing of the periodic transfer list is started after the next SOF. When 0 is written, processing of the periodic transfer list is stopped after the next SOF.</td><td>0b</td><td>R/W</td><td>R</td></tr>
<tr><td>1:0</td><td>Control Bulk Service Ratio (CBSR)
This specifies the service ratio between control transfer and bulk transfer.
<table>
<tr><th>CBSR</th><th>No. of Control EDs Over Bulk EDs Served</th></tr>
<tr><td>0</td><td>1 : 1</td></tr>
<tr><td>1</td><td>2 : 1</td></tr>
<tr><td>2</td><td>3 : 1</td></tr>
<tr><td>3</td><td>4 : 1</td></tr>
</table></td><td>00b</td><td>R/W</td><td>R</td></tr>
</table>

[Note] Be sure to insert a process to set the HCFS bits to "10b (USB operational)" before setting the HCFS bits to "11b (USB suspend)." (This is because a process to directly change the HCFS bit from its initial state of "00b (USB reset)" to "11b (USB suspend)" is out of guarantee.)

6.3.3 HcCommandStatus Register (108h)

The HcCommandStatus register is used by the Host Controller to receive commands issued by the Host Controller Driver, as well as reflecting the current status of the Host Controller.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
17:16	Scheduling Overrun Count (SOC) This field is incremented when a SchedulingOverrun error occurs. If periodic transfer list processing does not end before EOF, a SchedulingOverrun error will occur. Even if the SchedulingOverrun of HcInterruptStatus is already set, this bit will be incremented if a SchedulingOverrun error occurs.	00b	R	R/W
3	Ownership Change Request (OCR) The ML60842 does not support Ownership Change. This is always 0.	0b	R/W	R/W
2	Bulk List Filled (BLF) This bit is used to indicate whether TD is in the bulk list or not. When TD is added to an ED executing a bulk list, this bit will always be set by the host controller driver. When the host controller starts processing the head of the bulk list, it checks BLF. As long as BulkListFilled is 0, the host controller will not start processing of the bulk list. When BulkListFilled is 1, the host controller will start processing the bulk list, and set BLF to 0. When the host controller finds TD in the list, it will continue bulk list processing and set BLF to 1. If TD is not found in the bulk list, or if the host controller driver does not set BulkListFilled, then the host controller will set BLF to 0 when it finishes bulk list processing and bulk list stop processing.	0b	R/W	R/W
1	Control List Filled (CLF) When ControlListFilled is 0, the host controller will not start processing the control transfer list. When ControlListFilled is 1, the host controller will start processing the control list, and set ControlListFilled to 0. When the host controller finds TD in the list, it will continue control transfer list processing, and set ControlListFilled to 1. When TD is not found in the control list, or when the host controller driver does not set ControlListFilled, the host controller will set CLF to 0 when it finishes control list processing and control list stop processing.	0b	R/W	R/W
0	Host Controller Reset (HCR) This bit is set to initiate a software reset of the host controller. At this time, the host controller moves to the USB Suspend state, and the host controller registers excluding the root hub will be reset.	0b	R/W	R/W

6.3.4 HcInterruptStatus Register (10Ch)

This register provides status on events that cause hardware interrupts. When an event occurs, the host controller sets the corresponding bit in this register. If the interrupt of the bit is enabled in the HcInterruptEnable register and the MasterInterruptEnable bit is set, a hardware interrupt will be generated.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
30	Ownership Change (OC) The ML60842 does not support Ownership Change. This bit is always 0.	0b	R	R
6	Root Hub Status Change (RHSC) When HcRhStatus or RhPortStatus0 changes, this bit is set.	0b	R/W	R/W
5	Frame Number Overflow(FNO) When HcFmNumber overflows, this bit is set.	0b	R/W	R/W
4	Unrecoverable Error (UE) This bit is set when the host controller detects a system error that is not related to USB. When this bit is set, the host section of the ML60842 should be reset and reinitialized.	0b	R/W	R/W
3	Resume Detected (RD) This bit is set when a resume signal is received from a device connected to USB. This bit is not set when the host controller driver sets the USBRESUME state.	0b	R/W	R/W
2	Start of Frame (SF) This bit is set after the beginning of each frame, that is, the HccaFrameNumber, is updated. The host controller will send SOF packets at this time.	0b	R/W	R/W
1	Writeback Done Head (WDH) This bit is set when the host controller updates HccaDoneHead with HcDoneHead. HccaDoneHead will not be updated again until this bit is cleared. After the contents of HccaDoneHead has been saved, the host controller driver should clear this bit.	0b	R/W	R/W
0	Scheduling Overrun (SO) When the USB schedule exceeds the current frame, this bit is set, and then the HccaFrameNumber is updated. The SchedulingOverrunCount of HcCommandStatus is also incremented.	0b	R/W	R/W

[Note] The OC bit is a read-only bit and its value is fixed at "0." Therefore, this bit does not change even if the OCR bit of the HcCommandStatus register is set to "1." In addition, no interrupt is generated even if the IR bit of the HcControl register has been set to "1."

6.3.5 HcInterruptEnable Register (110h)

This register enables interrupts a bit at a time for events that cause hardware interrupts.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31	Master Interrupt Enable (MIE) 0—Ignored by HC, 1—Enables interrupt generation due to events specified in the other bits of this register. When 1 is written, the Master Interrupt Enable interrupt is enabled. Nothing happens when 0 is written.	0b	R/W	R
30	Ownership Change (OC) 0—Ignore, 1—Enable interrupt The ML60842 does not support Ownership Change. Writing 1 is invalid.	0b	R/W	R
6	Root Hub Status Change (RHSC) 0—Ignore, 1—Enable interrupt When 1 is written, the Root Hub Status Change interrupt is enabled. Nothing happens when 0 is written.	0b	R/W	R
5	Frame Number Overflow (FNO) 0—Ignore, 1—Enable interrupt When 1 is written, the Frame Number Overflow interrupt is enabled. Nothing happens when 0 is written.	0b	R/W	R
4	Unrecoverable Error (UE) 0—Ignore, 1—Enable interrupt When 1 is written, the Unrecoverable Error interrupt is enabled. Nothing happens when 0 is written.	0b	R/W	R
3	Resume Detected (RD) 0—Ignore, 1—Enable interrupt When 1 is written, the Resume Detected interrupt is enabled. Nothing happens when 0 is written.	0b	R/W	R
2	Start of Frame (SF) 0—Ignore, 1—Enable interrupt When 1 is written, the Start of Frame interrupt is enabled. Nothing happens when 0 is written.	0b	R/W	R
1	Writeback Done Head (WDH) 0—Ignore, 1—Enable interrupt When 1 is written, the Writeback Done Head interrupt is enabled. Nothing happens when 0 is written.	0b	R/W	R
0	Scheduling Overrun (SO) 0—Ignore, 1—Enable interrupt When 1 is written, the Scheduling Overrun interrupt is enabled. Nothing happens when 0 is written.	0b	R/W	R

When the interrupt enable register is read, 1 is read if each bit is enabled.

6.3.6 HcInterruptDisable Register (114h)

This register enables interrupts a bit at a time for events that cause hardware interrupts.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31	Master Interrupt Enable (MIE) 0—Ignored by HC 1—Disables interrupt generation due to events specified in the other bits of this register. The Master Interrupt Enable interrupt is prohibited when 1 is written. Nothing will happen when 0 is written.	0b	R/W	R
30	Ownership Change (OC) 0—Ignore, 1—Disable interrupt The ML60842 does not support Ownership Change. Writing 1 is invalid.	0b	R/W	R
6	Root Hub Status Change (RHSC) 0—Ignore, 1—Disable interrupt When 1 is written, the Root Hub Status Change interrupt is enabled. Nothing happens when 0 is written.	0b	R/W	R
5	Frame Number Overflow (FNO) 0—Ignore, 1—Disable interrupt When 1 is written, the Frame Number Overflow interrupt is enabled. Nothing happens when 0 is written.	0b	R/W	R
4	Unrecoverable Error (UE) 0—Ignore, 1—Disable interrupt When 1 is written, the Unrecoverable Error interrupt is enabled. Nothing happens when 0 is written.	0b	R/W	R
3	Resume Detected (RD) 0—Ignore, 1—Disable interrupt When 1 is written, the Resume Detected interrupt is enabled. Nothing happens when 0 is written.	0b	R/W	R
2	Start of Frame (SF) 0—Ignore, 1—Disable interrupt When 1 is written, the Start of Frame interrupt is enabled. Nothing happens when 0 is written.	0b	R/W	R
1	Writeback Done Head (WDH) 0—Ignore, 1—Disable interrupt When 1 is written, the Writeback Done Head interrupt is enabled. Nothing happens when 0 is written.	0b	R/W	R
0	Scheduling Overrun (SO) 0—Ignore, 1—Disable interrupt generation When 1 is written, the Scheduling Overrun interrupt is enabled. Nothing happens when 0 is written.	0b	R/W	R

When the interrupt disable register is read, 1 is read if each bit is enabled. The same value as the interrupt enable register is read.

6.3.7 HcHCCA Register (118h)

The HcHCCA register contains the physical address of the host controller communication area.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:8	Host Controller Communications Area (HCCA) Base Address Bits 7:0 will always return a 0. Indicates the physical address of the host controller communication area	0h	R/W	R
7:0	Always 0	0h	R	R

6.3.8 HcPeriodCurrentED Register (11Ch)

The HcPeriodCurrentED register indicates the physical address to the ED that is processing the current isochronous transfer or interrupt transfer.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:4	Period Current ED (PCED) Base Address Bits 3:0 will always return a 0. This bit is updated by the host controller when the periodic transfer ED is processed. The contents of this register are updated by the host controller. The host controller driver will read the content in determining which ED is currently being processed at the time of reading.	0h	R	R/W
3:0	Always 0	0h	R	R

6.3.9 HcControlHeadED Register (120h)

The HcControlHeadED register indicates the physical address of the first ED in the control transfer list.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:4	Control Head ED (CHED) Base Address Bits 3:0 will always return a 0. The host controller processes the control transfer list that starts with the HcControlHeadED pointer.	0h	R/W	R
3:0	Always 0	0h	R	R

6.3.10 HcControlCurrentED Register (124h)

The HcControlCurrentED register contains the physical address of ED of the control transfer list that is currently being processed.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:4	Control Current ED (CCED) Base Address Bits 3:0 will always return a 0. When the processing of the current control transfer ED is finished, the host controller sets the pointer to the next ED to be processed. When ControlListFilled of HcCommandStatus is set to 1, the host controller copies the contents of HcControlHeadED in HcControlCurrentED, and clears the bit. When 1 is not set, nothing happens. Only when 1 is not set in ControlListEnable of HcControl, the host controller driver can modify this driver. When 1 is set, the host controller driver can only read in order to know the current ED that is being processed. Set 0 as the initial value	0h	R/W	R/W
3:0	Always 0	0h	R	R

6.3.11 HcBulkHeadED Register (128h)

The HcBulkHeadED register contains the physical address for the first ED of the bulk transfer list.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:4	Bulk Head ED (BHED) Base Address Bits 3:0 will always return a 0. The host controller processes the bulk list that starts with the HcBulkHeadED pointer.	0h	R/W	R
3:0	Always 0	0h	R	R

6.3.12 HcBulkCurrentED Register (12Ch)

The HcBulkCurrentED register contains the physical address of ED of the bulk transfer list that is currently being processed.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:4	Bulk Current ED (BCED) Base Address Bits 3:0 will always return a 0. When the processing of the current control transfer ED is finished, the host controller sets the pointer to the next ED to be processed. When BulkListFilled of HcCommandStatus is set to 1, the host controller copies the contents of HcBulkHeadED in HcBulkCurrentED, and clears the bit. When 1 is not set, nothing happens. Only when 1 is not set in ControlListEnable of HcControl, the host controller driver can modify this driver. When 1 is set, the host controller driver can only read in order to know the current ED that is being processed. Set 0 as the initial value.	0h	R/W	R/W
3:0	Always 0	0h	R	R

6.3.13 HcDoneHead Register (130h)

The HcDoneHead register contains the physical address of the last TD added to the Done queue after processing is finished. In normal operations, the host controller driver should not read this register.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:4	Done Head ED (DH) Base Address Bits 3:0 will always return a 0. When TD is finished, the host controller writes the value of HcDoneHead in the NextTD field of the TD. Next, it overwrites the address of the TD in HcDoneHead. This is set to 0 whenever the host controller writes the contents of this register to HCCA. It also sets WritebackDoneHead of HcInterruptStatus.	0h	R	R/W
3:0	Always 0	0h	R	R

6.3.14 HcFmInterval Register (134h)

The HcFmInterval register includes a 14-bit value that indicates the bit time interval in the frame (between two consecutive SOFs), and a 15-bit value that indicates the maximum packet size that transmits and receives at full speed without causing a scheduling overrun in the host controller. The host controller driver can adjust the frame interval by writing a new value at each SOF. This provides a mechanism in which the host controller can synchronize with external clocking source and adjust any known local clock offset.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31	Frame Interval Toggle (FIT) When loading a new value for the FrameInterval, the host controller driver should toggle this bit.	0b	R/W	R
30:16	FS Largest Data Packet (FSMPS) This field specifies the value loaded in Frame Remaining of the frame remain register that comes at the beginning of each frame. This value indicates the maximum number of bits that can be transmitted and received by the host controller during one transaction within the allotted time without causing a scheduling overrun.	0h	R/W	R
13:0	Frame Interval (FI) This bit specifies the interval between two consecutive SOFs in bit times.	2EDFh	R/W	R

[Note] To utilize control using packets whose sizes do not satisfy MaximumPacketSize (short packets) (refer to Section 4.3.1.3.5 of "OpenHCI Release 1.0a"), it is necessary to set FSMPS and FI by taking account of the data processing time of the microcontroller. For more information, see (4), "HcFmInterval Register" in Section 7.7, "Precautions for Host Control."

6.3.15 HcFmRemaining Register (138h)

The HcFmRemaining register is a 14-bit down counter that shows the bit time remaining in the current frame.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31	Frame Remaining Toggle (FRT) When FrameRemaining reaches 0, this bit is loaded from FrameIntervalToggle of HcFmInterval. This bit is used by the host controller driver to synchronize FrameInterval and FrameRemaining.	0b	R	R/W
13:0	Frame Remaining (FR) This counter is decremented each bit. After it reaches 0, the FrameInterval value of HcFmInterval is loaded at the next frame boundary. When in the USBOPERATIONAL state, the host controller copies FrameInterval of HcFmInterval, and starts counting again from the next SOF.	0h	R	R/W

[Note] This register is write-disabled. If an attempt is made to write to this register, correct operation cannot be guaranteed.

6.3.16 HcFmNumber Register (13Ch)

The HcFmNumber register is a 16-bit counter. This register provides a timing reference among events happening in the host controller and host controller driver.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
15:0	Frame Number (FN) This bit is incremented when HcFmRemaining is reloaded. When the value reaches ffffh, it next becomes 0000h. When in the USBOPERATIONAL state, it is incremented automatically. After the host controller has incremented FrameNumber at each frame boundary and sent SOF but before the host controller reads the first ED in the frame, the content will be written to HCCA. The host controller sets StartofFrame of HcInterruptStatus after it writes the value of this register into the HccaFrameNumber field of HCCA.	0h	R	R/W

[Note] This register is write-disabled. If an attempt is made to write to this register, correct operation cannot be guaranteed.

6.3.17 HcPeriodicStart Register (140h)

The HcPeriodicStart register specifies the bit time at which the host controller starts processing of the periodic transfer list.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
13:0	Periodic Start (PS) After a hardware reset, this field is cleared. Then, it should be set by the host controller driver while the host controller is being initialized. Normally, it is set to 3E67h, which is a 10% OFF value of the HcFmInterval. When HcFmRemaining reaches the specified value, processing of the periodic transfer list starts with control transfer and bulk transfer receiving priority.	0h	R/W	R

6.3.18 HcLSThreshold (144h)

The HcLSThreshold register includes the value of the 11 bits that the host controller uses to determine whether to commit to the transfer of a maximum of 8-byte low speed packet before EOF. During operation, neither the host controller nor the host controller driver can change this value.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
11:0	LS Threshold This field is compared with the FrameRemaining field when low speed transactions are started. Transactions are only started when the value of the FrameRemaining field is equal to or larger than this field. The value is calculated during initialization by the host controller driver with the consideration of transmission and setup overhead.	628h	R/W	R

6.3.19 HcRhDescriptorA Register (148h)

The HcRhDescriptorA register is one of two registers that describe the characteristics of the root hub. The descriptor length (11), descriptor type (TBD) and hub controller current (0) fields of the hub class descriptor should be emulated by the host controller driver. Other fields are indicated in the HcRhDescriptorA and HcRhDescriptorB registers.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31:24	Power On to Power Good Time (POTPGT) This field specifies the duration the host controller driver must wait before the root hub can access a port to which power is supplied. The unit of time is 2 ms. The duration is calculated as (POTPGT × 2) ms	32h	R/W	R
12	No Overcurrent Protection (NOCP) This bit decribes the reporting method for the root hub overcurrent status. 0: Overcurrent status is reported. 1: Overcurrent status is not reported	0b	R/W	R
11	Overcurrent Protection Mode (OCPM) This bit specifies the reporting method for the root hub overcurrent status. This field is only valid when the NoOverCurrentProtection field is 0. 0: Overcurrent status for all ports is reported. 1: Overcurrent status is reported by port. Because the ML0841 only has one downstream port, always set this bit to 0.	0b	R/W	R
10	Device Type (DT) This field is always 0.	0b	R	R
9	No Power Switching (NPS) This bit specifies either that root hub power switching is supported or that ports are always powered. 0: Port power switched 1: Ports are always powered on when the host controller is powered on. This should always be set to 0 for the ML60842.	0b	R/W	R
8	Power Switching Mode (PSM) This bit specifies the control method for power switching. 0: Power is supplied concurrently to all ports. 1: Power is supplied individually to ports. Because the ML60842 only has one downstream port, this is always set to 0.	0b	R/W	R
7:0	Number Downstream Ports (NDP) This field specifies the number of downstream ports of the root hub. This is 1 for the ML60842.	1h	R	R

6.3.20 HcRhDescriptorB Register (14Ch)

The HcRhDescriptorB register is one of two registers that describes the characteristics of the root hub.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
17	Port Power Control Mask (PPCM) There is no need to use this with the ML60842. Always set this to 0.	0b	R/W	R
1	Device Removable (DR) There is no need to use this with the ML60842. Always set this to 0.	0b	R/W	R

6.3.21 HcRhStatus register (150h)

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
31	Clear Remote Wakeup Enable (CRWE) When 1 is written, DeviceRemoveWakeupEnable is cleared. When 0 is written, nothing will happen.	0b	W	R
17	Overcurrent Indicator Change (OCIC) When a change occurs in the OCI field of this register, this bit will be set by hardware. When 1 is written, DeviceRemoveWakeupEnable is cleared. When 0 is written, nothing will happen.	0b	R/W	R/W
16	Local Power Status Change (LPSC) (When reading) **LocalPowerStatusChange (LPSC)** This is always 0 for the ML60842. (When writing) **SetGlobalPower** When 1 is written, GlobalPower is set, and power is supplied to the ports. When 0 is written, nothing will happen.	0b	R/W	R
15	Device Remote Wakeup Enable (DRWE) (When reading) **DeviceRemoteWakeupEnable** When the ConnectStatusChange bit is set, this bit specifies whether to set the ResumeDetected interrupt as a resume event. 0: Remote wakeup event 1: Not a remote wakeup event (When writing) **SetRemoteWakeupEnable** When 1 is written, DeviceRemoveWakeupEnable is set. When 0 is written, nothing will happen.	0b	R/W	R
1	Overcurrent Indicator (OCI) This bit indicates the overcurrent status. 0: Operating normally 1: Overcurrent generated	0b	R	R/W
0	Local Power Status (LPS) (When reading) **LocalPowerStatus** This is always 0 for the ML60841. (When writing) **ClearGlobalPower** When 1 is written, GlobalPower is cleared and power is not supplied to the ports. When 0 is written, nothing will happen.	0b	R/W	R

6.3.22 HcRhPortStatus register (154h)

The HcRhPortStatus1 register controls events in port units, and is used to report their status. The lower word reflects the port status. The upper word reflects the change in status. When executing a write that changes the port status, do not update this register until the processing is completed (i.e., until the port status is updated). Always write 0 to reserved bits.

The ML60842 only has one downstream port that is supported.

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
20	Port Reset Status Change (PRSC) This bit is set when 10 ms port reset is completed. 0: Port reset not completed 1: Port reset completed When 1 is written, Port Reset Status Change is cleared. When 0 is written, nothing will happen.	0b	R/W	R/W
19	Port Overcurrent Indicator Change (OCIC) This is always 0 for the ML60842.	0b	R/W	R/W
18	Port Suspend Status Change (PSSC) This bit is set when the resume sequence is completed. This sequence includes the 20ms resume pulse, LS EOP, and 3 ms resynchronizing delay. 0: Resume is not completed 1: Resume is completed When 1 is written, Port Suspend Status Change is cleared. When 0 is written, nothing will happen. When Reset Status Change is set, this bit will also be cleared.	0b	R/W	R/W
17	Port Enable Status Change (PESC) When the PortEnableStatus bit is cleared by a hardware event, this bit is set. This bit is not set by a write from the host controller driver. When 1 is written, Port Enable Status Change is cleared. When 0 is written, nothing will happen. 0: No change in PortEnableStatus 1: PortEnableStatus has changed	0b	R/W	R/W
16	Connect Status Change (CSC) This bit is set when a connection or a disconnect event is generated. When 1 is written, Connect Status Change is cleared. When 0 is written, nothing will happen. When writing to SetPortReset, SetPortEnable, or SetPortSuspend, CurrentConnectStatus is cleared and this bit is set. It is necessary to reconnect the host controller driver. 0: No change in CurrentConnectStatus 1: Change in CurrentConnectStatus	0b	R/W	R/W

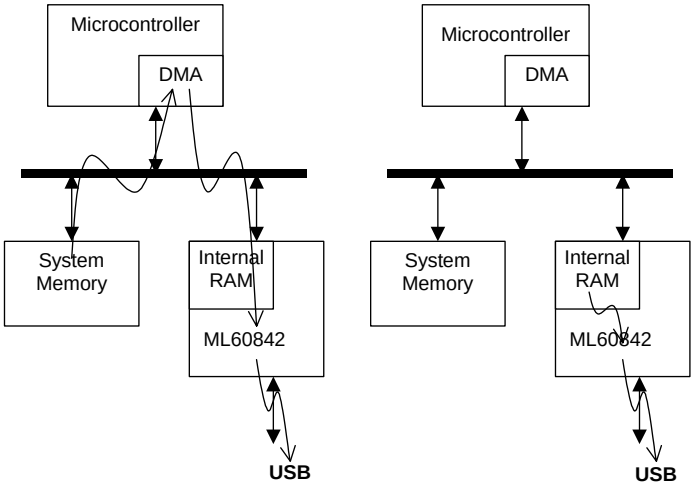
Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
9	Low-speed Device Attached (LSDA) (When reading) **Low Speed Device Attached (LSDA)** This bit indicates the speed of a connected device. This field is only valid when CurrentConnectStatus is set. 0: Full speed device attached 1: Llow speed device attached (When writing) **Clear Port Power** When 1 is written, PortPowerStatus is cleared. When 0 is written, nothing will happen.	0b	R/W	R/W
8	Port Power Status (PPS) (When reading) **PortPowerStatus (PPS)** This bit indicates the port power status. When overcurrent status is detected, this bit is cleared. The host controller driver sets this bit by writing SetGlobalPower. The host controller driver clears this bit by writing ClearGlobalPower. When the power power is invalid, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus are cleared. 0: Port power is off. 1: Port power is on. (When writing) **SetPortPower** When 1 is written, PortPowerStatus is cleared. When 0 is written, nothing will happen.	0b	R/W	R/W
4	Port Reset Status (PRS) (When reading) **PortResetStatus (PRS)** When SetPortReset is set, the port reset signal is active. After reset is completed and PortResetStatusChange is set, this bit is cleared. When CurrentConnectStatus is 0, this bit is not set. 0: Port reset signal is not active. 1: Port reset signal is active. (When writing) **SetPortReset** When 1 is written, SetPortReset is set. When 0 is written, nothing will happen. When CurrentConnectStatus is 0, PortResetStatus is not set but ConnectStatusChange is set when 1 is written.	0b	R/W	R/W
3	Port Overcurrent Indicator (POCI) (When reading) **PortOverCurrentIndicato (POCI)** This is always 0 for ML60841. The overcurrent status is notified by the Overcurrent Indicator. (When writing) **ClearSuspendStatus** When 1 is written, resume is started. When 0 is written, nothing will happen. Resume starts only when PortSuspendStatus is set.	0b	R/W	R/W

Bits	Field	Reset	HCD (Host Controller Driver)	HC (Host Controller)
2	(When reading) **PortSuspendStatus (PSS)** This bit indicates that a port is suspended or in the resume sequence. This bit is set by a write to SetSuspendState and cleared when PortSuspendStatusChange is set at the end of resume. When CurrentConnectStatus is 0, this bit is not set. When PortResetStatusChange is set at the end of port reset or when the host controller goes to the USBRESUME state, this bit will be cleared. 0: Port is not suspended. 1: Port is suspended. (When writing) **SetPortSuspend** When 1 is written, PortSuspendStatus is set. When 0 is written, nothing will happen. When CurrentConnectStatus is 0, PortSuspendStatus is not set. Instead, ConnectStatusChange is set.	0b	R/W	R/W
1	Port Enable Status (PES) (When reading) **PortEnableStatus (PES)** This bit indicates whether a port is valid or invalid. The rot hub clears this bit for overcurrent conditions, disconnect events, power off and operational bus errors, such as bubbles. When this bit changes, PortEnableStatusChange is set. When CurrentConnectStatus is 0, this bit is not set. 0: Port is disabled. 1: Port is enabled. (When writing) **SetPortEnable** When 1 is written, PortEnableStatus is set. When 0 is written, nothing will happen. When CurrentConnectStatus is 0, PortEnableStatus is not set. Instead, ConnectStatusChange is set.	0b	R/W	R/W
0	Current Connect Status (CCS) (When reading) **CurrentConnectStatus (CCS)** This bit indicates the current status of downstream ports. 0: No device connected 1: Device connected (When writing) **ClearPortEnable** When 1 is written, PortEnableStatus is cleared. When 0 is written, nothing will happen. When CurrentConnectStatus is 0, PortEnableStatus is not set. CurrentConnectStatus is not affected by arbitrary writes.	0b	R/W	R/W

6.4 Host Controller Memory

The ML60842 has 4K bytes of internal RAM for communications between the microcontroller and host controller. In order to transfer data from system memory on the microcontroller side to the USB, the data must first be copied to this host controller memory before transferring or the transfer must be executed by using DMA.

Normal OpenHCI controllers operate as bus masters, and acquire HCCA and the ED and TD of each transfer directly from system memory. Because the ML60842 acts as a bus slave, it must use DMA to acquire data in system memory. In order to prevent ML60842 operation from imposing a burden on microcontroller operation, HCCA, ED, and TD should be resided in the RAM internal to the ML60842. If these are resided in microcontroller system memory, DMA transfer requests will occur frequently, and this may affect other processing of the microcontroller.



Offset	Description	Reset	HCD (Host Controller Driver)	HC (Host Controller)
1000h -1FFFh	4KB (1K double words) HCCA, ED/TD buffer memory	X	R/W	R/W

6.5 Types and Configuration of the Registers for the Peripheral Controller

Category	Offset	R/W	Bit position			
			Bits31:24	Bits23:16	Bits15:8	Bits7:0
FIFO	400h	W	EP0 transmit FIFO (EP0TXFIFO)			
	404h	R	EP0 receive FIFO (EP0RXFIFO)			
	41Xh	R/W	EP1 transmit/receive FIFO (EP1FIFO)			
	42Xh	R/W	EP2 transmit/receive FIFO (EP2FIFO)			
	43Xh	R/W	EP3 transmit/receive FIFO (EP3FIFO)			
	44Xh	R/W	EP4 transmit/receive FIFO (EP4FIFO)			
	45Xh	R/W	EP5 transmit/receive FIFO (EP5FIFO)			
Common	300h	R	wValueMSB setup register (wValueMSB)	wValueLSB setup register (wValueLSB)	bRequest setup register (bRequest)	BmRequestType setup register (bmRequestType)
	304h	R	WLengthMSB setup register (wLengthMSB)	WLengthLSB setup register (wLengthLSB)	wIndexMSB setup register (wIndexMSB)	wIndexLSB setup register (wIndexLSB)
	308h	R/W				Device address register (DVCADR)
	30Ch	R			Frame number register MSB(FRAME MSB)	Frame number register LSB(FRAME LSB)
	310h	R/W			Interrupt status register 1 (INTSTAT1)	Interrupt status register 2 (INTSTAT2)
	314h	R/W			Interrupt enable register 1 (INTENBL1)	Interrupt enable register 2 (INTENBL2)
	318h	R/W				System control register (SYSCON)
	31Ch	R/W			ISO mode select register (ISOMODE)	Transmit packet ready control register (TXPKTCONT)
DMA	320h	R/W				DMA0 control register (DMA0CON)
	324h	R/W				DMA1 control register (DMA1CON)

*1) Access to any of unlisted bits has no significance.

*2) Access to the FIFOs

- For 16 bits: Access each of the addresses listed in the table above twice in pairs in 16-bit width. For example, in the case of EP1, it is necessary to access 41Xh twice.
- For 8 bits: Access each of the addresses listed in the table above four times in pairs in 8-bit width. For example, in the case of EP1, it is necessary to access 41Xh four times.

*3) The shaded sections indicate that these registers have different specifications from the registers of the ML60852A and the differences are described in this specification document.

Category	Offset	R/W	Bit position			
			Bits31:24	Bits23:16	Bits15:8	Bits7:0
EP support	330h	R			EP0 payload register (EP0PLD)	EP0 configuration register (EP0CONF)
	334h	R/W			EP1payload register (EP1PLD)	EP1 configuration register (EP1CONF)
	338h	R/W			EP2 payload register (EP2PLD)	EP2 configuration register (EP2CONF)
	33Ch	R/W			EP3 payload register (EP3PLD)	EP3 configuration register (EP3CONF)
	340h	R/W	EP4 payload register MSB (EP4PLDMSB)	EP4 payload register LSB (EP4PLDLSB)		EP4 configuration register (EP4CONF)
	344h	R/W	EP5 payload register MSB (EP5PLDMSB)	EP5 payload register LSB (EP5PLDLSB)		EP5 configuration register (EP5CONF)
	348h	R/W			EP0 receive byte count (EP0RXCNT)	EP0 status register (EP0STAT)
	34Ch	R/W			EP1 receive byte count (EP1RXCNT)	EP1 status register (EP1STAT)
	350h	R/W			EP2 receive byte count (EP2RXCNT)	EP2 status register (EP2STAT)
	354h	R/W			EP3 receive byte count (EP3RXCNT)	EP3 status register (EP3STAT)
	358h	R/W	EP4 receive byte count MSB (EP4RXCNT MSB)	EP4 receive byte count LSB (EP4RXCNT LSB)		EP4 status register (EP4STAT)
	35Ch	R/W	EP5 receive byte count MSB (EP5RXCNT MSB)	EP5 receive byte count LSB (EP5RXCNT LSB)		EP5 status register (EP5STAT)
	360h	R/W				EP0 transmit data byte count register (EP0TXCNT)
	364h	R/W				EP1transmit data byte count register (EP1TXCNT)

*1) Access to any of unlisted bits has no significance.
*2) The shaded sections indicate that these registers have different specifications from the registers of the ML60852A and the differences are described in this specification document.

Category	Offset	R/W	Bit position			
			Bits31:24	Bits23:16	Bits15:8	Bits7:0
EP support	368h	R/W				EP2 transmit data byte count register (EP2TXCNT)
	36Ch	R/W				EP3 transmit data byte count register (EP3TXCNT)
	370h	R/W			EP4 transmit data byte count register MSB (EP4TXCNT MSB)	EP4 transmit data byte count register LSB (EP4TXCNT LSB)
	374h	R/W			EP5 transmit data byte count register MSB (EP5TXCNT MSB)	EP5 transmit data byte count register LSB (EP5TXCNT SB)
	378h	R/W				EP0 control register (EP0CONT)
	37Ch	R/W				EP1 control register (EP1CONT)
	380h	R/W				EP2 control register (EP2CONT)
	384h	R/W				EP3 control register (EP3CONT)
	388h	R/W				EP4 control register (EP4CONT)
	38Ch	R/W				EP5 control register (EP5CONT)

*1) Access to any of unlisted bits has no significance.
*2) The shaded sections indicate that these registers have different specifications from the registers of the ML60852A and the differences are described in this specification document.

(The registers for the peripheral controller conform to the ML60852A. The following shows the registers that are not listed in the ML60852A Data Sheet because they are different from those of the ML60852A or their categories are classified as optional.)

6.5.1 INTENBL1/2 Register (314h)

Bits	Symbol	Description	Reset	USB Reset	R/W
31:16	—	Don't care	X	X	X
15	EP0TXRDY	EP0 transmit packet ready interrupt enable	0b	Maintains the state before reset.	R/W
14	EP0RXRDY	EP0 receive packet ready interrupt enable	0b		R/W
13	EP5RDY	EP5 packet ready interrupt enable	0b		R/W
12	EP4RDY	EP4 packet ready interrupt enable	0b		R/W
11	EP3RDY	EP3 packet ready interrupt enable	0b		R/W
10	EP2RDY	EP2 packet ready interrupt enable	0b		R/W
09	EP1RDY	EP1 packet ready interrupt enable	0b		R/W
08	EP0RDY	Setup ready interrupt enable	1b		R/W
07:05	—	Don't care	000b		X
04	AWAKE	Device awake state interrupt enable	0b		R/W
03	USBSUS	Device suspend state interrupt enable	0b		R/W
02	USBOPE	USB interface reset deassert interrupt enable	0b		R/W
01	USBRST	USB interface reset assert interrupt enable	0b		R/W
00	SOF	SOF interrupt enable	0b		R/W

[Note] Only the content of the EP5RDY bit is different from the contents described in the ML60852A Data Sheet. For more information about the bits other than the EP5RDY bit, refer to the ML60852A Data Sheet.

[Description]
No EP5 packet ready interrupt occurs regardless of the value of the EP5RDY bit when 5EP mode is selected (EPMODE bit 02 of the SYSCON register is "1").
Similarly, bit 13 (EP5 packet ready interrupt status) of the INTSTAT1 register is always set to "0."

6.5.2 SYSCON Register (318h)

Bits	Symbol	Description	Reset	USB Reset	R/W
31:05	—	Don't care	X	X	X
04	RMTWKUP	Remote wakeup is executed by writing "1." This bit itself stays "0."	0b	Maintains the state before reset.	W
3	—	Don't care	X	X	X
02	EPMODE	Specifies the EP mode. 0: 6EP mode, 1: 5EP mode	0b	Maintains the state before reset.	R/W
01:00	—	Don't care	X	X	X

[Note] Only the contents of the RMTWKUP bit are different from the contents described in the ML60852A Data Sheet.
For more information about the EPMODE bit, refer to the ML60852A Data Sheet.

[Description]
If "1" is written in the RMTWKUP bit, remote wakeup is executed. This bit stays "0."
It is necessary to set the CLKSTOP bit of the RstClkCtl register to "1" so as to set the clock supply state before writing "1" to this bit.

6.5.3 ISOMODE/TXPKTCONT Register (31Ch)

Bits	Symbol	Description	Reset	USB Reset	R/W
31:14	—	Don't care	X	X	X
13	EP5MODE	The EP5MODE bit goes valid only if the EP5 has been configured for ISO IN transfer. This bit specifies when to switch the sides of the double-sided FIFO corresponding to the EP5 and when to clear the FIFO. 0: Switches the sides of the FIFO and clears the FIFO at every SOF reception. 1: Switches the sides of the FIFO and clears the FIFO only when an IN token to the EP5 has been sent from the host in just the previous frame. The ML60842 refers to this bit every time it receives an SOF and executes the corresponding operation.	0b	0b	R/W
12	EP4MODE	The EP4MODE bit goes valid only if the EP4 has been configured for ISO IN transfer. This bit specifies when to switch the sides of the double-sided FIFO corresponding to the EP4 and when to clear the FIFO. 0: Switches the sides of the FIFO and clears the FIFO at every SOF reception. 1: Switches the sides of the FIFO and clears the FIFO only when an IN token to the EP4 has been sent from the host in just the previous frame. The ML60842 refers to this bit every time it receives an SOF and executes the corresponding operation.	0b	0b	R/W
07:06	—	Don't care	X	X	X
05	EP5 TXPKTCONT	Specifies the EP5 transmit packet ready interrupt and the assert/deassert condition for the EP5TXRDY bit of the EP5STAT register.	0b	Maintains the state before reset.	R/W
04	EP4 TXPKTCONT	Specifies the EP4 transmit packet ready interrupt and the assert/deassert condition for the EP4TXRDY bit of the EP4STAT register.	0b		R/W
03	EP3 TXPKTCONT	Reserved (write "0" at the time of write operation.)	0b		R/W
02	EP2 TXPKTCONT	Specifies the EP2 transmit packet ready interrupt and the assert/deassert condition for the EP2TXRDY bit of the EP2STAT register.	0b		R/W
01	EP1 TXPKTCONT	Specifies the EP1 transmit packet ready interrupt and the assert/deassert condition for the EP1TXRDY bit of the EP1STAT register.	0b		R/W
00	—	Reserved (write "0" at the time of write operation.)	0b		R/W

[Description]
The transmit packet ready interrupt generation condition can be changed by manipulating the EP5TXPKTCONT, EP4TXPKTCONT, EP2TXPKTCONT, and P1TXPKTCONT bits.
The following shows how the interrupt occurrence conditions are set by the state of the EPn transmit FIFO and the state of the EPnTXPKTCONT bit when the EPnRDY bit is "1."

EPn transmit FIFO state	EPnTXPKTCONT bit = "0"	EPnTXPKTCONT bit = "1"
Neither side A nor side B is empty.	-INTR signal is in deassert state.	-INTR signal is in deassert state.
One side is empty, and the other is not empty.	-INTR signal is in assert state.	-INTR signal is in deassert state.
Both sides A and B are empty.	-INTR signal is in assert state.	-INTR signal is in assert state.

[Note] The transmit FIFO is empty when either one of the following conditions is satisfied:
- Writing to the FIFO from the microcontroller has not been completed and "1" has not been written to bit 01 of the EPnSTAT register.
- Transmit data written to the FIFO by the microcontroller was transferred to the host and the host returned an ACK.

The following shows the assert and deassert conditions for bit 01 (transmit packet ready bit) of the EPnSTAT register when this bit is set to "1."

	Condition	Operation
Assert	When the microcontroller has set the transmission packet ready bit of either side A or B to "1".	Transmission from the EPn can be performed (data transmission for an IN token) when either side A or B has been asserted.
Deassert	When an ACK has been received from the host for the transmit data of both sides A and B	The EP4 and EP5 are locked (a NACK is replied for an IN token) when the transmit data of neither side A nor side B is ready.

The EP5MODE and EP4MODE bits are valid only if the EP5 and EP4 have been configured for ISO IN transfer, respectively. These bits define the switching of the sides of the corresponding double-sided FIFOs and FIFO clear timings at ISO IN transfer.
If the EP4 and EP5 have been configured for other than the ISO IN transfer, these bits are ignored (does not affect operations).
For more information about how to use this bit, see Section 7.8, "Precautions for Peripheral Control."

6.5.4 DMA0CON Register (320h), DMA1CON Register (324h)

Bits	Symbol	Description	Reset	USB Reset	R/W
31:08	—	Don't care	X	X	X
07	—	Don't care	X	X	X
06:05	DMA0EP (for DMA0) DMA1EP (for DMA1)	Specifies the EP as the target of DMA transfer *1,*2 0: EP1, 1: EP2, 2: EP4, 3: EP5	00b	Maintains the state before reset.	R/W
04:03	—	Don't care	X	X	X
02	DMA0INS (for DMA0) DMA1INS (for DMA1)	Specifies whether or not to insert DMA byte count when the EP specified as the target of DMA transfer has been configured for bulk transfer or interrupt transfer.*1, *3 0: Does not insert byte count. 1: Inserts byte count at the beginning of transfer data.	0b	Maintains the state before reset.	R/W
01	—	Don't care	X	X	X
00	DMA0EN (for DMA0) DMA1EN (for DMA1)	DMA enable*1 0: DMA disable, 1: DMA enable	0b	Maintains the state before reset.	R/W

*1) Complete the settings of the DMA0EP, DMA1EP, DMA0INS, DMA1INS, DMA0EN, and DMA1EN bits before token packets for the EP1 to EP15 arrive, and do not change them thereafter.
Correct operation cannot be guaranteed if they are changed.

*2) If the same EP is specified for DMA channels 0 and 1, DREQ0/1, DRACK0/1, and DACK0/1 will have the same values.

*3) Although DMA transfer can be executed for bulk, interrupt, and isochronous transfers, the DMA byte count insertion function set by this bit is valid only for bulk and interrupt transfers.
Correct operation cannot be guaranteed if this bit is set to "1" for isochronous transfer.

6.5.5 EP5PLD Register MSB/LSB/EP5CONF Register (344h)

Bits	Symbol	Description	Reset	USB Reset	R/W
31:24	EP5MAXSZ MSB	MSB of the maximum EP5 packet size	00h	Maintains the state before reset.	R/W
23:16	EP5MAXSZ MSB	LSB of the maximum EP5 packet size	00h		R/W
15:08	—	Don't care	X	X	X
07	EP5DIR	EP5 transfer direction	0b	Maintains the state before reset.	R/W
06:05	—	Don't care	X	X	X
04	EP5CONF	EP5 configuration	0b	Maintains the state before reset.	R/W
03:02	—	Don't care	X	X	X
01:00	EP5TYPE	EP5 transfer type	00b	Maintains the state before reset.	R/W

[Note] Only the contents of the EP5CONF bit are different from the contents described in the ML60852A Data Sheet. For more information about the bits other than the EP5CONF bit, refer to the ML60852A Data Sheet.

[Description]
If a Set Configuration request to activate the EP5 is received from the host, write "1" to the EP5CONF bit from the microcontroller in the status stage of control transfer.
Data transmission and reception between the host and the EP5 are enabled when this bit is "1." If this bit is "0," no response is made to transactions targeted for the EP5.
However, when the EP5 mode is selected (the EPMODE bit of the SYSCON register is "1"), no response is made to transactions targeted for the EP5 regardless of the value of the EP5CONF bit. In other words, the same operation as when "0" is set is performed even if "1" is written to this bit.

6.5.6 EP1RXCNT/EP1STAT Register (34Ch), EP2RXCNT/EP2STAT Register (350h)

Bits	Symbol	Description	Reset	USB Reset	R/W
31:16	—	Don't care	X	X	X
15:08	EP1RXCNT (for EP1) EP2RXCNT (for EP2)	Counts the number of bytes of the received packet to EP1/EP2, and shows its value. For more information, refer to the descriptions of the EP1 and EP2 receive byte count registers in the ML60852A Data Sheet.	00h	00h	R
07:02	—	Reserved (write "0" at the time of write operation.)	00h	00h	R/W
01	EP1TXRDY (for EP1) EP2TXRDY (for EP2)	This bit is valid only when the EP1/EP2 has been set for bulk or INT transfer. This indicates whether or not valid data has been stored in the FIFOs inside the ML60842. For more information, see [Description] below.	0b	0b	R/W
00	EP1RXRDY (for EP1) EP2RXRDY (for EP2)	This bit is valid only when the EP1/EP2 has been set for bulk or INT transfer. This indicates whether or not valid data has been stored in a FIFO inside the ML60842. For more information, refer to the descriptions of the receive packet ready bits of the EP1 and EP2 status registers in the ML60852A Data Sheet.	0b	0b	R/W

Note 1: Only the contents of the EP1TXRDY and EP2TXRDY bits are different from the contents described in the ML60852A Data Sheet.
For more information about the bits other than the EP1TXRDY and EP2TXRDY bits, refer to the ML60852A Data Sheet.

Note 2: Write "0" to the EP1RXRDY and EP2RXRDYb bits when writing to the EP1TXRDY and EP2TXRDY bits, and to the EP1TXRDY and EP2TXRDY bits when writing to the EP1RXRDY and EP2RXRDYb bits. If a value other than "0" is written, correct operation cannot be guaranteed.

[Description]
Both the EP1TXRDY and EP2TXRDY bits can be read and set. These bits can be set to "1" by writing "1" to them. The following shows the assert/deassert conditions of these bits. The EP1/EP2 has a double-sided (sides A and B) FIFO.
There is a separate transmit packet ready bit for each of sides A and B, and these two sides are automatically switched by the ML60842.

	Condition	Operation
Assert	When the microcontroller sets the bits for both sides A and B	Transmission from the EP1/EP2 can be performed (data transmission for an IN token) when either side A or B has been asserted.
Deassert	When an ACK has been received from the host for the transmit data of either side A or B	The EP1/EP2 is locked (a NACK is replied for an IN token) when the transmit data of both sides A and B is not ready.

Specific examples are given below.

		Side A of FIFO (64B)	Side B of FIFO (64B)	Side A of FIFO packet ready bit	Side B of FIFO packet ready bit	EP1/EP2 transmit packet ready bit
1	Both sides A and B of FIFO are empty.			×	×	×
2	The microcontroller writes data to side A of FIFO.			×	×	×
3	Writing one packet data is complete.			√	×	×
4	Transmitting the side A data of FIFO to the USB and writing the next packet data to side B of FIFO.			√	×	×
5a	When writing data to side B of FIFO has been completed before side A of FIFO is emptied			√	√	√
5b	When writing data to side A of FIFO has been completed before side B of FIFO is emptied			×	×	×
6	From 5a: Side A of FIFO is emptied. From 5b: Side B of FIFO is full.			×	√	√
7	The transmission of the side B data of FIFO to the USB bus has started.			×	√	×

√: Assert, ×: Deassert

6.5.7 EP4RXCNT/EP4STAT Register (358h), EP5RXCNT/EP5STAT Register (35Ch)

Bits	Symbol	Description	Reset	USB Reset	R/W
31:16	EP4RXCNT (for EP4) EP5RXCNT (for EP5)	Counts the number of bytes of the received packet to EP4/EP5, and shows its value. For more information, refer to the descriptions of the EP4 and EP5 receive byte count registers in the ML60852A Data Sheet.	00h	00h	R
15:8	—	Don't care	X	X	X
07	EP4PREFMST (for EP4) EP5PREFMST (for EP5)	This bit is valid only when the EP4/EP5 has been set for ISO IN transfer. This bit indicates whether an IN token for this EP has been transmitted from the host in just previous frame. 0: An IN token for this EP has not been transmitted in just previous frame. 1: An IN token for this EP has been transmitted in just previous frame. For more information, see [Description] below.	00h	00h	R
06:02	—	Reserved (write "0" at the time of write operation.)	00h	00h	R/W
01	EP4TXRDY (for EP4) EP5TXRDY (for EP5)	This bit is valid only when EP4/EP5 has been set for bulk or INT transfer. This indicates whether or not valid data has been stored in the FIFOs inside the ML60842. For more information, see [Description] below.	0b	0b	R/W
00	EP4RXRDY (for EP4) EP5RXRDY (for EP5)	This bit is valid only when EP4/EP5 has been set for bulk or INT transfer. This indicates whether or not valid data has been stored in a FIFO inside the ML60842. For more information, refer to the descriptions of the receive packet ready bits of the EP4 and EP5 status registers in the ML60852A Data Sheet.	0b	0b	R/W

Note 1: Only the contents of EP4PREFMST, EP5PREFMST, EP4TXRDY, and EP5TXRDY bits are different from the contents described in the ML60852A Data Sheet. For more information about the bits other than the EP4PREFMST, EP5PREFMST, EP4TXRDY, and EP5TXRDY bits, refer to the ML60852A Data Sheet.

Note 2: Write "0" to the EP4RXRDY and EP5RXRDYb bits when writing to the EP4TXRDY and EP5TXRDY bits, and to the EP4TXRDY and EP5TXRDY bits when writing to the EP4RXRDY and EP5RXRDYb bits. If a value other than "0" is written, correct operation cannot be guaranteed.

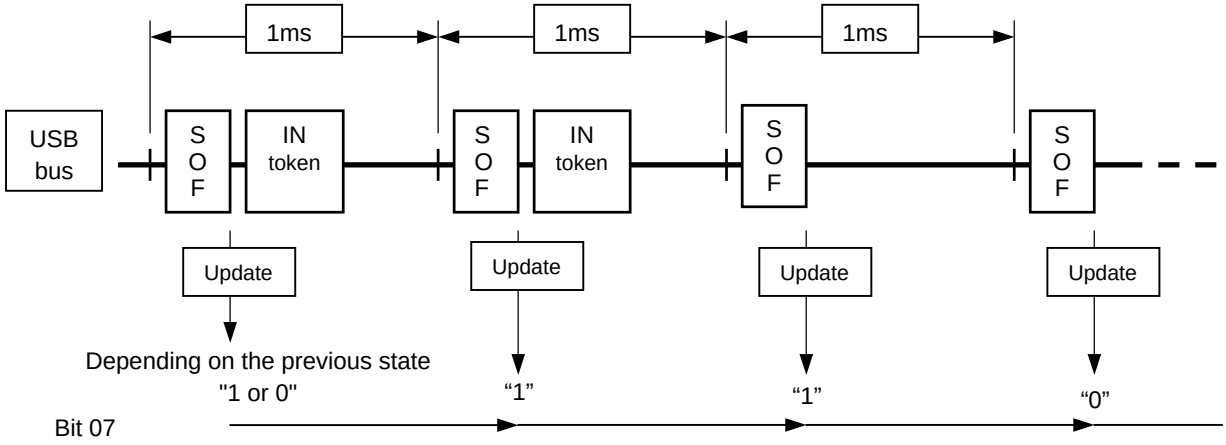
[Description]

The EP4PREFMST and EP5PREFMST bits are valid only if the EP4 and EP5 have been configured in ISO IN, respectively. If they are configured in other than ISO IN, they will be undefined.

When the ML60842 detects an SOF, it judges whether or not an IN token for this EP has been transmitted from the host in the immediately previous frame and then updates the value of this bit.

- If an IN token for this EP has been transmitted: This bit is updated to "1."
- If an IN token for this EP has not been transmitted: This bit is updated to "0."

Therefore, the microcontroller can know the correct status of the immediately previous frame by reading this bit after an SOF interrupt. For detailed timings, see the figure below.



For more information about how to use the EP4PREFMST/EP5PREFMST bits, see Section 7.8, "Precautions for Peripheral Control."

Both the EP4TXRDY and EP5TXRDY bits can be read and set. These bits can be set to "1" by writing "1" to them. The following shows the assert/deassert conditions of these bits. The EP4/EP5 has a double-sided (sides A and B) FIFO.
There is a separate transmit packet ready bit for each of sides A and B, and these two sides are automatically switched by the ML60842.

	Condition	Operation
Assert	When the microcontroller sets the bits for both sides A and B.	Transmission from the EP4/EP5 can be performed (data transmission for an IN token) when either side A or B has been asserted.
Deassert	When an ACK has been received from the host for the transmit data of either side A or B	The EP4/EP5 is locked (a NACK is replied for an IN token) when the transmit data of both sides A and B is not ready.

Specific examples are given below.

		Side A of FIFO (64B)	Side B of FIFO (64B)	Side A of FIFO packet ready bit	Side B of FIFO packet ready bit	EP4/EP5 transmit packet ready bit
1	Both sides A and B of FIFO are empty.			×	×	×
2	The microcontroller writes data to side A of FIFO.			×	×	×
3	Writing one packet data is complete.			√	×	×
4	Transmitting the side A data of FIFO to the USB and writing the next packet data to side B of FIFO.			√	×	×
5a	When writing data to side B of FIFO has been completed before side A of FIFO is emptied			√	√	√
5b	When writing data to side A of FIFO has been completed before side B of FIFO is emptied			×	×	×
6	From 5a: Side A of FIFO is emptied. From 5b: Side B of FIFO is full.			×	√	×
7	The transmission of the side B data of FIFO to the USB bus has started.			×	√	×

√: Assert, ×: Deassert

6.5.8 EP0TXCNT Register (360h)

Bits	Symbol	Description	Reset	USB Reset	R/W
31:06	—	Don't care	X	X	X
05:00	EP0TXCNT	EP0TFCnt[5:0]	0h	0h	R/W

[Description]
Transmitting invalid data can be suppressed by setting the number of bytes that should be sent per packet ("01h" in the case of 1 byte) in this register.
It is not necessary to set this register every time if packets with the same number of bytes are to be sent (as the previously set value is retained).
When in PIO mode, write the number of data bytes to be sent to this register, write data to the FIFO for packet data transfer, and then set the transmit PKTRDY bit to "1."

6.5.9 EP1TXCNT Register (364h)

Bits	Symbol	Description	Reset	USB Reset	R/W
31:07	—	Don't care	X	X	X
06:00	EP1TXCNT	EP1TFCnt[6:0]	0h	0h	R/W

[Description]
Transmitting invalid data can be suppressed by setting the number of bytes that should be sent per packet ("01h" in the case of 1 byte) in this register.
It is not necessary to set this register every time if packets with the same number of bytes are to be sent (as the previously set value is retained).
When in PIO mode, write the number of data bytes to be sent to this register, write data to the FIFO for packet data transfer, and then set the transmit PKTRDY bit to "1."
When in DMA mode, write the number of data bytes to be sent to this register, and then write data to the FIFO.
For more information about how to use the EP1TXCNT register, see Section 7.8, "Precautions for Peripheral Control."

6.5.10 EP2TXCNT Register (368h)

Bits	Symbol	Description	Reset	USB Reset	R/W
31:07	—	Don't care	X	X	X
06:00	EP2TXCNT	EP2TFCnt[6:0]	0h	0h	R/W

[Description]
Transmitting invalid data can be suppressed by setting the number of bytes that should be sent per packet ("01h" in the case of 1 byte) in this register.
It is not necessary to set this register every time if packets with the same number of bytes are to be sent (as the previously set value is retained).
When in PIO mode, write the number of data bytes to be sent to this register, write data to the FIFO for packet data transfer, and then set the transmit PKTRDY bit to "1."
When in DMA mode, write the number of data bytes to be sent to this register, and then write data to the FIFO.
For more information about how to use the EP2TXCNT register, see Section 7.8, "Precautions for Peripheral Control."

6.5.11 EP3TXCNT Register (36Ch)

Bits	Symbol	Description	Reset	USB Reset	R/W
31:06	—	Don't care	X	X	X
05:00	EP3TXCNT	EP3TFCnt[5:0]	0h	0h	R/W

[Description]
Transmitting invalid data can be suppressed by setting the number of bytes that should be sent per packet ("01h" in the case of 1 byte) in this register.
It is not necessary to set this register every time if packets with the same number of bytes are to be sent (as the previously set value is retained).
When in PIO mode, write the number of data bytes to be sent to this register, write data to the FIFO for packet data transfer, and then set the transmit PKTRDY bit to "1."

6.5.12 EP4TXCNT Register (370h)

Bits	Symbol	Description	Reset	USB Reset	R/W
31:10	—	Don't care	X	X	X
09:08	EP4TXCNT MSB	EP4TFCntMSB[1:0]	0h	0h	R/W
07:00	EP4TXCNT LSB	EP4TFCntLSB[7:0]	0h	0h	R/W

[Description]
Transmitting invalid data can be suppressed by setting the number of bytes that should be sent per packet ("01h" in the case of 1 byte) in this register.
It is not necessary to set this register every time if packets with the same number of bytes are to be sent (as the previously set value is retained).
When in PIO mode, write the number of data bytes to be sent to this register, write data to the FIFO for packet data transfer, and then set the transmit PKTRDY bit to "1."
When in DMA mode, write the number of data bytes to be sent to this register, and then write data to the FIFO.
For more information about how to use the EP4TXCNT register, see Section 7.8, "Precautions for Peripheral Control."

6.5.13 EP5TXCNT Register (374h)

Bits	Symbol	Description	Reset	USB Reset	R/W
31:09	—	Don't care	X	X	X
08	EP5TXCNT MSB	EP5TFCntMSB[0]	0b	0b	R/W
07:00	EP5TXCNT LSB	EP5TFCntLSB[7:0]	0h	0h	R/W

[Description]
Transmitting invalid data can be suppressed by setting the number of bytes that should be sent per packet ("01h" in the case of 1 byte) in this register.
It is not necessary to set this register every time if packets with the same number of bytes are to be sent (as the previously set value is retained).
When in PIO mode, write the number of data bytes to be sent to this register, write data to the FIFO for packet data transfer, and then set the transmit PKTRDY bit to "1."
When in DMA mode, write the number of data bytes to be sent to this register, and then write data to the FIFO.
For more information about how to use the EP5TXCNT register, see Section 7.8, "Precautions for Peripheral Control."

7. PRECAUTIONS FOR CONTROLLING THE ML60842

7.1 Session Request Protocol (SRP) Control

In SRP control, the following operations, broadly categorized, are required.

- Detection of the initial state (operation of device B)
- Execution of data line pulsing (operation of device B)
- Execution of VBUS pulsing (operation of device B)
- Detection of VBUS pulsing (operation of device A)

The following describes the control procedure for each of the SRP control items above.

(1) Detection of the Initial State

Device B must check the following two items when starting the SRP.

- VBUS is less than 0.8 V.
- Both D+ and D- are at "low" level at least 2 ms (corresponding to b_se0_srp).

The ML60842 can detect the two items above using the following procedure.

<Detecting that VBUS is less than 0.8 V>

① Verify that the ABSESSVLDST bit of the OTGIntStt register is "0" (corresponding to b_sess_vld/).
② Set the DISCHRGVBUS bit of the OTGCtl register to "1" and start VBUS discharge.
③ Set the DISCHRGVBUS bit of the OTGCtl register to "0" and end VBUS discharge.

The ML60842 has a pull-down resistor of TBD (1 kΩ) that is connected to the SVBUS pin. VBUS can be pulled down by setting the DISCHRGVBUS bit of the OTGCtl register to "1". Also, this pull-down can be cleared by setting the DISCHRGVBUS bit to "0".

<Detecting that both D+ and D- are at "low" level (SE0) at least 2 ms>

① Set the BSE0SRPDETENB bit of the OTGCtl register to "1" and start the timer to measure the SE0 state.
② If the SE0 state continues at least 2 ms, the BSE0SRPDETST bit of the OTGIntStt register is set to "1."

(2) Executing Data Line Pulsing

To execute data line pulsing, it is necessary to increase the voltage of the D+ line to the specified level (2.7 V) or higher via a pull-up resistor.

The ML60842 has a resistor of TBD (X kΩ) that is connected to the D+ pin. VBUS can be pulled up by setting the PUCTLDP bit of the OTGCtl register in the common block to "1". Also, this pull-up can be cleared by setting the PUCTLDP bit to "0".

Therefore, the microcontroller can execute data line pulsing by controlling the time when setting the PUCTLDP bit to "1" and increasing the voltage of the D+ line to the specified level.

(3) Controlling the Execution of VBUS Pulsing

To execute VBUS pulsing, it is necessary to increase the voltage of VBUS to the specified level (*) via a pull-up resistor.

The ML60842 has a pull-up resistor of TBD (1 kΩ) that is connected to the SVBUS pin. VBUS can be pulled up by setting the CHRGVBUS bit of the OTGCtl register to "1". Also, this pull-up can be cleared by setting the CHRGVBUS bit to "0".

Therefore, the microcontroller can execute VBUS pulsing by controlling the time when setting the CHRGVBUS bit to "1" and increasing the voltage of VBUS to the specified level.

(*) The specified voltage is defined as follows:
2.1 V or more when connected to a Dual-Role-Device (1.0 μF < VBUS capacity (Cdrd_vbus)< 6.5 μF), in other words, at 13 μF (2 × Cdrd_vbus max), and less than 2.0 V when connected to a standard host (VBUS capacity (Chst_vbus) > 9 6 μF), in other words, at 97 μF (Chst_vbus min + Cdrd_vbus min)

(4) Controlling the Detection of VBUS Pulsing

Device A must be able to detect either one of the following two states in the idle state:

- Detection of data line pulsing
- Detection of VBUS pulsing

The ML60842 can detect VBUS pulsing by referring to the ABSESSVLDST bit of the OTGIntStt register in the idle state.

7.2 Host Negotiation Protocol (HNP) Control

The Host Negotiation Protocol (HNP) refers to a procedure in which device A and device B switch roles (device A is the peripheral device and device B is the host) from their default states (device A is the host and device B is the peripheral device), execute a transaction, and then return to the default states again.

It is necessary to execute device state transition according to the following procedure:

- Transition from a_host to a_suspend (operation of device A)
- Transition from b_peripheral to b_wait_acon (operation of device B)
- Transition from a_suspend to a_peripheral (operation of device A)
- Transition from b_wait_acon to b_host (operation of device B)
- Transition from a_ peripheral to a_wait_bcon (operation of device A)
- Transition from b_ host to b_ peripheral (operation of device B)
- Transition from a_wait_bcon to a_host (operation of device A)

The following describes the control procedure for each of the state transitions above.

(1) Transition from a_host to a_suspend

Device A must check the following two requirements when starting the HNP:

- Device B to which device A is connected supports the HNP.
- b_hnp_enablem which is an internal variable of device B is enabled.

Device A can check the two requirements above by executing the GetDescriptor and SetFeature commands. After checking the two requirements above, write "11b" (USB suspend) to the HCFS bits of the HcControl register in the OHCI block.

(2) Transition from b_peripheral to b_wait_acon

① Verify that the USBSUS bit of the INTSTAT2 register in the peripheral block is "1" (corresponding to a_bus_suspend).
② Set the PUCTLDP bit of the OTGCtl register in the common block to "0" (clearing pull-up of the D+ signal).
③ Set the PDCTLDP bit of the OTGCtl register in the common block to "1" (pulling down the D+ signal).
④ Set the MODE bit of the HostPeriSel register in the common block to "0" (host setting).
⑤ Wait until the BUSY bit of the HostPeriSel register is set to "0."
⑥ Set the HCFS bits of the HcControl register in the OHCI block to "11b" (USB suspend).

[Note] Be sure to insert a process to set the HCFS bits to "10b (USB operational)" immediately before setting the HCFS bits of the HcControl register in the OHCI block to "11b (USB suspend)". (This is because a process to directly change the HCFS bits from their initial state of "00b (USB reset)" to "11b (USB suspend)" is out of guarantee.)

(3) Transition from a_suspend to a_peripheral

① Verify that the CCS bit of the HcRhPortStatus register in the OHCI block is "0" (corresponding to b_conn/).
② Set the VBUSMODE bits and the DRVVBUS bit of the OTGCtl register in the common block to "10" and "1", respectively.
(It is aimed to continue "L" output from the -PCONT pin even after switching to peripheral settings.)
③ Set the MODE bit of the HostPeriSel register in the common block to "1" (peripheral setting).
④ Wait until the BUSY bit of the HostPeriSel register is set to "0."
⑤ Set the PUCTLDP bit of the OTGCtl register in the common block to "1" (pull-up of the D+ signal).
⑥ Set the PUCTLDP bit of the OTGCtl register in the common block to "0" (clearing pull-down of the D+ signal).

[Note] The pull-down of the D- signal is not cleared in step ⑥ above (in accordance with Section 5.1.6 of the OTG Standard).

(4) Transition from b_wait_acon to b_host
① Verify that the CCS bit of the HcRhPortStatus register in the OHCI block is "1" (corresponding to a_conn/).
② Set the HCFS bits of the HcControl register in the OHCI block to "10b" (USB operational).
③ Execute a transaction using device A as the peripheral and device B as the host.
④ Upon completion of processing ③ above (corresponding to b_bus_req/), set the HCFS bits of the HcControl register in the OHCI block to "11b" (USB suspend).

(5) Transition from a_ peripheral to a_wait_bcon
① Verify that the USBSUS bit of the INTSTAT2 register in the peripheral block is "1" (corresponding to a_bus_suspend).
② Set the PUCTLDP bit of the OTGCtl register in the common block to "0" (clearing pull-up of the D+ signal).
③ Set the PDCTLDP bit of the OTGCtl register in the common block to "1" (pulling down the D+ signal).
④ Set the MODE bit of the HostPeriSel register in the common block to "0" (host setting).
⑤ Wait until the BUSY bit of the HostPeriSel register is set to "0."
⑥ Set the LPSC bit of the HcRhStatus register in the OHCI block to "1" (-PCONT pin at "L").
(At that time, the PPS bit of the HcRhPortStatus register is set to "1 (port power ON)".)
⑦ Set the VBUSMODE bits and the DRVVBUS bit of the OTGCtl register in the common block to "00" and "0", respectively.
(It is aimed to return the control of -PCONT pin output to the PPS.)

(6) Transition from b_ host to b_ peripheral
① Verify that the CCS bit of the HcRhPortStatus register in the OHCI block is "0" (corresponding to a_conn/).
② Set the MODE bit of the HostPeriSel register in the common block to "1" (peripheral setting).
③ Wait until the BUSY bit of the HostPeriSel register is set to "0."
④ Set the PUCTLDP bit of the OTGCtl register in the common block to "1" (pull-up of the D+ signal).
⑤ Set the PDCTLDP bit of the OTGCtl register in the common block to "0" (clearing pull-down of the D+ signal).

(7) Transition from a_wait_bcon to a_host
① Verify that the CCS bit of the HcRhPortStatus register in the OHCI block is "1" (corresponding to b_conn/).
② Set the HCFS bits of the HcControl register in the OHCI block to "10b" (USB operational).

In the control procedure above, the control of the interrupt mask bit is omitted.

Be sure to control device B in such a way that the output of the -PCONT pin is always "H" (state where VBUS is not driven).
In other words, set the VBUSMODE bits and the DRVVBUS bit of the OTGCtl register to "10" and "0", respectively.

7.3 Power Down Control

When "1" is written to the XSTOP and CLKSTOP bits of the RstClkCtl register, the ML60842 executes power down processing internally and is placed in the power down state. In the power down state, the following processes are performed:

- The oscillation circuit (XIN and XOUT pins) is disabled (when "1" is written to the XSTOP bit).
- Clock supply to the internal circuits of the ML60842 is stopped (when "1" is written to the CLKSTOP bit).
- The clock for synchronizing the WAIT signal (WSYNC_CLK pin) is disabled.
- The USB transceiver, excluding the receiver unit, is disabled.
  (Whether the receiver unit is enabled or disabled depends on the setting of the USBRCVENB bit of the OTGCtl register.)
- The suspend state signal is output to the external USB transceiver ("H" is output to the SUSPEND pin).
- Only the registers in the common block can be accessed; it is not possible to access other blocks (host controller block (registers/memory) and peripheral controller block).
- The -WAIT1:0 pin is fixed at "H" output.

[To cancel the power down state, write "0" to the XSTOP and CLKSTOP bits of the RstClkCtl register.]

The ML60842 can move to the power down state above while maintaining the required specification (functions to detect changes in the ID pin and VBUS) when it is in the "a_idle" or "b_idle" state defined in the OTG Specification.

(1) Procedure for Executing Power Down/Canceling Power Down in the a_idle State

① Verify that the ABSESSVLDST bit of the OTGIntStt register is "0."
② By writing "1" to the CLKSTOP bit of the RstClkCtl register, instruct to stop supplying the clock to the internal circuits.
③ Read the CLKSTOP bit of the RstClkCtl register and wait until the clock stop processing completes ("1").
④ By writing "1" to the XSTOP bit of the RstClkCtl register, instruct to stop the oscillation circuit.
⑤ Read the XSTOP bit of the RstClkCtl register and wait until the oscillation circuit stop processing completes ("1").
[By performing processing steps ① to ⑤ above, the ML60842 is placed in the power down state.]
⑥ An interrupt is generated when the state of the ID pin changes or "voltage of VBUS > threshold voltage of AB_SESSION_VALID" (corresponding to the VBUS pulse of the SRP) is detected, and the IDSELCHG or ABSESSVLDCHG bit of the OTGIntStt register is set to "1."
[When the state described in ⑥ above is detected, it is necessary to cancel the power down state of the ML60842 (i.e., changing to the power up state).]
⑦ By writing "0" to the XSTOP bit of the RstClkCtl register, instruct to cancel the stop state of the oscillation circuit.
⑧ Read the XSTOP bit of the RstClkCtl register and wait until the oscillation circuit resume processing completes ("0").
⑨ By writing "0" to the CLKSTOP bit of the RstClkCtl register, instruct to resume supplying the clock to the internal circuits after the output of the oscillation circuit stabilizes.
⑩ Read the CLKSTOP bit of the RstClkCtl register and wait until the clock resume processing completes ("0").
[By performing processing steps ⑦ to ⑩ above, the ML60842 is placed in the power down canceled state (i.e., power up state).]

(2) Procedure for Executing Power Down/Canceling Power Down in the b_idle State

① Verify that the ABSESSVLDST bit of the OTGIntStt register is "0."

② Writing "1" to the CLKSTOP bit of the RstClkCtl register, instruct to stop supplying the clock to the internal circuits.

③ Read the CLKSTOP bit of the RstClkCtl register and wait until the clock stop processing completes ("1").

④ By writing "1" to the XSTOP bit of the RstClkCtl register, instruct to stop the oscillation circuit.

⑤ Read the XSTOP bit of the RstClkCtl register and wait until the oscillation circuit stop processing completes ("1").

[By performing processing steps ① to ⑤ above, the ML60842 is placed in the power down state.]

⑥ An interrupt is generated when the state of the ID pin changes or "voltage of VBUS > threshold voltage of AB_SESSION_VALID" (corresponding to b_sess_vld) is detected, and the IDSELCHG or ABSESSVLDCHG bit of the OTGIntStt register is set to "1."

[When the state described in ⑥ above is detected, it is necessary to cancel the power down state of the ML60842 (i.e., changing to the power up state).]

⑦ By writing "0" to the XSTOP bit of the RstClkCtl register, instruct to cancel the power down state.

⑧ Read the XSTOP bit of the RstClkCtl register and wait until the oscillation circuit resume processing completes ("0").

⑨ By writing "0" to the CLKSTOP bit of the RstClkCtl register, instruct to resume supplying the clock to the internal circuits after the output of the oscillation circuit stabilizes.

⑩ Read the CLKSTOP bit of the RstClkCtl register and wait until the clock resume processing completes ("0").

[By performing processing steps ⑦ to ⑩ above, the ML60842 is placed in the power down canceled state (i.e., power up state).]

After the power down state is canceled, the ML60842 retains the register settings prior to power down. Therefore, it is not necessary for the microcontroller to perform register re-setting processing.

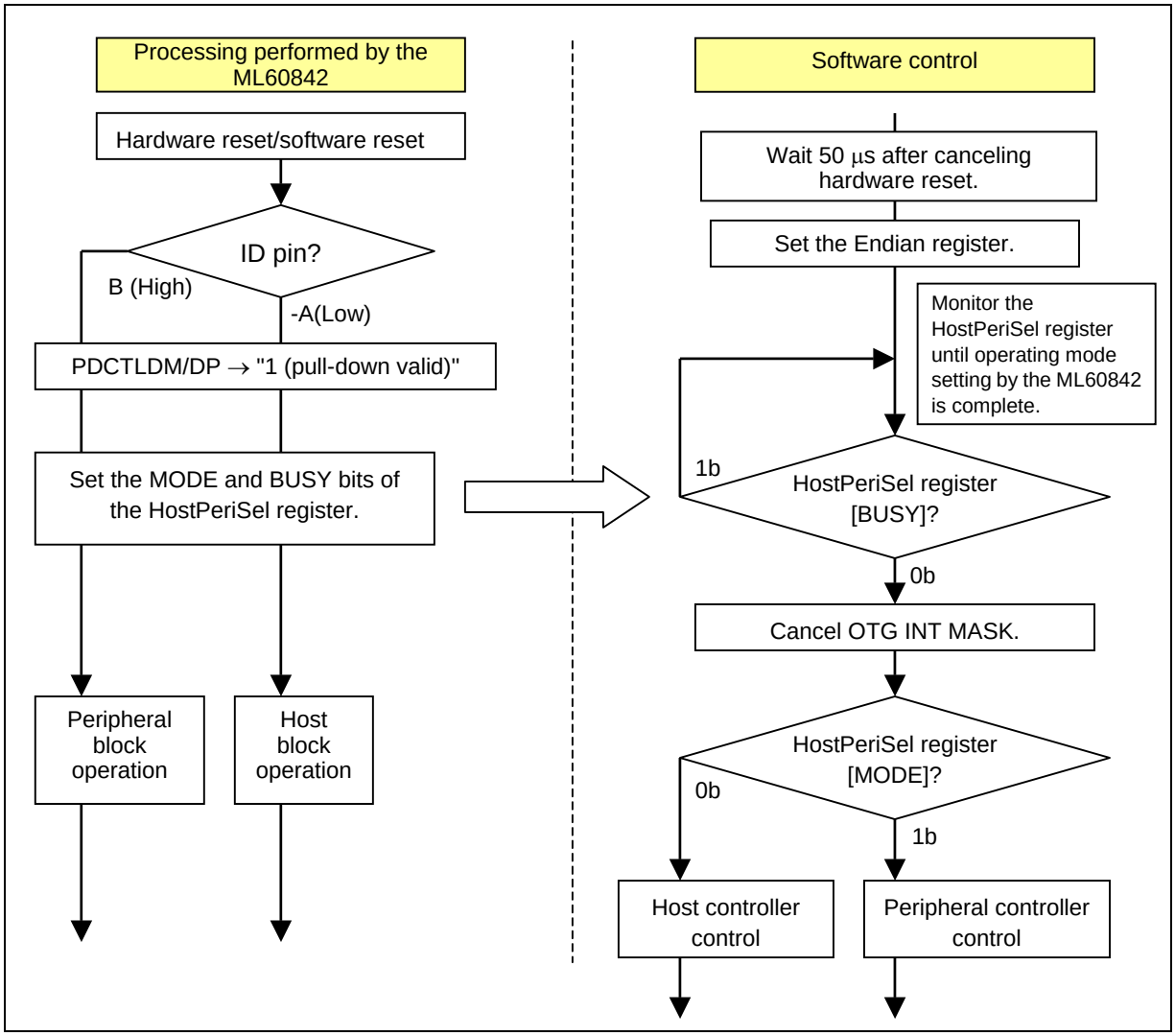
7.4 Host/Peripheral Setting Control

The ML60842 sets the host/peripheral operating mode according to the state of the ID pin at the time of reset or the value written to the MODE bit of the HostPeriSel register. Therefore, the microcontroller must stand by until this setting completes. Once an operating mode is set, correct operation is guaranteed only for writing to the registers that correspond to the operating mode.

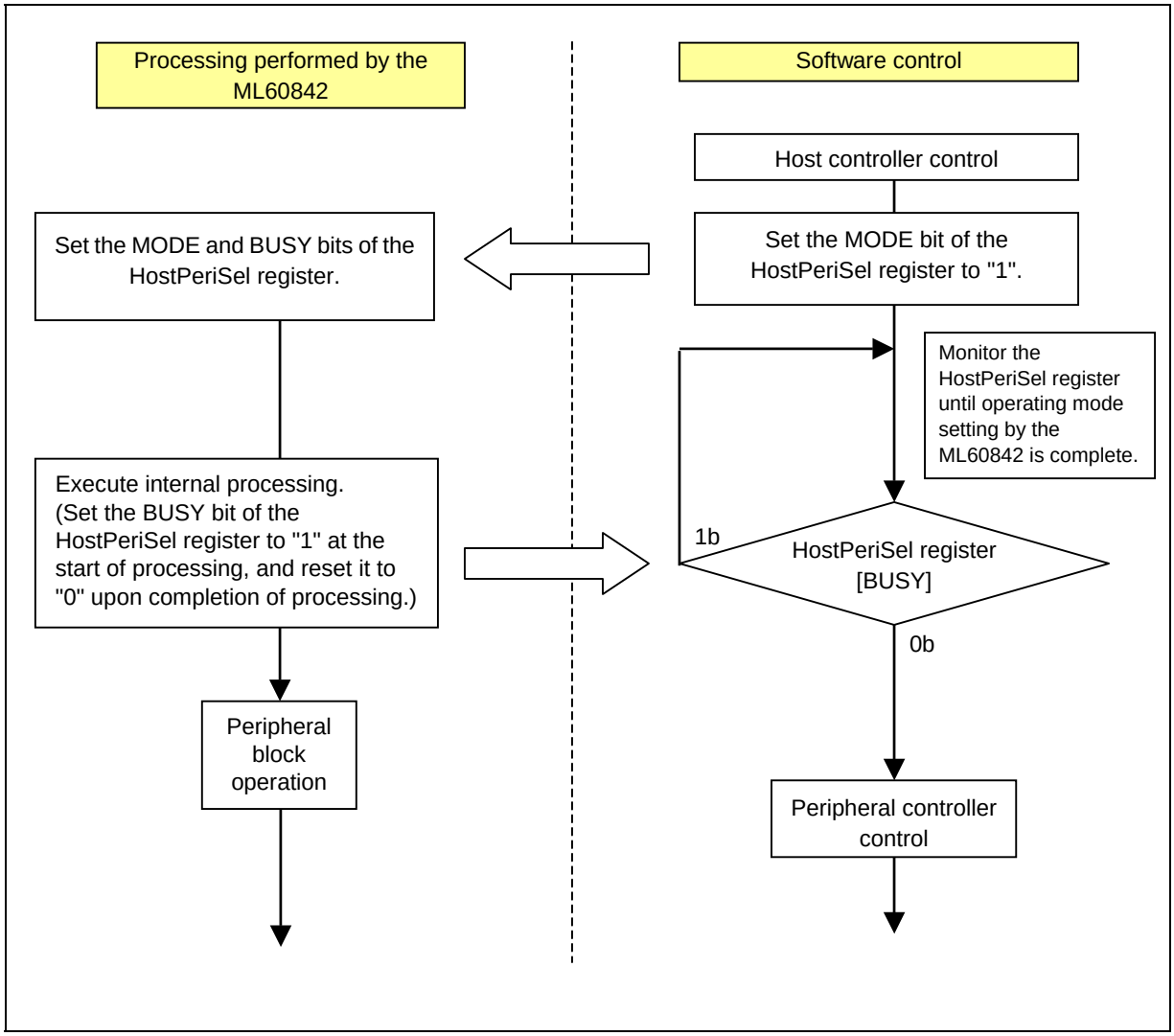
Note that the ML60842 is designed to reduce the supply current by stopping the clock supply to the peripheral control block when it is set to be the host and to the host control block when it is set to be the peripheral device.

The following flowcharts show the software control procedures for setting the host/peripheral operating mode.

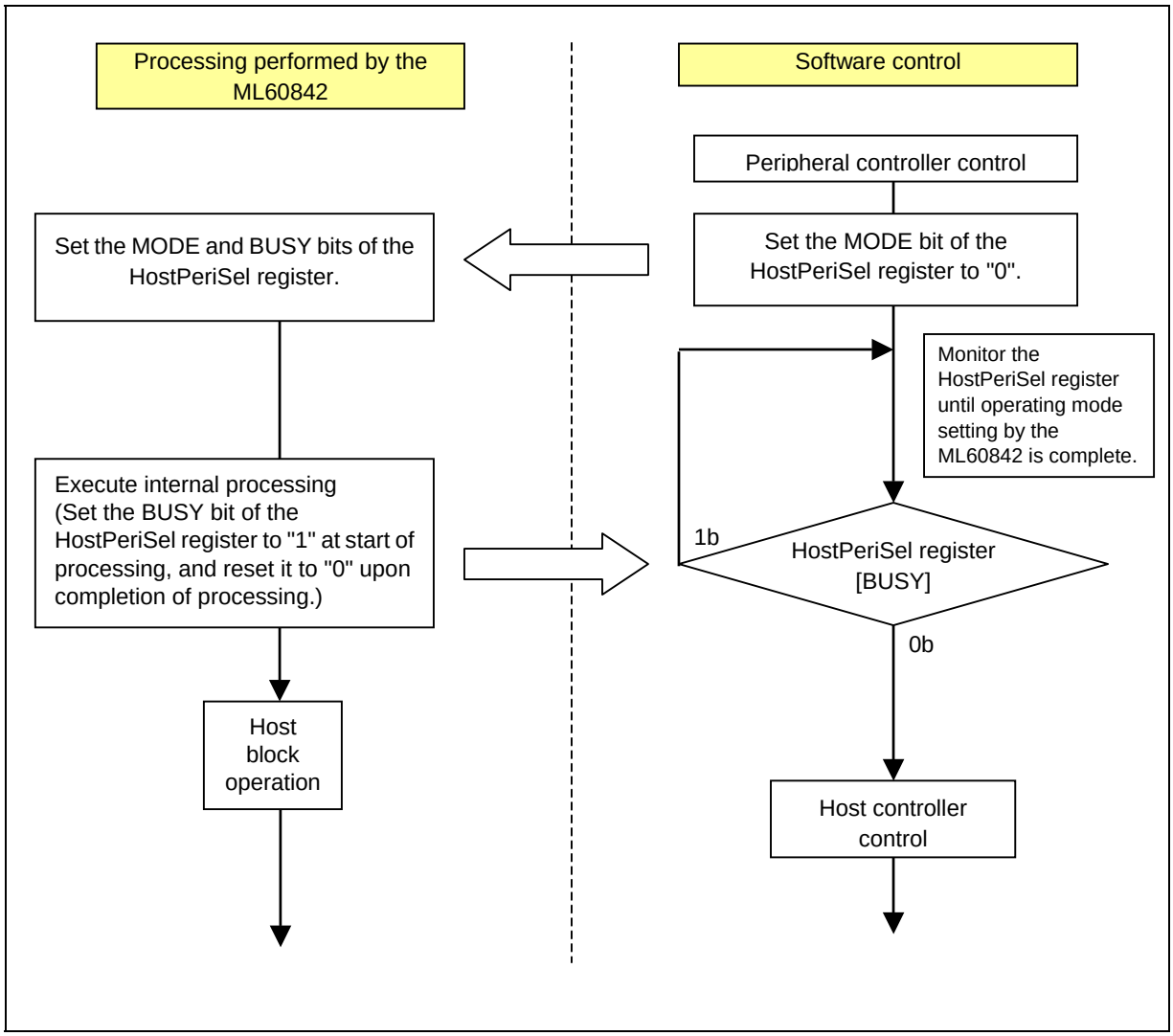
(1) Hardware Reset/Software Reset of the Entire Chip



(2) Transition from Host Operating Mode to Peripheral Operating Mode



(3) Transition from Peripheral Operating Mode to Host Operating Mode



7.5 Data Alignment (Endian Conversion Operation)

The ML60842 has the big endian/little endian conversion function as a data alignment function.
Big endian/little endian is specified by the ENDIAN3, 2, 1, and 0 bits of the Endian register.
Also, two type of conversion methods can be specified by the BigEdanMod pin if big endian is specified by the ENDIAN3, 2, 1, and 0 bits of the Endian register and the access target is the internal RAM (if the access target is a register or FIFO, the state of the BigEdanMod pin is ignored).

B3h, B2h, B1h, and B0h in the table below indicate the values that should be written to each "8-bit part" assigned to bits 31:24, bits 23:16, bits 15:8, and bits 7:0 of the 32-bit registers, FIFOs, or internal RAM listed in the specifications.
When accessing a FIFO, data is transmitted from the USB interface in the order of B0h, B1h, B2h, and then B3h.
When accessing the internal RAM, the addresses of the data storage destination are incremented in the order of B0h, B1h, B2h, and then B3h if referenced from the host core side.

<Little endian conversion operation (common to all accesses to the registers, FIFOs, and internal RAM)>
The following table lists the data alignment in little endian (when the ENDIAN3, 2, 1, and 0 bits of the Endian register are all "0") using a write operation as an example.
However, note that the FIFOs can only be accessed in the bit width units specified by DBWidth0:1 (for example, it is not allowed to perform 8-bit access in 16-bit width mode).

DBWidth1:0	A1:A0	D31:D24	D23:D16	AD15:AD8	AD7:AD0	-WR3:-WR0	Remarks
“L:L” (16-bit width)	0:X	—	—	B1h	B0h	-WR1:-WR0=‘L’	
	1:X	—	—	B3h	B2h	-WR1:-WR0=‘L’	
	0:X	—	—	Don’t Care	B0h	-WR1=‘H’ -WR0=‘L’	
	0:X	—	—	B1h	Don’t Care	-WR1=‘L’ -WR0=‘H’	
	1:X	—	—	Don’t Care	B2h	-WR1=‘H’ -WR0=‘L’	
	1:X	—	—	B3h	Don’t Care	-WR1=‘L’ -WR0=‘H’	
“L:H” (8-bit width)	0:0	—	—	—	B0h	-WR0=‘L’	
	0:1	—	—	—	B1h	-WR0=‘L’	
	1:0	—	—	—	B2h	-WR0=‘L’	
	1:1	—	—	—	B3h	-WR0=‘L’	

As for read operations, valid data is output to the byte lanes not indicated by "—" in the table above.

<Big endian conversion operation when accessing the registers>
The following table lists the data alignment in big endian (when one of the ENDIAN3, 2, 1, and 0 bits of the Endian register is "1") using a write operation as an example.

DBWidth1:0	A1:A0	D31:D24	D23:D16	AD15:AD8	AD7:AD0	-WR3:-WR0	Remarks
"L:L" (16-bit width)	0:X	—	—	B3h	B2h	-WR1:-WR0='L'	
	1:X	—	—	B1h	B0h	-WR1:-WR0='L'	
	0:X	—	—	B3h	Don't Care	-WR1='L' -WR0='H'	
	0:X	—	—	Don't Care	B2h	-WR1='H' -WR0='L'	
	1:X	—	—	B1h	Don't Care	-WR1='L' -WR0='H'	
	1:X	—	—	Don't Care	B0h	-WR1='H' -WR0='L'	
"L:H" (8-bit width)	0:0	—	—	—	B3h	-WR0='L'	
	0:1	—	—	—	B2h	-WR0='L'	
	1:0	—	—	—	B1h	-WR0='L'	
	1:1	—	—	—	B0h	-WR0='L'	

As for read operations, valid data is output to the byte lanes not indicated by "—" in the table above.

<Big endian conversion operation when accessing the FIFOs>
The following table lists the data alignment in big endian (when one of the ENDIAN3, 2, 1, and 0 bits of the Endian register is "1") using a write operation as an example.
However, note that the FIFOs can only be accessed in the bit width units specified by DBWidth0:1 (for example, it is not allowed to perform 8-bit access in 16-bit width mode).

DBWidth1:0	A1:A0	D31:D24	D23:D16	AD15:AD8	AD7:AD0	-WR3:-WR0	Remarks
"L:L" (16-bit width)	X:X	—	—	B0h	B1h	-WR1:-WR0='L'	
	X:X	—	—	B2h	B3h	-WR1:-WR0='L'	
"L:H" (8-bit width)	X:X	—	—	—	B0h	-WR0='L'	
	X:X	—	—	—	B1h	-WR0='L'	
	X:X	—	—	—	B2h	-WR0='L'	
	X:X	—	—	—	B3h	-WR0='L'	

As for read operations, valid data is output to the byte lanes not indicated by "—" in the table above.

<Big endian conversion operation when accessing the internal RAM and BigEdanMod pin = "L">
The following table lists the data alignment in big endian (when one of the ENDIAN3, 2, 1, and 0 bits of the Endian register is "1") and BigEdanMod pin = "L" using a write operation as an example.

DBWidth1:0	A1:A0	D31:D24	D23:D16	AD15:AD8	AD7:AD0	-WR3:-WR0	Remarks
"L:L" (16-bit width)	0:X	—	—	B0h	B1h	-WR1:-WR0='L'	
	1:X	—	—	B2h	B3h	-WR1:-WR0='L'	
	0:X	—	—	B0h	Don't Care	-WR1='L' -WR0='H'	
	0:X	—	—	Don't Care	B1h	-WR1='H' -WR0='L'	
	1:X	—	—	B2h	Don't Care	-WR1='L' -WR0='H'	
	1:X	—	—	Don't Care	B3h	-WR1='H' -WR0='L'	
"L:H" (8-bit width)	0:0	—	—	—	B0h	-WR0='L'	
	0:1	—	—	—	B1h	-WR0='L'	
	1:0	—	—	—	B2h	-WR0='L'	
	1:1	—	—	—	B3h	-WR0='L'	

As for read operations, valid data is output to the byte lanes not indicated by "—" in the table above.

<Big endian conversion operation when accessing the internal RAM and BigEdanMod pin = "H">
The following table lists the data alignment in big endian (when one of the ENDIAN3, 2, 1, and 0 bits of the Endian register is "1") and BigEdanMod pin = "H" using a write operation as an example.

DBWidth1:0	A1:A0	D31:D24	D23:D16	AD15:AD8	AD7:AD0	-WR3:-WR0	Remarks
"L:L" (16-bit width)	0:X	—	—	B3h	B2h	-WR1:-WR0=' L'	
	1:X	—	—	B1h	B0h	-WR1:-WR0=' L'	
	0:X	—	—	B3h	Don't Care	-WR1=' L' -WR0=' H'	
	0:X	—	—	Don't Care	B2h	-WR1=' H' -WR0=' L'	
	1:X	—	—	B1h	Don't Care	-WR1=' L' -WR0=' H'	
	1:X	—	—	Don't Care	B0h	-WR1=' H' -WR0=' L'	
"L:H" (8-bit width)	0:0	—	—	—	B3h	-WR0=' L'	
	0:1	—	—	—	B2h	-WR0=' L'	
	1:0	—	—	—	B1h	-WR0=' L'	
	1:1	—	—	—	B0h	-WR0=' L'	

As for read operations, valid data is output to the byte lanes not indicated by "—" in the table above.

7.6 Precautions for Data Transfer

7.6.1 DREQ Signal

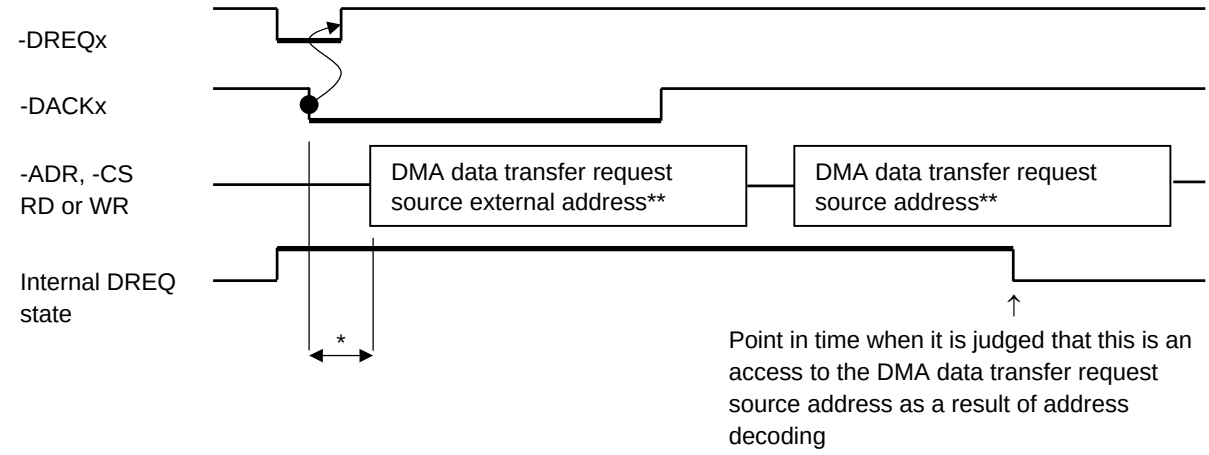
The DMA of the ML60842 operates in single transfer and dual address mode.
"Single transfer" refers to executing one transfer per DREQ. "Dual address mode" refers to outputting the access destination addresses in a transfer cycle.
Also, the DREQ signal is cleared when either one of the following conditions is met:

- The DACK signal has been input while the DREQ signal is active.
- An access to the DMA data transfer request source address has occurred while the DREQ signal is active.

However, note that the DREQ state inside the ML60842 is cleared if an access to the DMA data transfer request source address has occurred even when the DACK signal has been input while the DREQ signal is active. Therefore, it is necessary to input an appropriate address even for DMA transfer.

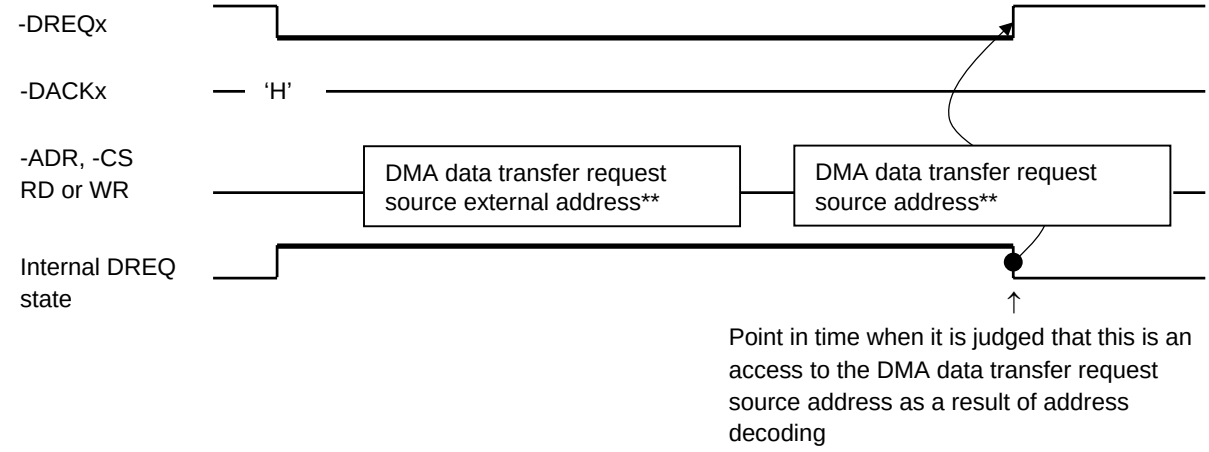
The following shows the DREQ signal and the clear timing of the internal DREQ state.

<When the DACK signal is present>



Note that the timing in which the signals are made valid must be controlled in such a way that the -DACKx signal must always be made valid before the RD or WR signal when the ADR and -CS signals are valid, as indicated by * above. If any access occurs without satisfying this signal timing, data transferred via DMA cannot be guaranteed.

<When the DACK signal is not present>



**: DMA data transfer request source external addresses/DMA data transfer request source addresses
"DMA data transfer request source address" refers to the FifoAcc register (24Xh) when operating as a host (host function). When operating as a peripheral device, it refers to the EPn transmit/receive FIFO specified by the DMA0EP and DMA1EP bits (bits 06:05) of the DMA0CON register (320h) and DMA1CON register (424h), respectively.
"DMA data transfer request source external address" refers to registers, FIFOss and RAM other than those listed above.

7.6.2 Data Allocation

When the ML60842 is used as a host (host function), the DMASTART bits of the HostDataTransReq register, which indicate the head address of the data requested to be transferred from the host core, shows the address in units of 4-byte boundaries. This means that the lower two bits must be handled as "0."

However, if the DMADIR bit of the HostDataTransReq register is "0," the microcontroller can calculate the head address in byte units by using the RDBE bits of the SttTransCnt register.

Also, the amount of data requested to be transferred is shown in the WRCNT or RDCNT bits of the SttTransCnt register in double word (32 bits) units. Set the amount of data transferred by a single DREQ to be the same as the data bus width (DBWidth) and the number of data bytes to be transferred as an integral multiple of 4. In other words, it is necessary to transfer dummy data if the number of bytes is not an integral multiple of 4.

The following shows examples of data transfer for each data bus width under the conditions below:

- The DMASTART bits of the HostDataTransReq register: 00 00 30 58h
- The WRCNT or RDCNT bits of the SttTransCnt register: 011b
- Data allocated at address 00 00 30 58h: XX020304 15161718 292AXXXXh
  (The "X" parts indicate dummy data*.)

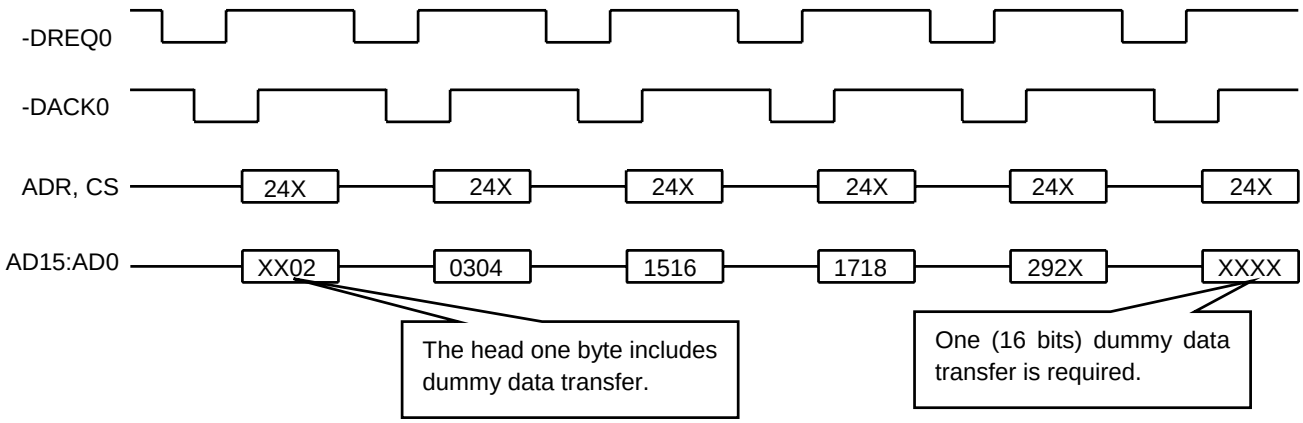
*: Dummy Data

The ML60842 requests an address on 4-byte boundaries, and the number of transfer bytes in an integral multiple of 4 for data transfer.

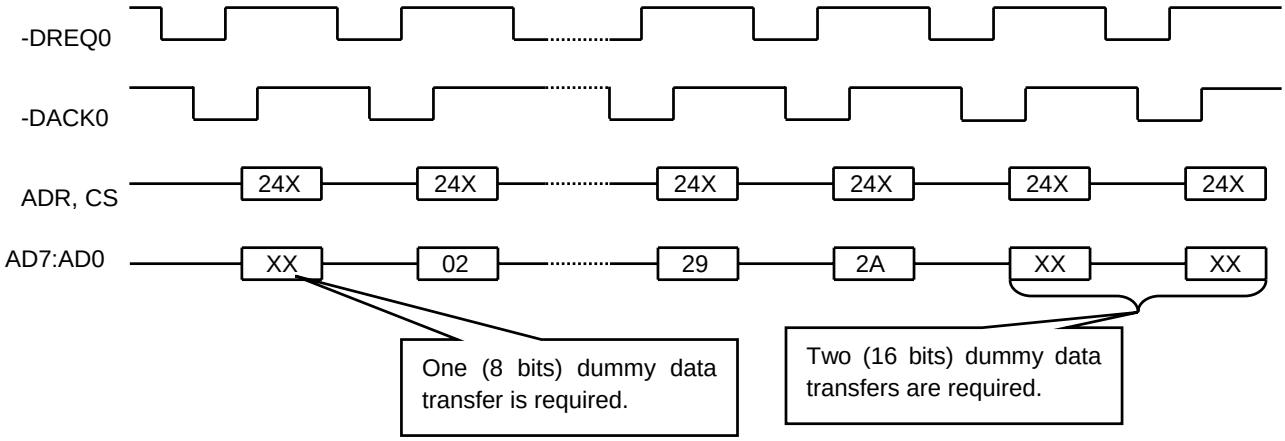
However, dummy data may be transferred during data transfer, depending on data allocation (for example, when the head data address or the number of data bytes to be transferred is not an integral multiple of 4).

The head parts in the examples below are dummy data generated because data is not allocated on 4-byte boundaries, and the tail parts are dummy data generated because the number of data bytes is not an integral multiple of 4.

<For data bus width 16 (DBWidth = "L:L")>



<For data bus width 8 (DBWidth = "L:H")>



7.7 Precautions for Host Control

The host function of the ML60842 conforms to the OHCI Specification in principle, but it also supports the settings and features specific to the ML60842 in addition to the OHCI specification.
The following describes the items specific to the ML60842.

(1) Host Control Register

The Host Control register sets the interrupt source mask bits from the host block (the OHCIRQMASK and DMAIRQMASK bits of the HostCtl register) and the DMA/PIO transfer bit (the DREQMSK bit of the HostCtl register).

If the DREQMSK bit is set to "1" (PIO transfer), an interrupt is generated when the transfer request address from the host core is outside the internal RAM address range. In such a case, it is necessary to process data equal to the number of double words indicated by the WRCNT bits (in the case of writing) or RDCNT bits (in the case of reading) of the SttTransCnt register.

(2) Allocation of Descriptors, Data Buffer and Others

The ML60842 must allocate the endpoint descriptor (ED), transfer descriptor (TD) and interrupt table (HCCA) required for transfer via the OHCI in the internal RAM (4 KB) of the ML60842.

It must also allocate the ED and TD within 16-byte boundaries (32-byte boundaries in the case of isochronous transfer TD) and the HCCA within 256-byte boundaries.

The buffer for data to be transferred can be allocated to either the internal RAM of the ML68042 or an external memory area.

The ML68042 always compares the addresses set in the RamAdr register and transfer request addresses; since the ML68042 processes a transfer request as a transfer to the internal RAM of the ML68042 if they match, it does not request the microcomputer to generate an interrupt pertaining to host data transfer.

Therefore, by allocating the data buffer in the internal RAM of the ML68042, the number of requests, such as for interrupts, to the microcontroller is minimized and, as a result, the CPU load can be significantly reduced.

However, this is not intended to limit the use of the ML68042. It is necessary to perform the optimum allocation by taking account of restrictions on the system configuration, the load on the microcontroller and other factors.

(3) Interrupt Processing

There are two types of interrupts in the host block of the ML60842: interrupts pertaining to host data transfer and interrupts from the host core.

The conditions under which interrupts pertaining to host data transfer are generated are determined as follows, according to the value of the DREQMSK bit (DMA/PIO) of the HostCtl register.

① When the DREQMSK bit of the HostCtl register is "0" (DMA)

- If the transfer address is outside the range of the internal RAM addresses of the ML68042
- If the transfer address is within the range of the internal RAM addresses of the ML60842, and any of the following conditions has occurred:
  - If the continuity (*) of transfer addresses is lost
    The ML60842 monitors the continuity of the transfer addresses and generates an interrupt if the continuity is lost. Therefore, this type of interrupt always occurs at the first transfer.
  - If the transfer direction has changed
    If the transfer direction has changed in relation to just previously executed transfer; specifically, if the value of the DMADIR bit of the HostDataTrnsReq register has changed.

In interrupt processing, it is necessary to reset the transfer start address and transfer length (basically the maximum value) for the DMA controller. It is also necessary to clear the source of this interrupt after the settings for the DMA controller are complete.

② When the DREQMSK bit of the HostCtl register is "1" (PIO)

If the transfer address is outside the range of the internal RAM addresses of the ML60842, an interrupt is generated every time a transfer request occurs.

However, no interrupt is generated for the transfer of double words indicated in the RDCNT bits (in the case of reading) or WRCNT bits (in the case of writing) of the SttTrnsCnt register at the occurrence of an interrupt (the number of double words indicated in the corresponding bits can be transferred by a single interrupt.)

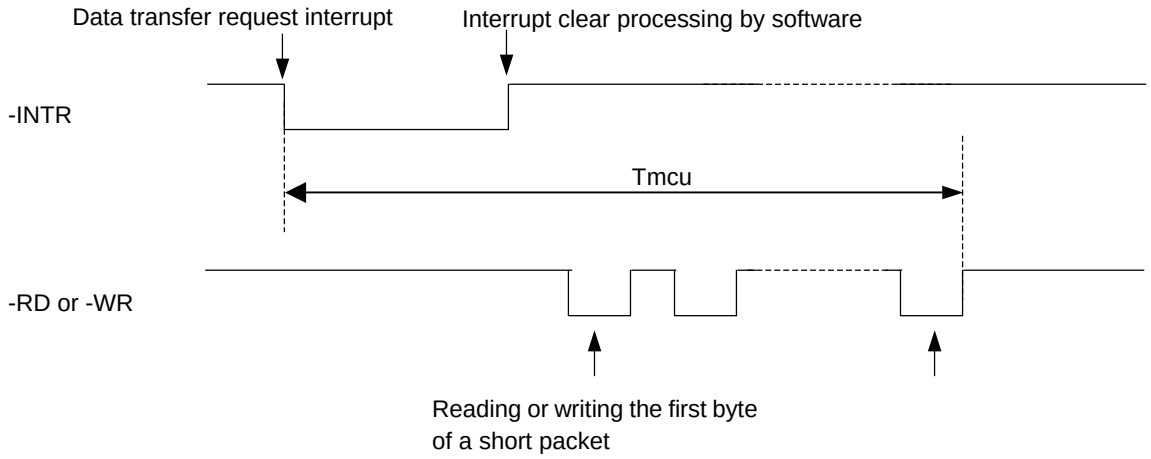
In interrupt processing, it is necessary to read/write data from/to the FifoAcc register by PIO after clearing this interrupt source.

(*): Address Continuity
"Address continuity" refers to a case where an address is "+4h" in relation to the previous transfer address. For example, when accessing 10h byte data from addresses 00h to 0Fh in 16-bit units by dividing it into Ah bytes and 6h bytes, the address changes 00h → 02h → 04h → 06h → 08h, and then 08h → 0Ah → 0Ch. Because 08h appears twice consecutively, the continuity is lost here. Therefore, an interrupt occurs when starting the transfer of the next 6h bytes of data after the transfer of the first Ah bytes of data is complete.

(4) HcFmInterval Register

To utilize control using packets whose sizes do not satisfy MaximumPacketSize (short packets) (refer to Section 4.3.1.3.5 of "OpenHCI Release 1.0a"), it is necessary to set FSMPS and FI in the HcFmInterval Register by taking account of the data processing time of the microcontroller.

<Microcontroller's data processing time>



It is necessary to set MAXIMUM_OVERHEAD so as to allocate a margin of 170-bit time or more, as shown below, for the data processing time (Tmcu) of the microcontroller shown in the illustration above.

MAXIMUM_OVERHEAD > Tmcu + 170-bit time

In the expression above,
1-bit time = approximately 84 ns
MAXIMUM_OVERHEAD = FI - FSMPS * 7/6

It is thus necessary to set FSMPS and FI so as to satisfy the above constraint conditions.

7.8 Precautions for Peripheral Control

The peripheral function of the ML60842 conforms to the ML60852A specification in principle, but it also supports the settings and features specific to the ML60842 that are different from those of the ML60852A specification. The following describes the items specific to the ML60842.

(1) Packet Data Transmission (ML60842 → USB Host)

The microcontroller interface of the ML60842 is switchable between 16-bit data bus width and 32-bit data bus width.

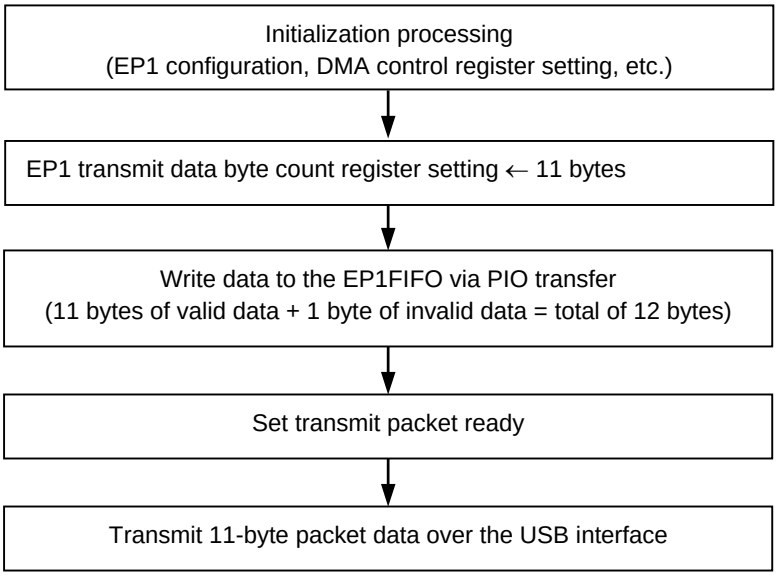
Data can only be transferred via PIO transfer to the EP0 and EP3 packet data transfer FIFOs, whereas data can be transferred via DMA or PIO transfer to the EP1, EP2, EP4, and EP5 packet data transfer FIFOs.

For example, if 11 bytes of packet data is written to the packet data transfer FIFO via PIO transfer using a data bus width of 16 bits, the number of bytes written to the FIFO is 12 bytes. In other words, valid packet data (11 bytes) and invalid packet data (1 byte) are written.

The ML60842 can suppress invalid packet data by setting the number of valid packet data bytes per packet in the EPn transmit data byte count register so that only valid packet data can be transmitted over the USB interface.

The following examples show specific cases where a data bus width of 16 bits is used.

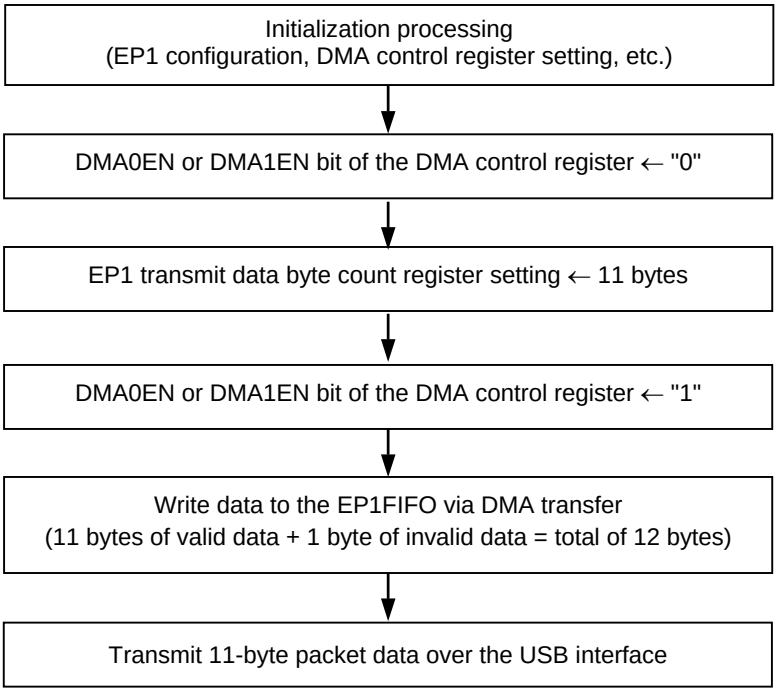
<Example 1> When 11 bytes of valid data plus 1 byte of invalid data are written to the EP1 via PIO transfer



In Example 1 above, writing to the EP1FIFO is executed six times (12 bytes) using a bus width of 16 bits. However, since valid data only consists of 11 bytes, 1 byte is added as invalid data. By setting the number of valid data bytes (11 bytes) in the EP1 transmit data byte count register, 1 byte of invalid data is discarded inside the ML60842 after setting the transmit packet ready bit, and only 11 bytes of valid data are transmitted over the USB interface.

Note that "PIO transfer" refers to a case where an EP is not specified as the DMA transfer target EP by the DMA0EP/DMA1EP bits of the DMA0CON/DMA1CON register, respectively, or an EP is specified as the DMA transfer target EP but DMA is disabled by the DMA0EN/DMA1EN bits.

<Example 2> When 11 bytes of valid data plus 1 byte of undefined data are written to the EP1 via DMA transfer



In Example 2 above, writing to the EP1FIFO is executed six times (12 bytes) using a bus width of 16 bits. However, since valid data only consists of 11 bytes, 1 byte is added as invalid data. By setting the number of valid data bytes (11 bytes) in the EP1 transmit data byte count register, 1 byte of invalid data is discarded inside the ML60842 after completing the DMA transfer of 12 bytes, and only 11 bytes of valid data are transmitted over the USB interface.
Note that "DMA transfer" refers to a case where an EP is specified as the DMA transfer target EP by the DMA0EP/DMA1EP bits of the DMA0CON/DMA1CON register, respectively, and an EP is specified as the DMA transfer target EP but DMA is enabled by the DMA0EN/DMA1EN bits.

The following table shows the relationships among the number of bytes written to the packet data transfer FIFO, the setting values of the transmit data byte count register at DMA transfer/PIO transfer, and the number of packet data bytes transmitted over the USB interface.

	Number of bytes written to the packet data transfer FIFO	Setting value of the transmit data byte count register	Number of packet data bytes transmitted over the USB interface	Remarks
DMA transfer	*1	M	M	
PIO transfer	*2	N	N	

*1: Data transfers are requested by outputting a DREQ until as many bytes as set in the transmit data byte count register have been transferred (for example, the number of DMA transfer bytes is 12 if M = 11 and 6 if M = 6 when the data bus width is 16 bits, and the number of DMA transfer bytes is 12 if M = 11 and 8 if M = 6 when the data bus width is 32 bits). The DREQ output is stopped once the designated number of bytes is reached, and M bytes of packet data is transmitted over the USB interface.

*2: N bytes of packet data equivalent to the setting value (N) in the transmission data byte count register is transmitted at the timing when the packet ready bit is set, regardless of the number of bytes written to the packet data transfer FIFO. In other words, if less than N bytes are written to the packet data transfer FIFO, N bytes of packet data, appended with undefined data equivalent to the number of missing bytes, is transmitted over the USB interface. This also means that if more than N bytes are written to the packet data transfer FIFO, only N bytes of packet data is transmitted over the USB interface after discarding excess byte data.

(2) ISO IN Transfer Control

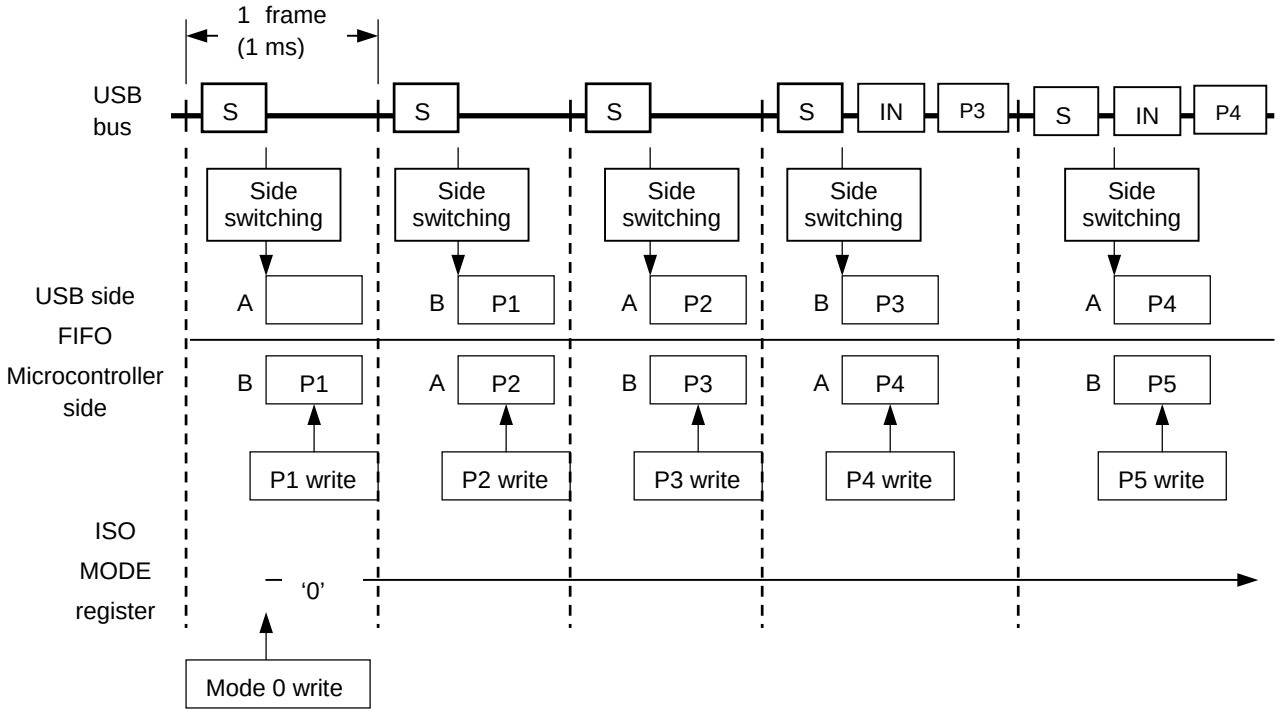
The ML60842 allows specifying the following two types of operating modes if an EP has been configured for ISO IN transfer:

① A mode for switching between the two sides of a double-sided FIFO every time an SOF is received so as to continuously transfer data (mode 0)

② A mode for switching between the two sides of a double-sided FIFO after data written to the FIFO is transmitted to the USB host (when the next SOF after receiving an IN token is detected) in order to avoid data loss (mode 1)

These operating modes can be specified by the ISOMODE register (378h). The operation of the ML60842 in each of these operating modes is explained below.

<Operation equivalent to the ML60852A (corresponding bit of the ISOMODE register = "0")>



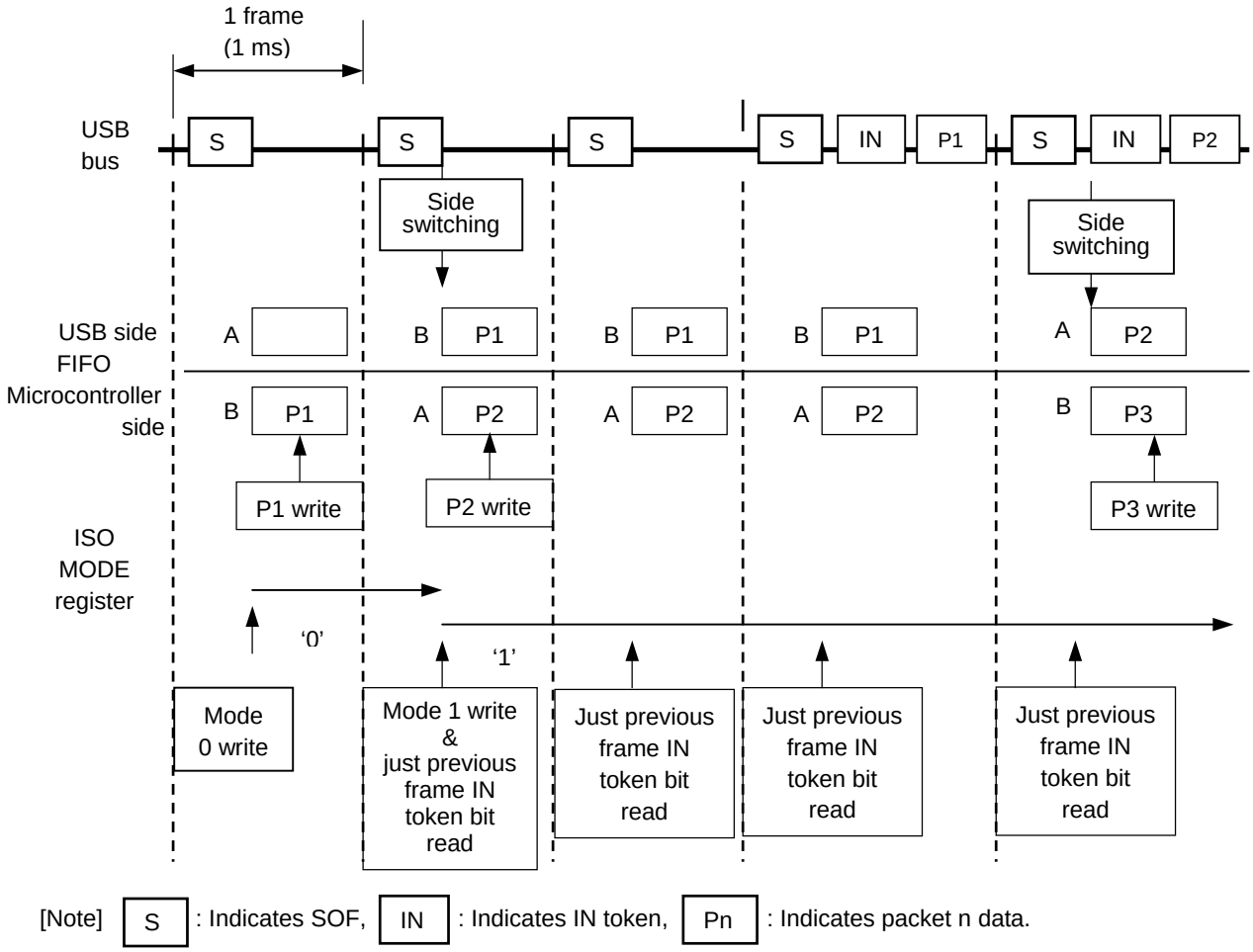
[Note] S : Indicates SOF, IN : Indicates IN token, Pn : Indicates packet n data.

The illustration above shows a case where data packets P1, P2,…, P5 are written sequentially from the microcontroller side, and an IN token is transmitted from the USB host in the next frame upon completion of writing P3 packet data.

Set the ISOMODE register to "0" after the first SOF interrupt; it is not necessary to change the setting thereafter.

This mode (mode 0) switches between the two sides of the FIFO every time an SOF is received; therefore, the data prior to the data packet written during the frame period immediately before receiving an IN token (P3 packet data in the illustration above) is not transmitted. P3, the latest data at the time when the IN token is received, is transmitted in real time.

<Operation for switching the two sides of the FIFO after transmitting FIFO data (corresponding bit of the ISOMODE register = "1")>



[Note] S : Indicates SOF, IN : Indicates IN token, Pn : Indicates packet n data.

The illustration above shows a case where P1, P2, and P3 packet data are written sequentially from the microcontroller side, and an IN token is transmitted from the USB host in the frame after the next frame upon completion of writing P2 packet data.

Set the ISOMODE register to "0" after the first SOF interrupt. By setting mode 0 here, the ML60842 automatically switches between the two sides of the FIFO by the next SOF. Set the ISOMODE register to "1" after the next SOF interrupt upon completion of writing P1 packet data so as to specify operation in mode 1 thereafter.

Once mode 1 is specified, the ML60842 reads bit 07 (the IN token bit in the immediately previous frame) of the EPn status register at each SOF interrupt. If this bit is set to "1," it indicates that packet data has been transferred to the USB host in the immediately previous frame; thus, the ML60842 automatically switches the two sides of the FIFO. Since one side of the FIFO is empty, the microcontroller writes packet data to the FIFO. If this bit is set to "0," writing data to the FIFO is suspended.

In this mode (mode 1), the two sides of the FIFO are switched when an SOF is detected immediately after receiving an IN token from the USB host. Therefore, packet data previously written to the FIFO from the microcontroller (P1 and P2 packet data in the illustration above) is not lost.

However, depending on the relative timings at which data is written from the microcontroller and an IN token is transmitted from the USB host, the latest data may not be transmitted. For this reason, be sure to use mode 0 in applications that request the transmission of the latest data.

(3) Suspend/Resume Control

When executing power down upon detecting the suspend state, the suspend/resume state must be controlled as follows:

① When the suspend state is detected (the SE0 state continues 3 ms) on the USB interface, set the device suspend state interrupt status bit of the INTSTAT2 register to "1" so as to generate an interrupt.

↓

② Using this interrupt as a trigger, the microcontroller sets the CLKSTOP bit of the RstClkCtl register to "1" and executes clock stop processing.

↓

③ The microcontroller waits until the CLKSTOP bit of the RstClkCtl register is set to "1" (clock stop), sets the XSTOP bit of the RstClkCtl register to "1" and then executes oscillation stop processing.

By these steps, the ML60842 can be powered down when the suspend state is detected.
Note that it is not necessary to execute processing steps ② and ③ above if powering down the ML60842 is not required.

④ When the resume start is detected (the state transits from the idle state to the K state) over the USB interface, set the USBIFCHG bit of the OTGIntStt register to "1" so as to generate an interrupt.

↓

⑤ If processing step ③ above has been executed, the microcontroller uses this interrupt as a trigger to reset the XSTOP bit of the RstClkCtl register to "0" and executes oscillation start processing.

↓

⑥ If processing step ② above has been executed, the microcontroller waits for the duration of the oscillation stabilization time after executing processing step ⑤, resets the CLKSTOP bit of the RstClkCtl register to "0" and then executes clock start processing.

7.9 Precautions for VBUS Overcurrent Control

To operate the ML60842 as device A of the OTG standard or as a standard host, it is necessary to supply power to VBUS.
The ML60842 can control an external voltage regulator for VBUS by using the -PCONT pin.
Also, any overcurrent that occurs while power is being supplied to VBUS can be recognized by using the -OVRCRT pin and the OHCI register, as well as by monitoring the VBUS voltage level using the SVBUS pin.

The following describes how to recognize overcurrent by monitoring the VBUS voltage level using the SVBUS pin.

Connect the VBUS signal over the USB interface to the SVBUS pin, and monitor the voltage level of the SVBUS pin.
More specifically, set the AVBUSVLDENB bit of the OTGCtl register to "1" (enable) while supplying power to VBUS, and monitor that the voltage level of the SVBUS pin is always above the designated value.
If the voltage level of the SVBUS pin drops below the setting value of the SELSV bit of the OTGCtl register, the ML60842 sets the AVBUSVLDCHG bit of the OTGIntStt register to "1" so as to generate an interrupt. Using this interrupt as a trigger, the microcontroller judges that the VBUS voltage level has dropped below the designated value if the AVBUSVLDST bit of the OTGIntStt register is "0" and recognizes the occurrence of overcurrent.

Note that if overcurrent occurs, it is necessary to immediately stop supplying power to VBUS by an external circuit.

8. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Rated value	Unit
Power supply voltage	V_{DD}	Tj = 25°C, GND = 0 V	-0.3 to +4.6	V
Input voltage	V_I		-0.3 to +V_{DD}+0.3	V
Output current	I_O		-12 to +12	mA
Power dissipation (BGA)	Pb	Top = 70°C	330	mW
Power dissipation (TQFP)	Pt		300	
Storage temperature	T_{STG}	—	-55 to +150	°C

9. RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	—	3.0 to 3.6	V
Operating temperature	T_{OP}	—	0 to 70	°C
Crystal frequency	f_{OSC}	—	48±0.024	MHz

10. ELECTRICAL CHARACTERISTICS

10.1 DC Characteristics (1)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit	Target pin
"H" input voltage	V_{IH}		V_{DD}×0.7	—	—	V	Note 1
"L" input voltage	V_{IL}		—	—	0.8	V	
"H" input voltage	V_{IH}		V_{DD}×0.8	—	—	V	Xin
"L" input voltage	V_{IL}		—	—	V_{DD}×0.2	V	
Schmitt trigger input voltage	Vt+		—	—	V_{DD}×0.7	V	-RESET
	Vt-		0.8	—	—	V	
"H" output voltage	V_{OH}	I_{OH} = -4 mA	2.2	—	—	V	Note 2
"L" output voltage	V_{OL}	I_{OL} = 4 mA	—	—	0.45	V	Note 3
"H" input current	I_{IH}	$V_{IH} = V_{DD}$	—	0.1	10	µA	Note 4
"L" input current	I_{IL}	V_{IL} = GND	-10	-0.1	—	µA	
"H" input current	I_{IH}	$V_{IH} = V_{DD}$	—	0.1	10	µA	Note 5
"L" input current	I_{IL}	V_{IL} = GND	-200	-66	-10	µA	
3-state output leakage current	I_{OZH}	$V_{OH} = V_{DD}$	—	0.1	10	µA	Note 6
	I_{OZL}	V_{OL} = GND	-10	-0.1	—	µA	
Power supply current when in operation	I_{CC}	Note 7	—	—	50	mA	V_{DD}
Power supply current when stationary	I_{CCS}	0 to 50°C, Note 8	—	30	100	µA	
		to 70°C, Note 8	—	30	200		

The values listed in the minimum, typical, and maximum columns in the table above indicate the design target values.

Note 1: Applies to I/O types "*2, *3, and *4" in the table shown in Section 4, "Pin Connections."
Note 2: Applies to I/O types "*3 and *5" in the table shown in Section 4, "Pin Connections."
Note 3: Applies to I/O types "*3 and *5" in the table shown in Section 4, "Pin Connections."
Note 4: Applies to I/O types "*4" in the table shown in Section 4, "Pin Connections."
Note 5: Applies to I/O types "*2" in the table shown in Section 4, "Pin Connections."
Note 6: Applies to I/O types "*3" in the table shown in Section 4, "Pin Connections."
Note 7: In-phase/out-of-phase 48 MHz clock input to $V_{IH} = V_{DD}$, V_{IL} = GND, WSYNC_CLK = 33 MHz, Xin/Xout pins
Note 8: State in which TBD (XX µs) has elapsed after writing "1" to the XSTOP bit of the RstClkCtl register. The output pins are all open.
$V_{IH} = V_{DD}$, V_{IL} = GND

10.2 DC Characteristics (2) USB Port

(V_{DD} = 3.0 to 3.6 V, GND = 0 V, Ta = 0 to +70°C)

Item	Symbol	Condition	MIN	TYP	MAX	Unit	Target pin
Differential input sensitivity	VDI	|(D+)-(D-)|	0.2	—	—	V	D+, D-
Differential common mode range	VCM	Including VDI portion	0.8	—	2.5	V	
Single-ended receiver threshold	VSE		0.8	—	2.0	V	
"H" output voltage	V_{OH}	15 kΩ to GND	2.8	—	3.6	V	
"L" output voltage	V_{OL}	1.5 kΩ to 3.6 V	—	—	0.3	V	
Output leakage current	I_{LO}	0 V<VIN<V_{DD}	-10	—	+10	µA	

10.3 AC Characteristics: USB Port Block (Full-Speed)

(V_{DD} = 3.0 to 3.6 V, GND = 0 V, Ta = 0 to +70°C)

Item	Symbol	Condition (Note 1)	MIN	TYP	MAX	Unit	Target pin
Rise time	TR	CL = 50 pF	4	—	20	ns	D+, D-
Fall time	TF	CL = 50 pF	4	—	20	ns	
Output signal crossover voltage	VCRS		1.3	—	2	V	
Driver output resistance	ZDRV	When driving in steady state	28	—	44	Ω	
Data rate	TDRATE	Average bit rate (12 Mbps ± 0.25%)	11.97	—	12.03	Mbps	

(Note 1) TR and TF represent the transition time between 10% amplitude and 90% amplitude.

10.4 AC Characteristics: USB Port Block (Low-Speed)

(V_{DD} = 3.0 to 3.6 V, GND = 0 V, Ta = 0 to +70°C)

Item	Symbol	Condition (Note 1)	MIN	TYP	MAX	Unit	Target pin
Rise time	TR	CL = 150 pF	75	—	300	ns	D+, D-
Fall time	TF	CL = 150 pF	75	—	300	ns	
Output signal crossover voltage	VCRS		1.3	—	2	V	
Data rate	TDRATE	Average bit rate (1.5 Mbps ± 0.25%)	1.4775	—	1.5225	Mbps	

(Note 1) TR and TF represent the transition time between 10% amplitude and 90% amplitude.

10.5 AC Characteristics: Microcontroller Interface Block

10.5.1 AC Characteristics: Microcontroller Interface Block (General-Purpose Product)

(1) Separate Bus, Read (ML60842 → Microcontroller) Specification

(V_{DD} = 3.0 to 3.6 V, GND = 0 V, Ta = 0 to +70°C, load capacity 20 pF)

Item	Symbol	MIN	MAX	Unit
Setup time of A12:A0 and BigEdanMod for -RD	t1	10		ns
Setup time of -CS1:0 for -RD	t2	0		
Delay time from when -RD is enabled until when -WAIT1 is determined	t3		20	
Delay time from when -RD is enabled until when AD15:AD0 are output	t4	0		
Hold time of A12:A0 for -RD	t5	0		
-RD pulse width	t6	42		
Hold time of -CS1:0 for -RD	t7	0		
Delay time from when valid data is output to AD15:AD0 until when -WAIT1 is cancelled	t8	0		
Delay time from when -RD is disabled until when AD15:AD0 is set to Hi-Z	t9	0	10	
Recovery time from when either -CS1:0 or -RD is disabled until when both -CS1:0 and -RD are enabled	t10	35		
Delay time from when both -CS1:0 are enabled until when -WAIT1 is not set to Hi-Z	t11	0	10	
Delay time from when one of -CS1:0 is disabled until when -WAIT1 is set to Hi-Z	t12		10	
Delay time from when -RD is enabled if -WAIT1 is not asserted until when valid data is output to D31:D16 and AD15:AD0	t13		27	

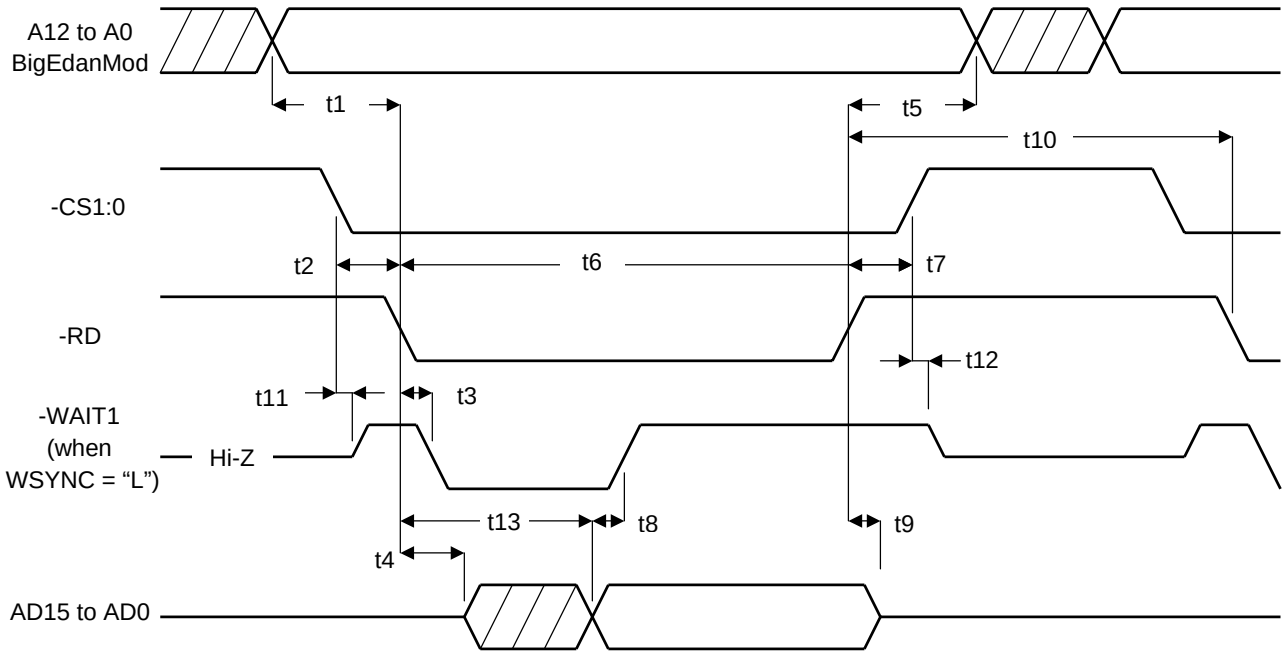
Note 1: The above values show the design target values.

Note 2: The delay time (t9) from when -RD is disabled until when AD15:AD0 are set to Hi-Z is 10 ns maximum. If a write access is made following a read access and the write data is output fast, a bus conflict may occur due to this delay time. In this case, it is necessary to insert an idle cycle of one clock cycle or more between the access cycles.

Note 3: The delay time (t3) from when -RD is enabled until when -WAIT1 is determined is 20 ns maximum. Insert software wait as necessary to ensure that the microcontroller can recognize -WAIT1.

Note 4: The specification of -WAIT1 indicates a case where WSYNC = “L.” For the timing specification when WSYNC = “H,” see (6), "Clock Synchronization WAIT Signal Specification."

Note 5: If the CLKSTOP bit of the RstClkCtl register is "1," the -WAIT signal is not asserted when accessing the common registers (offsets 000h to 01Ch). t13 indicates the delay in output of valid data in this case. Insert software wait in case the microcontroller that does not have sufficient setup time for valid data.


A12 to A0
BigEdanMod
t1
t5
t10
-CS1:0
t2
t6
t7
-RD
t12
t11
t3
-WAIT1
(when
WSYNC = “L”)
Hi-Z
t13
t8
t9
t4
AD15 to AD0

(2) Separate Bus, Write (Microcontroller →ML60842) Specification

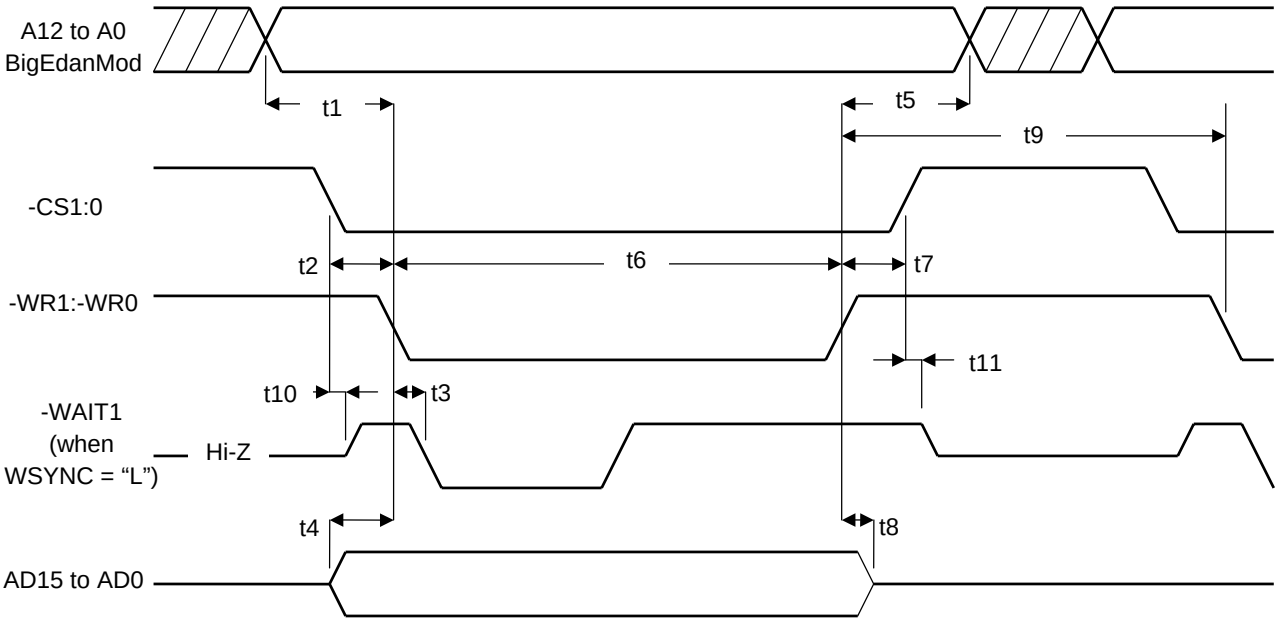
(V_{DD} = 3.0 to 3.6 V, GND = 0 V, Ta = 0 to +70°C, load capacity 20 pF)

Item	Symbol	MIN	MAX	Unit
Setup time of A12:A0 and BigEdanMod for -WR1:-WR0	t1	10		ns
Setup time of -CS1:0 for -WR1:-WR0	t2	0		
Delay time from when -WR1:-WR0 are enabled until when -WAIT1 is determined	t3		20	
Setup time of AD15:AD0 for -WR1:-WR0	t4	0		
Hold time of AD12:A0 for -WR1:-WR0	t5	10		
-WR1:-WR0 pulse width	t6	42		
Hold time of -CS1:0 for -WR1:-WR0	t7	10		
Hold time of AD15:AD0 for -WR1:-WR0	t8	10		
Recovery time from when either -CS1:0 or -WR1:-WR0 are disabled until when both -CS1:0 and -WR1:-WR0 are enabled	t9	35		
Delay time from when both -CS1:0 are enabled until when -WAIT1 is not set to Hi-Z	t10	0	10	
Delay time from when one of -CS1:0 is disabled until when -WAIT1 is set to Hi-Z	t11		10	

Note 1: The above values show the design target values.

Note 2: The delay time (t3) from when -WR1:-WR0 are enabled until when -WAIT1 is determined is 20 ns maximum.
Insert software wait as necessary to ensure that the microcontroller can recognize -WAIT1.

Note 3: The specification of -WAIT1 indicates a case where WSYNC = "L." For the timing specification of -WAIT1:0 when WSYNC = "H," see (6), "Clock Synchronization WAIT Signal Specification."



(3) Multiplex Bus, Read (ML60842 → Microcontroller) Specification

(V_{DD} = 3.0 to 3.6 V, GND = 0 V, Ta = 0 to +70°C, load capacity 20 pF)

Item	Symbol	MIN	MAX	Unit
Hold time of AD15:AD0 and BigEdanMod for ALE falling edge	t1	10		ns
Setup time of -CS1:0 for -RD	t2	0		
Delay time from when -RD is enabled until when AD15:AD0 are output	t3	0		
Delay time from when -RD is enabled until when -WAIT1 is established	t4		20	
Delay time from when -RD is disabled until when AD15:AD0 is set to Hi-Z	t5	0	10	
-RD pulse width	t6	42		
Hold time of -CS1:0 for -RD	t7	0		
Delay time from when valid data is output to AD15:AD0 until when -WAIT1 is cancelled	t8	0		
Setup time of AD15:AD0 and BigEdanMod for ALE falling edge	t9	10		
Recovery time from when either -CS1:0 or -RD is disabled until when both -CS1:0 and -RD are enabled	t10	35		
ALE pulse width	t11	15		
Delay time from when ALE is disabled until when -RD is enabled	t12	10		
Delay time from when both -CS1:0 are enabled until when -WAIT1 is not set to Hi-Z	t13	0	10	
Delay time from when one of -CS1:0 is disabled until when -WAIT1 is set to Hi-Z	t14		10	
Delay time from when -RD is enabled if -WAIT1 is not asserted until when valid data is output to AD15:AD0	t15		27	

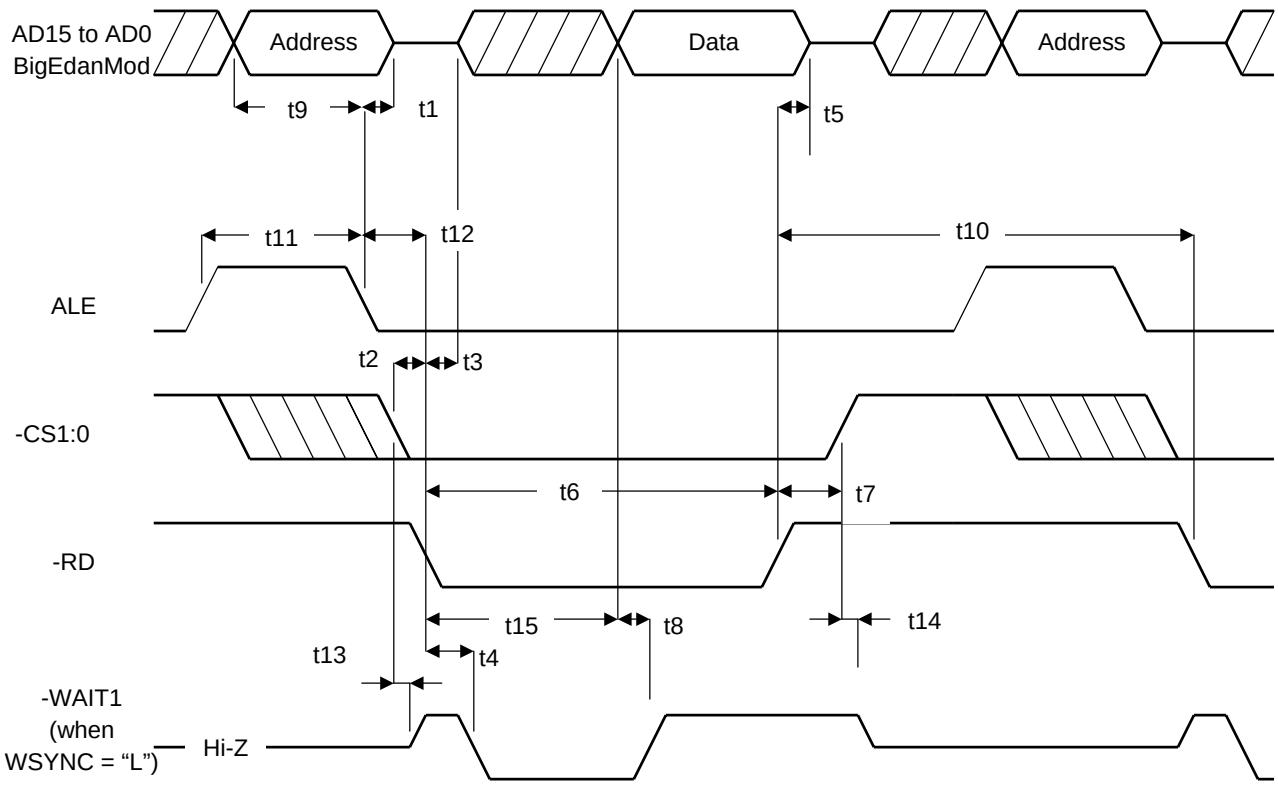
Note 1: The above values show the design target values.

Note 2: The delay time (t5) from when -RD is disabled until when AD15:AD0 are set to Hi-Z is 10 ns maximum. If a write access is made following a read access and the write data is output fast, a bus conflict may occur due to this delay time. In this case, it is necessary to insert an idle cycle of one clock cycle or more between the access cycles.

Note 3: The delay time (t4) from when -RD is enabled until when -WAIT1 is determined is 20 ns maximum. Insert software wait as necessary to ensure that the microcontroller can recognize -WAIT1.

Note 4: The specification of -WAIT1 indicates a case where WSYNC = “L.” For the timing specification of -WAIT1:0 when WSYNC = “H,” see (6), "Clock Synchronization WAIT Signal Specification."

Note 5: If the CLKSTOP bit of the RstClkCtl register is "1," the -WAIT signal is not asserted when accessing the common registers (offsets 000h to 01Ch). t15 indicates the delay in output of valid data in this case. Insert software wait in case the microcontroller that does not have sufficient setup time for valid data.

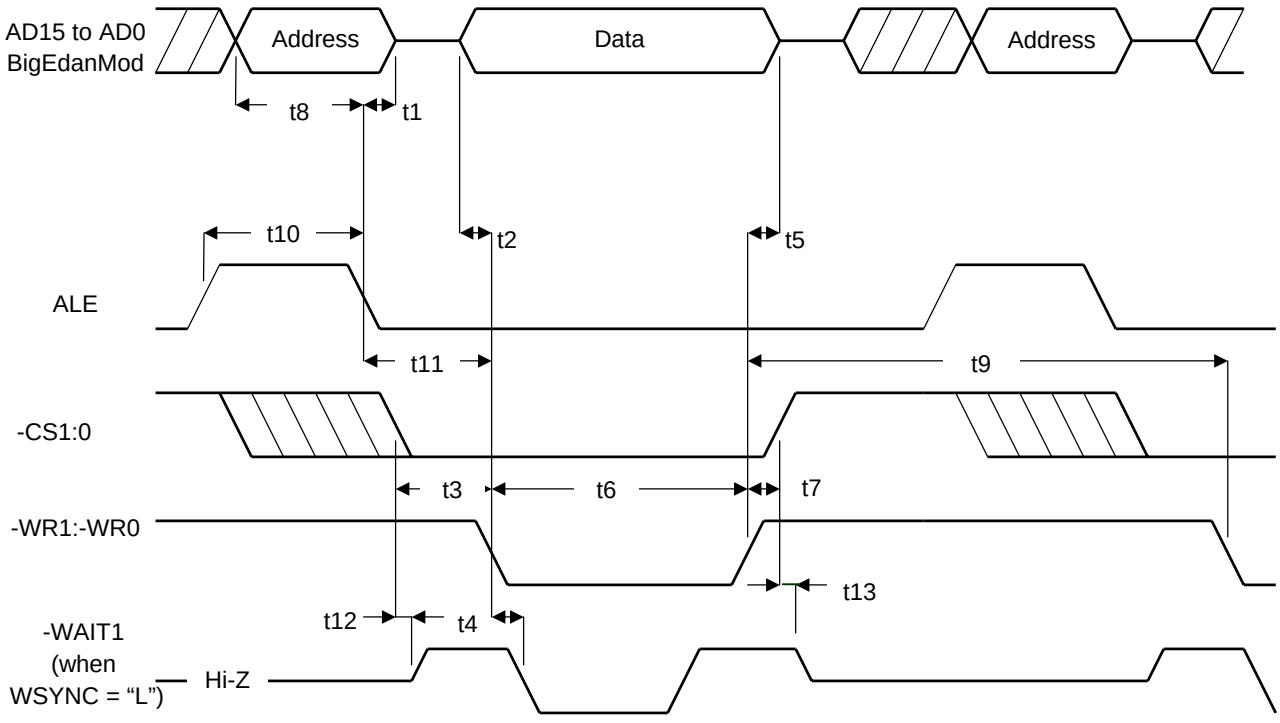

AD15 to AD0
BigEdanMod
Address
Data
Address
t9
t1
t5
t11
t12
t10
ALE
t2
t3
-CS1:0
t6
t7
-RD
t15
t8
t14
t13
t4
-WAIT1
(when
WSYNC = “L”)
Hi-Z

(4) Multiplex Bus, Write (Microcontroller → ML60842) Specification

(V_{DD} = 3.0 to 3.6 V, GND = 0 V, Ta = 0 to +70°C, load capacity 20 pF)

Item	Symbol	MIN	MAX	Unit
Hold time of AD15:AD0 and BigEdanMod for ALE falling edge	t1	10		ns
Setup time of AD15:AD0 for -WR1:-WR0	t2	0		
Setup time of -CS1:0 for -WR1:-WR0	t3	0		
Delay time from when -WR1:-WR0 are enabled until when -WAIT1 is determined	t4		20	
Hold time of AD15:AD0 for -WR1:-WR0	t5	10		
-WR1:-WR0 pulse width	t6	42		
Hold time of -CS1:0 for -WR1:-WR0	t7	10		
Setup time of AD15:AD0 and BigEdanMod for ALE falling edge	t8	10		
Recovery time from when either -CS1:0 or -WR1:-WR0 are disabled until when both -CS1:0 and -WR1:-WR0 are enabled	t9	35		
ALE pulse width	t10	15		
Delay time from when ALE is disabled until when -WR1:-WR0 are enabled	t11	10		
Delay time from when both -CS1:0 are enabled until when -WAIT1 is not set to Hi-Z	t12	0	10	
Delay time from when one of -CS1:0 is disabled until when -WAIT1 is set to Hi-Z	t13		10	

Note 1: The above values show the design target values.
Note 2: The delay time (t4) from when -RD is enabled until when -WAIT1 is determined is 20 ns maximum. Insert software wait as necessary to ensure that the microcontroller can recognize -WAIT1.
Note 3: The specification of -WAIT1 indicates a case where WSYNC = "L." For the timing specification when WSYNC = "H," see (6), "Clock Synchronization WAIT Signal Specification."



(5) DREQ Signal/DACK Signal Specification

There are two types of DREQ clear conditions for the ML60842 as follows:
- Clear by DACK response
- Clear by accessing the DMA request source

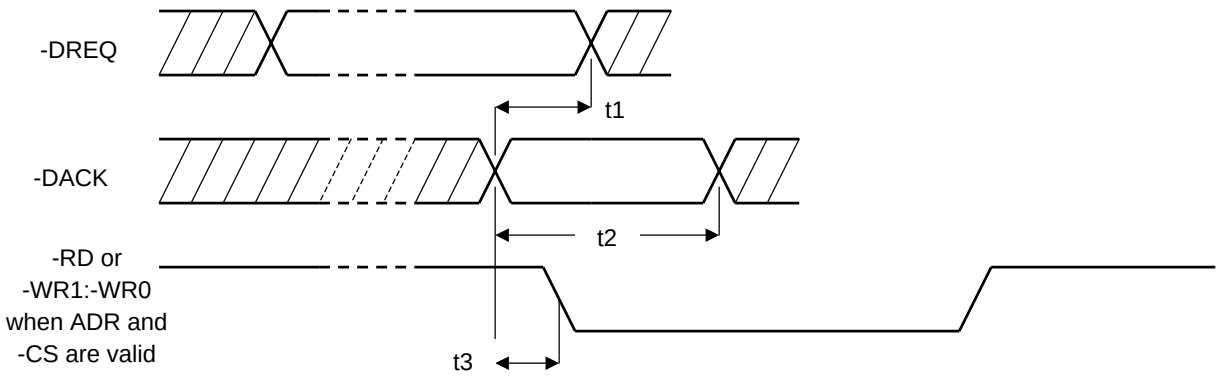
The following shows the AC specification in each case.

(V_{DD} = 3.0 to 3.6 V, GND = 0 V, Ta = 0 to +70°C, load capacity 20 pF)

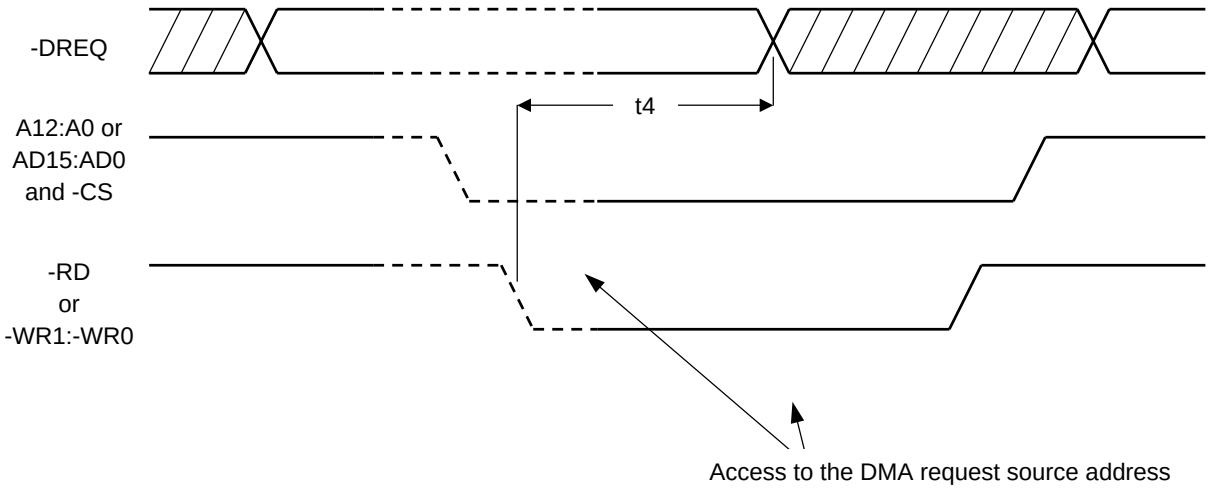
Item	Symbol	MIN	MAX	Unit
Delay time from when -DACK is enabled until when -DREQ is disabled	t1		20	ns
Minimum pulse width of -DACK	t2	30		
Time from when -DACK is enabled until when -CS1:0 and -RD or -WR1:0 are enabled	t3	0		
Delay time from when -RD or -WR1:-WR0 for the DMA request source address are enabled until when -DREQ is disabled	t4	TBD		

Note 1: The above values show the design target values.
Note 2: The time (t3) from when -DACK is enabled until when -CS01:0 and -RD or -WR1:0 are enabled is 0 ns minimum.
If an access occurs that enables -CS1:0 and -RD or -WR1:0 before -DACK is enabled, data transferred via DMA transfer cannot be guaranteed.

<Clear by DACK response>



<Clear by accessing the DMA request source>

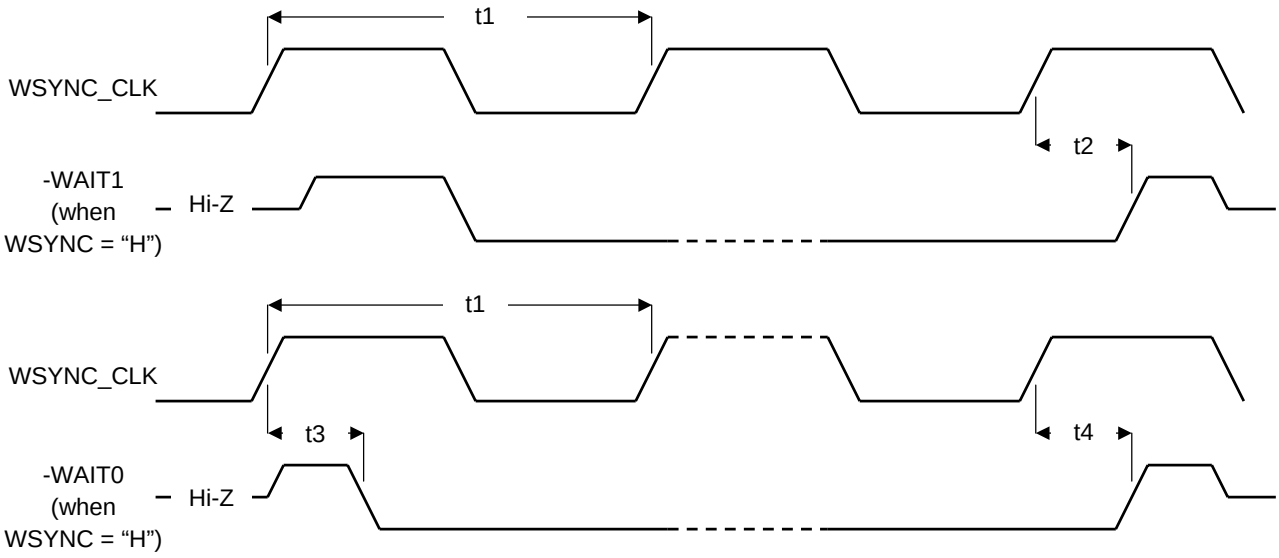


(6) Clock Synchronization WAIT Signal Specification

(V_{DD} = 3.0 to 3.6 V, GND = 0 V, Ta = 0 to +70°C, load capacity 20 pF)

Item	Symbol	MIN	MAX	Unit
Cycle of WSYNC_CLK	t1	30		ns
Delay time from the rising edge of WSYNC_CLK until when -WAIT1 is disabled	t2	8	18	
Delay time from the rising edge of WSYNC_CLK until when -WAIT0 is enabled	t3		15	
Delay time from the rising edge of WSYNC_CLK until when –WAIT0 is disabled	t4	8	18	

Note 1: The above values show the design target values.
Note 2: To sample -WAIT synchronously with WSYNC_CLK, sample it at the rising edge of WSYNC_CLK.
Note 3: For the timing specification to change to/from Hi-Z, see items (1) to (4) in this section.

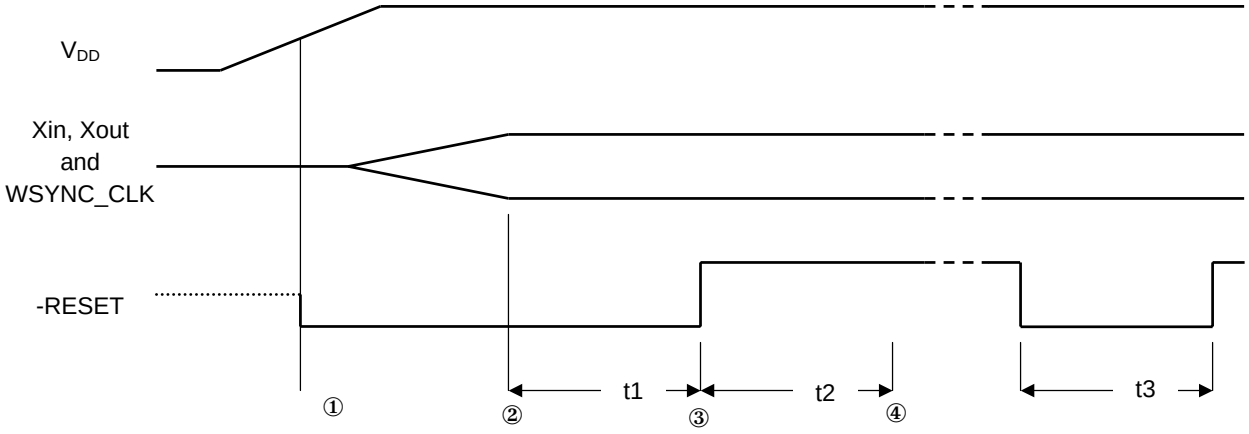


(7) RESET Signal Specification

(V_{DD} = 3.0 to 3.6 V, GND = 0 V, Ta = 0 to +70°C, load capacity 20 pF)

Item	Symbol	MIN	MAX	Unit
Time from when the oscillation of the oscillator stabilizes (48 MHz) and WSYNC_CLK is input (when WSYNC = "H") until when -RESET is deasserted	t1	50		µs
Time from when -RESET is deasserted until when the ML60842 becomes accessible	t2	50		
-RESET pulse width	t3	50		

Note 1: The above values show the design target values.
Note 2: Supply the WSYNC_CLK signal to the ML60842 before timing ② below (when WSYNC = "H").



① V_{DD} rises and the RESET signal is asserted.
② The oscillation of the oscillator stabilizes (48 MHz) and WSYNC _CLK is input.
The time until the oscillation of the oscillator stabilizes (① to ② above) varies depending on the oscillator used. Be sure to allocate sufficient time.
③ The RESET signal is deasserted.
Keep the RESET signal active at least 50 µs (② to ③ above) in order to initialize the ML60842.
④ The internal setup of the ML60842 is complete and it is then accessible from the microcontroller.
Do not access the ML60842 before timing ④ above.

10.5.2 AC Characteristics: Microcontroller Interface Block (Extended Voltage Temperature Range Product)

(1) Separate Bus, Read (ML60842 → Microcontroller) Specification

($A1V_{DD}$, $A2V_{DD}$ = 3.0 to 3.1 V, DV_{DD} = 2.7 to 2.9 V, GND = 0 V, Ta = -10 to +80°C, load capacity 20 pF)

Item	Symbol	MIN	MAX	Unit
Setup time of A12:A0 and BigEdanMod for -RD	t1	10		ns
Setup time of -CS1:0 for -RD	t2	0		
Delay time from when -RD is enabled until when -WAIT1 is established	t3		30	
Delay time from when -RD is enabled until when AD15:AD0 are output	t4	0		
Hold time of A12:A0 for -RD	t5	0		
-RD pulse width	t6	42		
Hold time of -CS1:0 for -RD	t7	0		
Delay time from when valid data is output to AD15:AD0 until when -WAIT1 is cancelled	t8	0		
Delay time from when -RD is disabled until when AD15:AD0 is set to Hi-Z	t9	0	25	
Recovery time from when either -CS1:0 or -RD is disabled until when both -CS1:0 and -RD are enabled	t10	35		
Delay time from when both -CS1:0 are enabled until when -WAIT1 is not set to Hi-Z	t11	0	20	
Delay time from when one of -CS1:0 is disabled until when -WAIT1 is set to Hi-Z	t12		20	
Delay time from when -RD is enabled if -WAIT1 is not asserted until when valid data is output to AD15:AD0	t13		35	

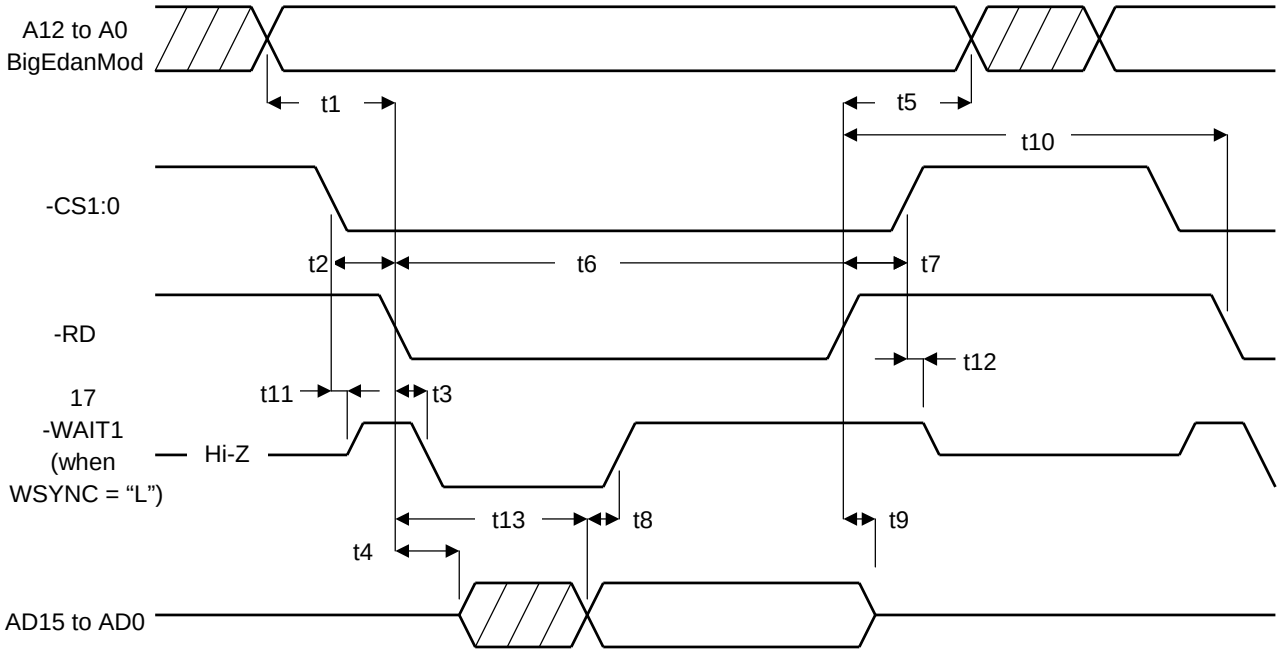
Note 1: The above values show the design target values.

Note 2: The delay time (t9) from when -RD is disabled until when AD15:AD0 are set to Hi-Z is 25ns maximum. If a write access is made following a read access and the write data is output fast, a bus conflict may occur due to this delay time. In this case, it is necessary to insert an idle cycle of one clock cycle or more between the access cycles.

Note 3: The delay time (t3) from when -RD is enabled until when -WAIT1 is determined is 30 ns maximum. Insert software wait as necessary to ensure that the microcontroller can recognize -WAIT1.

Note 4: The specification of -WAIT1 indicates a case where WSYNC = “L.” For the timing specification when WSYNC = “H,” see (6), "Clock Synchronization WAIT Signal Specification."

Note 5: If the CLKSTOP bit of the RstClkCtl register is "1," the -WAIT signal is not asserted when accessing the common registers (offsets 000h to 01Ch). t13 indicates the delay in output of valid data in this case. Insert software wait in case the microcontroller that does not have sufficient setup time for valid data.


A12 to A0
BigEdanMod
t1
t5
t10
-CS1:0
t2
t6
t7
-RD
t12
17
-WAIT1
(when
WSYNC = “L”)
t11
t3
Hi-Z
t13
t8
t9
t4
AD15 to AD0

(2) Separate Bus, Write (Microcontroller → ML60842) Specification

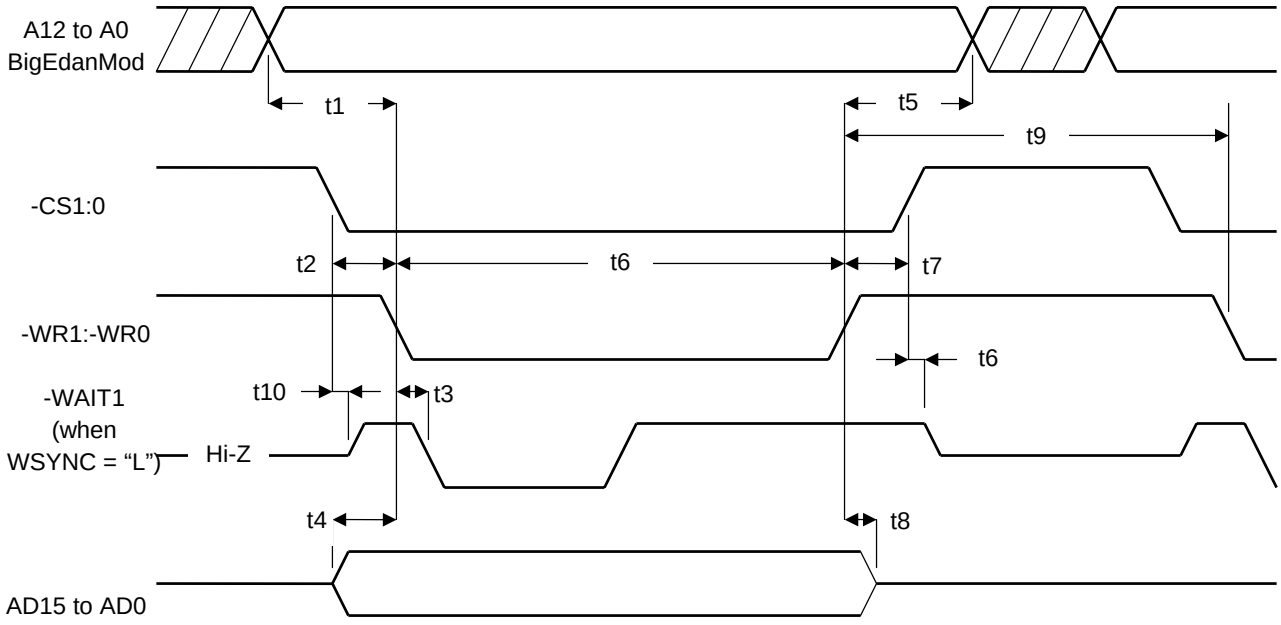
($A1V_{DD}$, $A2V_{DD}$ = 3.0 to 3.1 V, DV_{DD} = 2.7 to 2.9 V, GND = 0 V, Ta = -10 to +80°C, load capacity 20 pF)

Item	Symbol	MIN	MAX	Unit
Setup time of A12:A0 and BigEdanMod for -WR1:-WR0	t1	10		ns
Setup time of -CS1:0 for -WR1:-WR0	t2	0		
Delay time from when -WR1:-WR0 are enabled until when -WAIT1 is determined	t3		30	
Setup time of AD15:AD0 for -WR1:-WR0	t4	0		
Hold time of AD12:A0 for -WR1:-WR0	t5	10		
-WR1:-WR0 pulse width	t6	42		
Hold time of -CS1:0 for -WR1:-WR0	t7	10		
Hold time of AD15:AD0 for -WR1:-WR0	t8	6.5		
Recovery time from when either -CS1:0 or -WR1:-WR0 are disabled until when both -CS1:0 and -WR1:-WR0 are enabled	t9	35		
Delay time from when both -CS1:0 are enabled until when -WAIT1 is not set to Hi-Z	t10	0	20	
Delay time from when one of -CS1:0 is disabled until when -WAIT1 is set to Hi-Z	t11		20	

Note 1: The above values show the design target values.

Note 2: The delay time (t3) from when -WR1:-WR0 are enabled until when -WAIT1 is determined is 30 ns maximum.
Insert software wait as necessary to ensure that the microcontroller can recognize -WAIT1.

Note 3: The specification of -WAIT1 indicates a case where WSYNC = "L." For the timing specification of -WAIT1:0 when WSYNC = "H," see (6), "Clock Synchronization WAIT Signal Specification."



(3) Multiplex Bus, Read (ML60842 → Microcontroller) Specification

($A1V_{DD}$, $A2V_{DD}$ = 3.0 to 3.1 V, DV_{DD} = 2.7 to 2.9 V, GND = 0 V, Ta = -10 to +80°C, load capacity 20 pF)

Item	Symbol	MIN	MAX	Unit
Hold time of AD15:AD0 and BigEdanMod for ALE falling edge	t1	10		ns
Setup time of -CS1:0 for -RD	t2	0		
Delay time from when -RD is enabled until when AD15:AD0 are output	t3	0		
Delay time from when -RD is enabled until when -WAIT1 is established	t4		30	
Delay time from when -RD is disabled until when AD15:AD0 is set to Hi-Z	t5	0	25	
-RD pulse width	t6	42		
Hold time of -CS1:0 for -RD	t7	0		
Delay time from when valid data is output to AD15:AD0 until when -WAIT1 is cancelled	t8	0		
Setup time of AD15:AD0 and BigEdanMod for ALE falling edge	t9	10		
Recovery time from when either -CS1:0 or -RD is disabled until when both -CS1:0 and -RD are enabled	t10	35		
ALE pulse width	t11	15		
Delay time from when ALE is disabled until when -RD is enabled	t12	10		
Delay time from when both -CS1:0 are enabled until when -WAIT1 is not set to Hi-Z	t13	0	20	
Delay time from when one of -CS1:0 is disabled until when -WAIT1 is set to Hi-Z	t14		20	
Delay time from when -RD is enabled if -WAIT1 is not asserted until when valid data is output to AD15:AD0	t15		35	

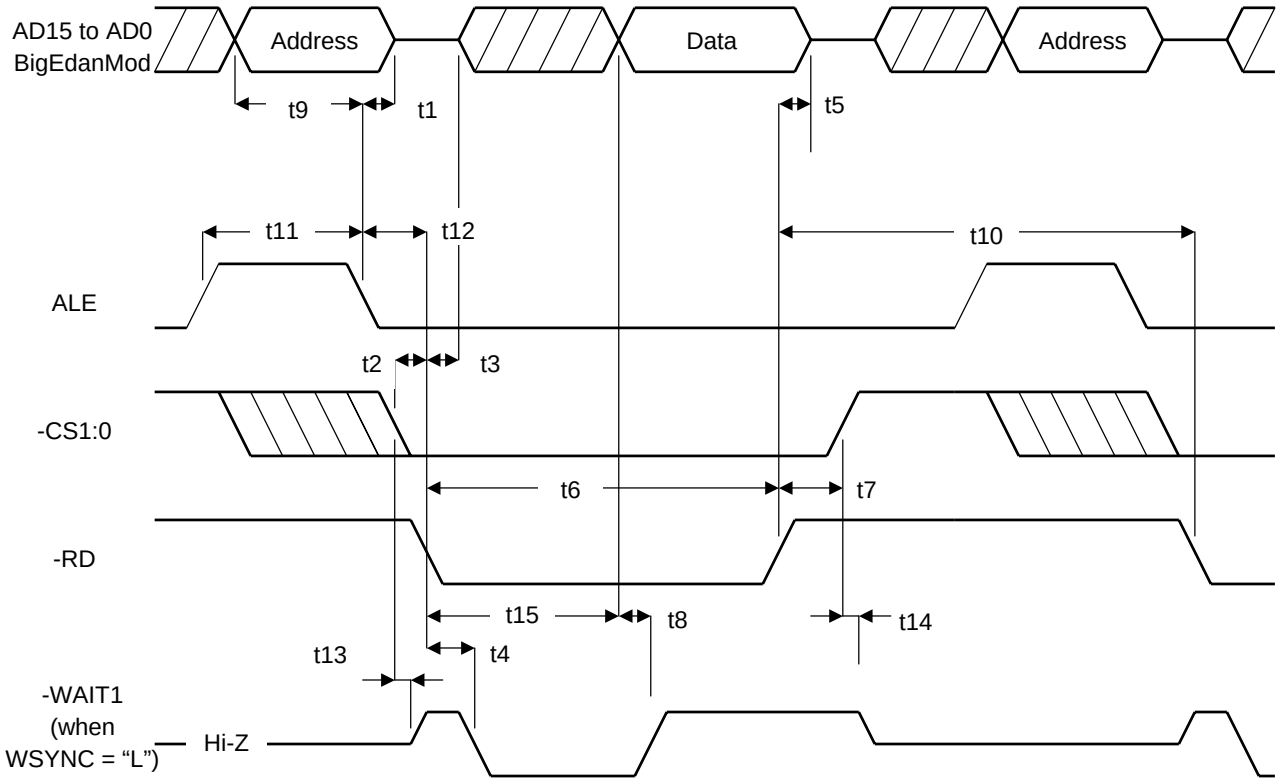
Note 1: The above values show the design target values.

Note 2: The delay time (t5) from when -RD is disabled until when AD15:AD0 are set to Hi-Z is 25 ns maximum. If a write access is made following a read access and the write data is output fast, a bus conflict may occur due to this delay time. In this case, it is necessary to insert an idle cycle of one clock cycle or more between the access cycles.

Note 3: The delay time (t4) from when -RD is enabled until when -WAIT1 is determined is 30 ns maximum. Insert software wait as necessary to ensure that the microcontroller can recognize -WAIT1.

Note 4: The specification of -WAIT1 indicates a case where WSYNC = “L.” For the timing specification of -WAIT1:0 when WSYNC = “H,” see (6), "Clock Synchronization WAIT Signal Specification."

Note 5: If the CLKSTOP bit of the RstClkCtl register is "1," the -WAIT signal is not asserted when accessing the common registers (offsets 000h to 01Ch). t15 indicates the delay in output of valid data in this case. Insert software wait in case the microcontroller that does not have sufficient setup time for valid data.

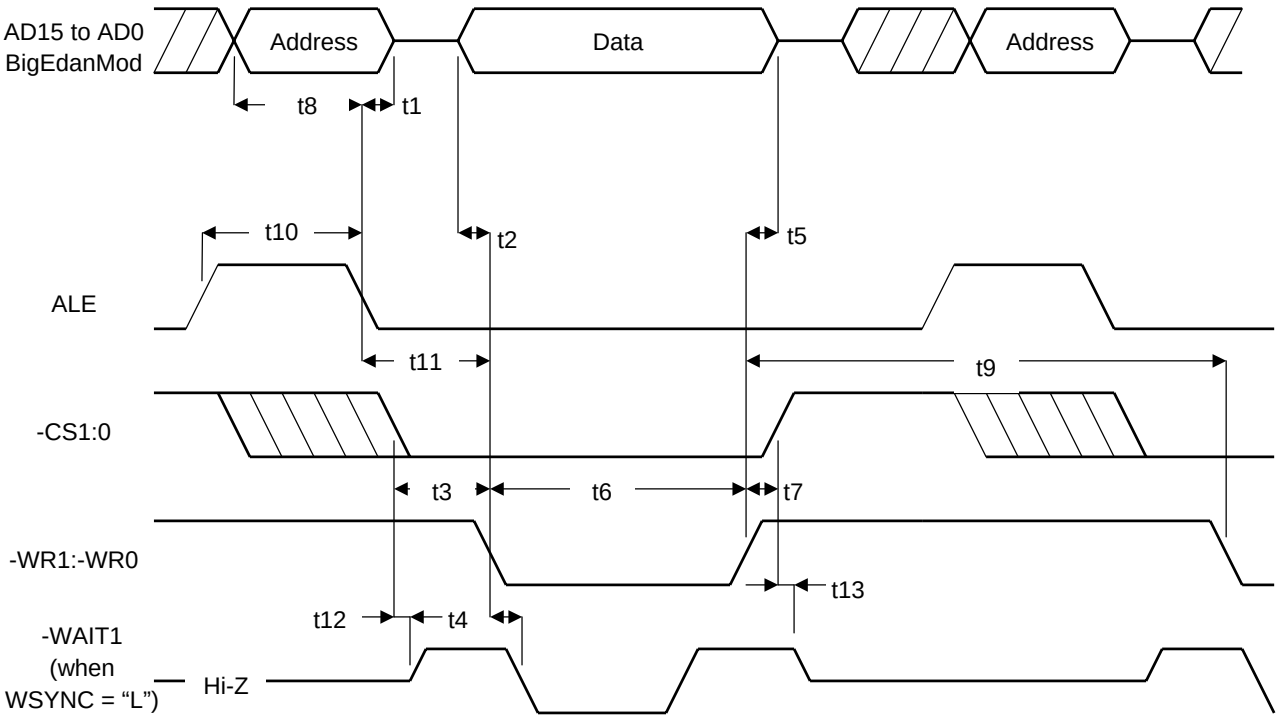

AD15 to AD0
BigEdanMod
Address
Data
Address
t9
t1
t5
t11
t12
t10
ALE
t2
t3
-CS1:0
t6
t7
-RD
t15
t8
t14
t13
t4
-WAIT1
(when
WSYNC = “L”)
Hi-Z

(4) Multiplex Bus, Write (Microcontroller → ML60842) Specification

($A1V_{DD}$, $A2V_{DD}$ = 3.0 to 3.1 V, DV_{DD} = 2.7 to 2.9 V, GND = 0 V, Ta = -10 to +80°C, load capacity 20 pF)

Item	Symbol	MIN	MAX	Unit
Hold time of AD15:AD0 and BigEdanMod for ALE falling edge	t1	10		ns
Setup time of AD15:AD0 for -WR1:-WR0	t2	0		
Setup time of -CS1:0 for -WR1:-WR0	t3	0		
Delay time from when -WR1:-WR0 are enabled until when -WAIT1 is determined	t4		30	
Hold time of AD15:AD0 for -WR1:-WR0	t5	6.5		
-WR1:-WR0 pulse width	t6	42		
Hold time of -CS1:0 for -WR1:-WR0	t7	10		
Setup time of AD15:AD0 and BigEdanMod for ALE falling edge	t8	10		
Recovery time from when either -CS1:0 or -WR1:-WR0 are disabled until when both -CS1:0 and -WR1:-WR0 are enabled	t9	35		
ALE pulse width	t10	15		
Delay time from when ALE is disabled until when -WR1:-WR0 are enabled	t11	10		
Delay time from when both -CS1:0 are enabled until when -WAIT1 is not set to Hi-Z	t12	0	20	
Delay time from when one of -CS1:0 is disabled until when -WAIT1 is set to Hi-Z	t13		20	

Note 1: The above values show the design target values.
Note 2: The delay time (t4) from when -RD is enabled until when -WAIT1 is determined is 30 ns maximum. Insert software wait as necessary to ensure that the microcontroller can recognize -WAIT1.
Note 3: The specification of -WAIT1 indicates a case where WSYNC = "L." For the timing specification when WSYNC = "H," see (6), "Clock Synchronization WAIT Signal Specification."



(5) DREQ Signal/DACK Signal Specification

There are two types of DREQ clear conditions for the ML60842 as follows:
- Clear by DACK response
- Clear by accessing the DMA request source

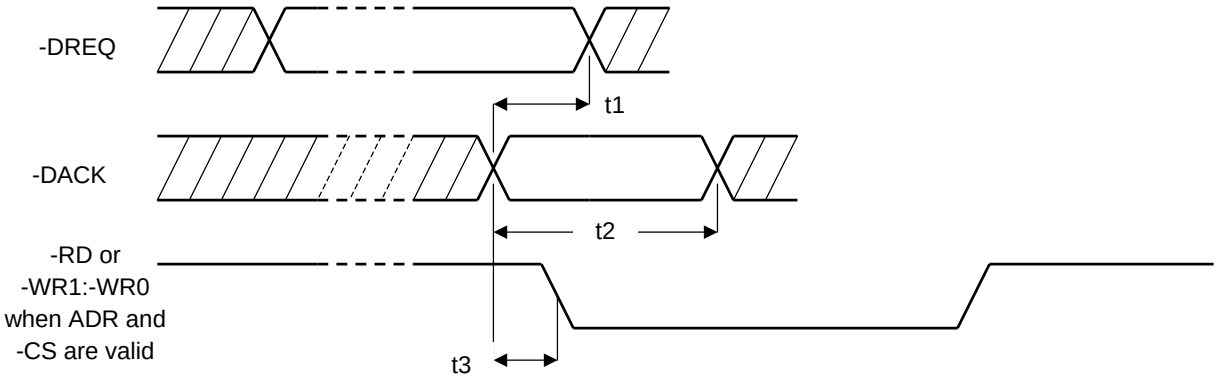
The following shows the AC specification in each case.

($A1V_{DD}$, $A2V_{DD}$ = 3.0 to 3.1 V, DV_{DD} = 2.7 to 2.9 V, GND = 0 V, Ta = -10 to +80°C, load capacity 20 pF)

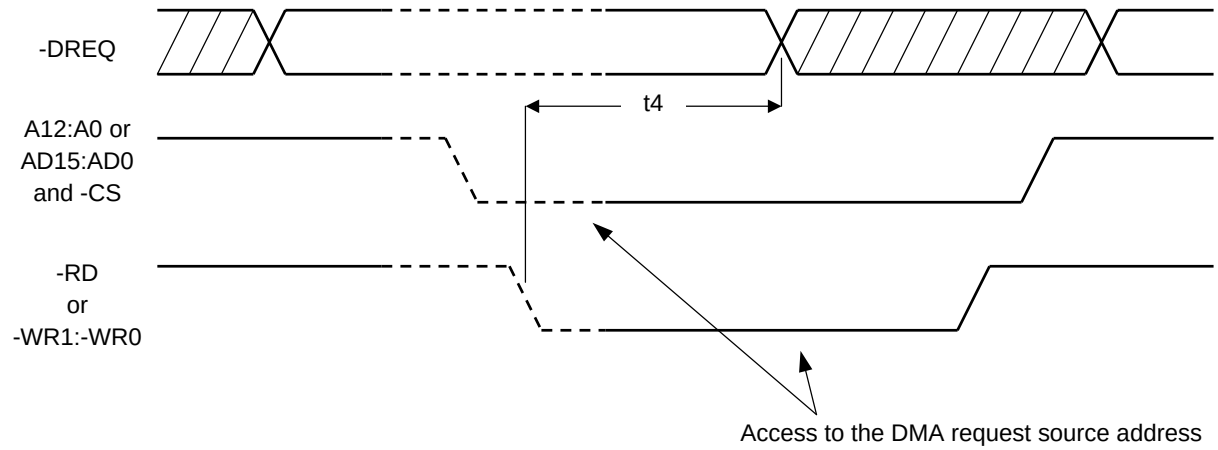
Item	Symbol	MIN	MAX	Unit
Delay time from when -DACK is enabled until when -DREQ is disabled	t1		20	ns
Minimum pulse width of -DACK	t2	30		
Time from when -DACK is enabled until when -CS1:0 and -RD or -WR1:0 are enabled	t3	0		
Delay time from when -RD or -WR1:-WR0 for the DMA request source address are enabled until when -DREQ is disabled	t4	TBD		

Note 1: The above values show the design target values.
Note 2: The time (t3) from when -DACK is enabled until when -CS01:0 and -RD or -WR1:0 are enabled is 0 ns minimum.
If an access occurs that enables -CS1:0 and -RD or -WR1:0 before -DACK is enabled, data transferred via DMA transfer cannot be guaranteed.

<Clear by DACK response>



<Clear by accessing the DMA request source>

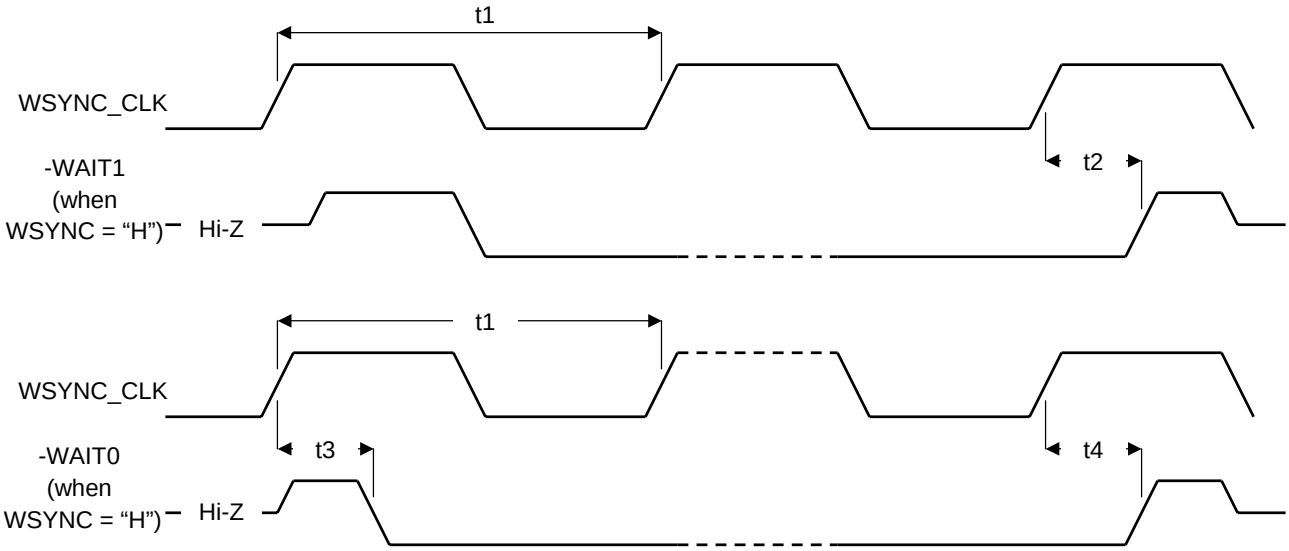


(6) Clock Synchronization WAIT Signal Specification

($A1V_{DD}$, $A2V_{DD}$ = 3.0 to 3.1 V, DV_{DD} = 2.7 to 2.9 V, GND = 0 V, Ta = -10 to +80°C, load capacity 20 pF)

Item	Symbol	MIN	MAX	Unit
Cycle of WSYNC_CLK	t1	30		ns
Delay time from the rising edge of WSYNC_CLK until when -WAIT1 is disabled	t2	3	18	
Delay time from the rising edge of WSYNC_CLK until when -WAIT0 is enabled	t3		15	
Delay time from the rising edge of WSYNC_CLK until when –WAIT0 is disabled	t4	3	18	

Note 1: The above values show the design target values.
Note 2: To sample -WAIT synchronously with WSYNC_CLK, sample it at the rising edge of WSYNC_CLK.
Note 3: The delay time (t2, t4) from the rising edge of WSYNC_CLK until when -WAIT1 and -WAIT0 are disabled is 3 ns minimum and 18 ns maximum. If the microcontroller does not have sufficient hold time for WAIT, verify that the operation of the microcontroller does not become abnormal (i.e., it recognizes WAIT as either active or inactive) in such a condition.
Note 4: The delay time (t3) from the rising edge of WSYNC_CLK until when -WAIT0 is enabled is 15 ns maximum. Insert software wait in case the microcontroller that does not have sufficient hold time for WAIT.
Note 5: For the timing specification to change to/from Hi-Z, see items (1) to (4) in this section.

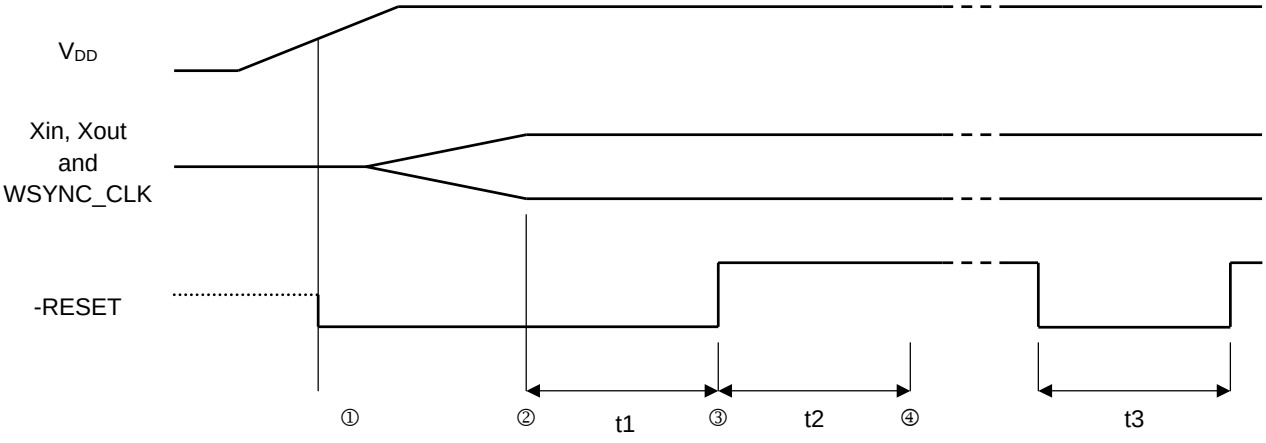


(7) RESET Signal Specification

($A1V_{DD}$, $A2V_{DD}$ = 3.0 to 3.1 V, DV_{DD} = 2.7 to 2.9 V, GND = 0 V, Ta = -10 to +80°C, load capacity 20 pF)

Item	Symbol	MIN	MAX	Unit
Time from when the oscillation of the oscillator stabilizes (48 MHz) and WSYNC_CLK is input (when WSYNC = "H") until when -RESET is deasserted	t1	50		µs
Time from when -RESET is deasserted until when the ML60842 becomes accessible	t2	50		
-RESET pulse width	t3	50		

Note 1: The above values show the design target values.
Note 2: Supply the WSYNC_CLK signal to the ML60842 before timing ② below (when WSYNC = "H").



① V_{DD} rises and the RESET signal is asserted.
② The oscillation of the oscillator stabilizes (48 MHz) and WSYNC _CLK is input.
The time until the oscillation of the oscillator stabilizes (① to ② above) varies depending on the oscillator used. Be sure to allocate sufficient time.
③ The RESET signal is deasserted.
Keep the RESET signal active at least 50 µs (② to ③ above) in order to initialize the ML60842.
④ T he internal setup of the ML60842 is complete and it is then accessible from the microcontroller.
Do not access the ML60842 before timing ④ above.

11. BASIC BUS CYCLES

(1) Separate Bus, PIO, Read (ML60842 → Microcontroller)

(TBD)

(2) Separate Bus, PIO, Write (Microcontroller → ML60842)

(TBD)

(3) Multiplex Bus, PIO, Read (ML60842 → Microcontroller)

(TBD)

(4) Multiplex Bus, PIO, Write (Microcontroller → ML60842)

(TBD)

(5) Separate Bus, DMA, Read (ML60842 → Microcontroller)

(TBD)

(6) Separate Bus, DMA, Write (Microcontroller → ML60842)

(TBD)

(7) Multiplex Bus, DMA, Read (ML60842 → Microcontroller)

(TBD)

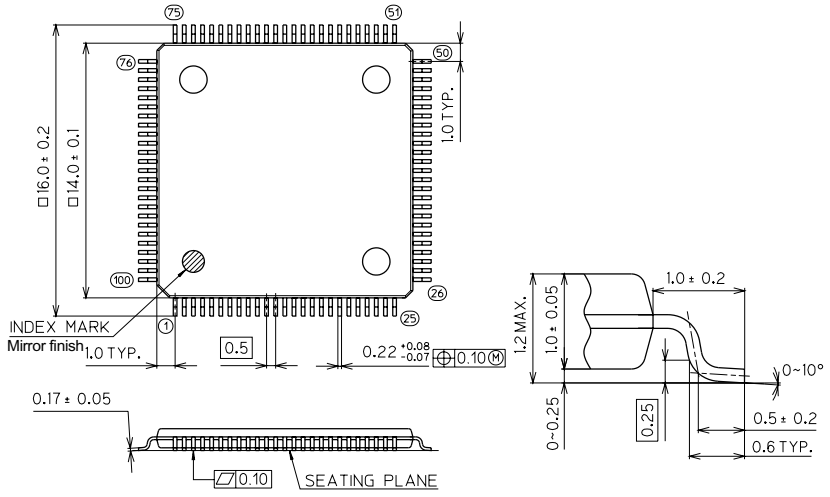
(8) Multiplex Bus, DMA, Write (Microcontroller → ML60842)

(TBD)

12. PACKAGE DIMENSIONS

(Unit:mm)

TQFP100-P-1414-0.50-K

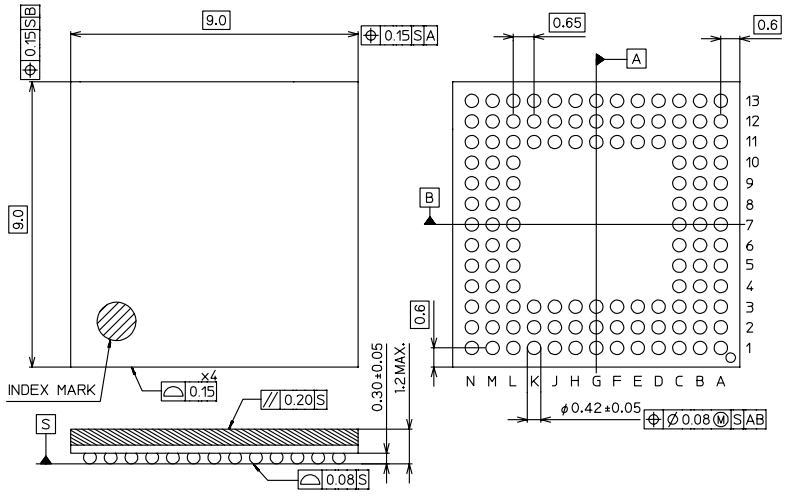


5

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

(Unit:mm)

P-TFBGA120-0909-0.65



5

Package material	Epoxy resin
Ball material	Sn/Pb
Package weight (g)	0.16 TYP.
Rev. No./Last Revised	1/Mar. 11, 2002

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL60842-01	Jul. 18, 2003	–	–	Preliminary edition 1
PEDL60842-02	Oct. 31, 2003			Explanation of the register of OHCI is added

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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