OKI Semiconductor

This version: Jan. 1998
Previous version: Dec. 1996

MSM548331

222,720-Word × 12-Bit Field Memory

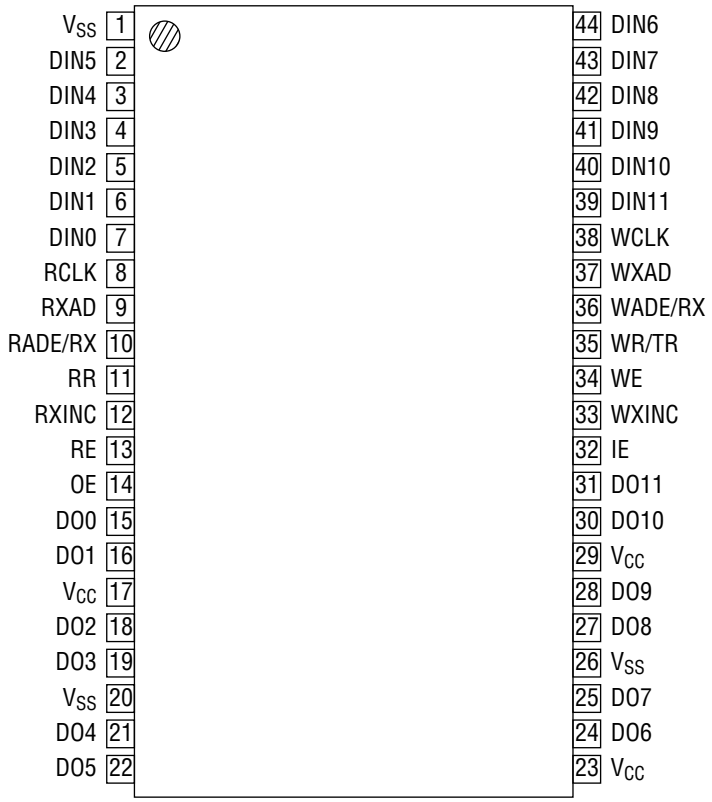
DESCRIPTION

The MSM548331 is a 2.7-Mbit, 768 bits × 290 lines, Field Memory. Access is done line by line. The line address must be set each time a line is changed.
More than two MSM548331s can be cascaded directly without any delay devices between them. Cascading MSM548331s provides larger capacity and longer delay.
X serial address input enables random initial address setting of serial access in a page. Other than the random address setting, MSM548331 has several types of address set modes such as line hold, address jump to initial address and line increment.
Self refresh function releases the MSM548331 from being applied external refresh control clocks even though it contains dynamic type memory cells. MSM548331 has write mask function or input enable function (IE), and read-data skipping function or output enable function (OE).
The MSM548331 is especially designed for digital TVs and VTRs for consumer use and video cameras.
The MSM548331 is not designed for high end use in such applications as medical systems, professional graphics systems which require long term picture storage, data storage systems and others.

FEATURES

- 768 × 290 × 12-bit configuration
- Line by line access
- X serial address inputs for random serial initial bit address
- Asynchronous operation
- Serial read and write cycle times
  - Read cycle: 30 ns
  - Write cycle: 30 ns
- Low operating supply voltage: 3.3 V ±0.3 V
- Self-refresh
- Various address reset mode for picture processing
- Write mask function (Input enable control)
- Data skipping function (Output enable control)
- Package:
  44-pin 400 mil plastic TSOP (Type II) (TSOPII44-P-400-0.80-K) (Product : MSM548331TS-K)

PIN CONFIGURATION (TOP VIEW)

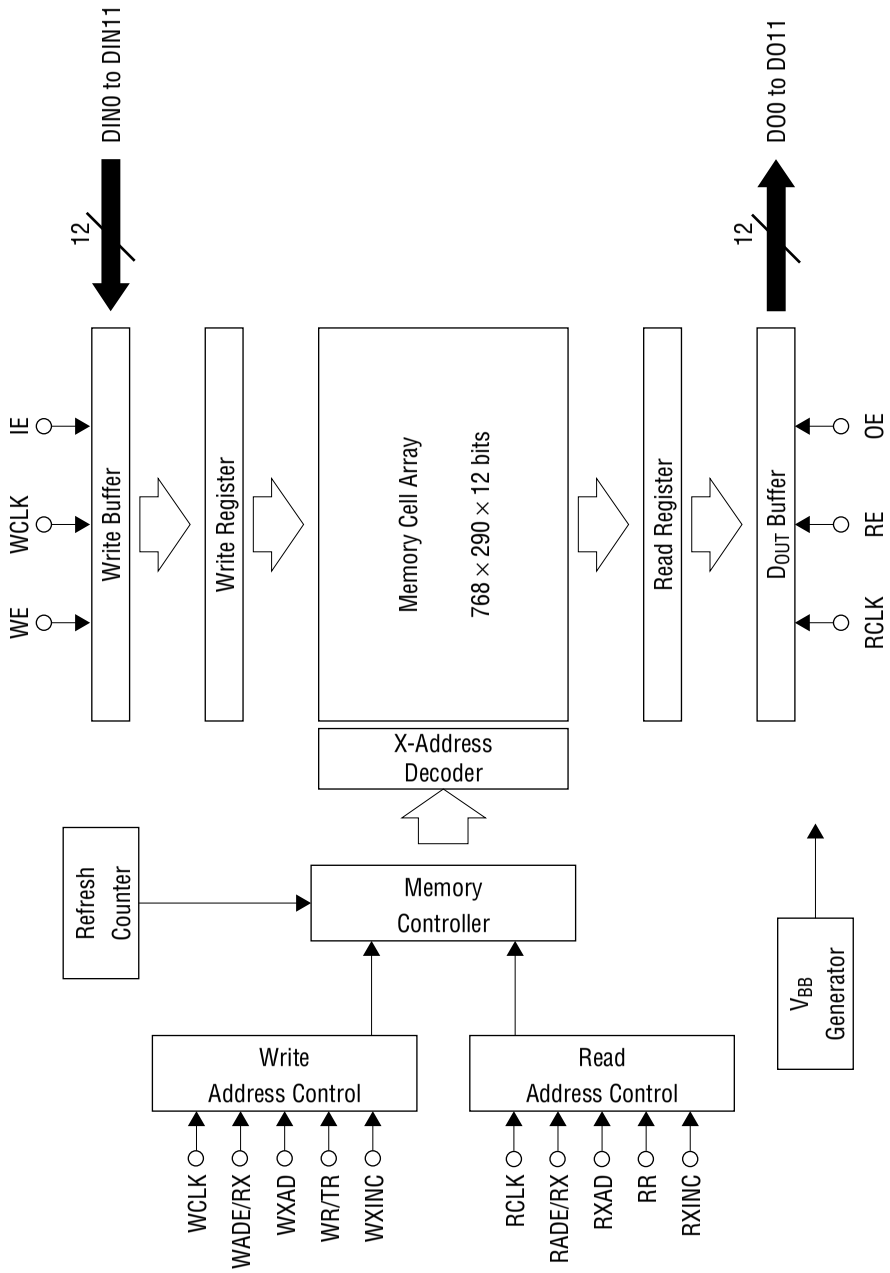


44-Pin Plastic TSOP (II)
(K Type)

Pin Name	Function	
	Address Setting Cycle	Serial Read/Write Cycle
RCLK	Read Port, X Serial Address Strobes	Read Port, Serial Read Clock
RE	—	Read Port, Read Enable
DO0 - 11	—	Read Port, Data Output
RR	Read Port, Address Reset Mode Enable	—
RXINC	Read Port, X Address Increment	—
RADE/RX	Read Port, X Address Input Enable Read Port, X Address Reset	—
RXAD	Read Port, X Serial Address Data	—
OE	—	Output Enable
WCLK	Write Port, X Serial Address Strobes	Write Port, Serial Write Clock
WE	—	Write Port, Write Enable
DIN0 - 11	—	Write Port, Input Data
WR/TR	Write Port, Address Reset Mode Enable	Write Port, Write Data Transfer
WXINC	Write Port, X Address Increment	—
WADE/RX	Write Port, X Address Input Enable Write Port, X Address Reset	—
WXAD	Write Port, X Serial Address Data	—
IE	—	Input Enable
V_{CC}	Power Supply Voltage (3.3 V)	
V_{SS}	Ground (0 V)	

Note: Same power supply voltage level must be provided to every V_{CC} pin.
Same ground voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



PIN FUNCTION

READ RELATED

RCLK : Read Clock
RCLK is the read control clock input. Synchronized with RCLK's rising edge, serial read access from read ports is executed when both RE and OE are high.
The internal counter for the serial read address is incremented automatically on the rising edge of RCLK. In a read address set cycle, all the read address bits which were input from RXAD pin are stored into internal address registers synchronized with RCLK. In this address set cycle, RADE/RX must be held high and RR must be held low.
In the read address reset cycle, various read address reset modes can be set synchronously with RCLK. These reset cycles work to replace complicated serial address control which requires many RCLK clocks with a simple reset cycle control requiring only a single RCLK cycle. It greatly facilitates memory access.

RE : Read Enable
RE is a read enable clock input. RE enables or disables both internal read address pointers and data-out buffers. When RE is high, the internal read address pointer is incremented synchronously with RCLK. When RE is low, even if the RCLK is input, the internal read address pointer is not incremented.

OE : Output Enable
OE is an output enable clock input. OE enables or disables data-outs. OE high level enables the outputs. The internal read address pointer is always incremented by cycling RCLK regardless of OE level.

DO0-11 : Data-Outs
DO0-11 are serial data-outs. Data is output synchronously with RCLK when OE is high. The output enable/disable operation through OE input is performed synchronously with OE and asynchronously with RCLK.

RR : Read Reset
RR is a read reset control input. Read address reset modes are defined when RR level is high according to the "FUNCTION TABLE for read".

RXINC : Read X Address Increment
RXINC is a read X address (or line address) increment control input. In the read address reset cycle, defined by RR high, the X address (or line address) is incremented by 1 when RXINC is pulled high with RADE/RX low.

RADE/RX : Read Address Enable/Read X Address Reset Logic Function
RADE/RX is a dual function control input. RADE, one of the two functions of RADE/RX, is a read address enable input. In the read address set cycle, defined by RR high, X address (or line address) input from the RXAD pin are latched into internal read X address register synchronously with RCLK. RX, the second function of RADE/RX, works as an element to set read X address (or line address) reset mode. In an address reset mode cycle, defined by RR high, read X address is reset to 0 when RADE/RX is pulled high with RXINC low.

RXAD : Read X Address
RXAD is a read X address (or line address) input. RXAD specifies the line address. 9 bits of read X address data are input serially from RXAD.

WRITE RELATED

WCLK : Write Clock

WCLK is a write control clock input. Synchronized with WCLK's rising edge, serial write access into write ports is executed when WE is high and IE is high.
According to WCLK clocks, the internal counter for the serial address is incremented automatically. In a write address set cycle, all the write addresses which were input from WXAD are stored into internal address registers synchronously with WCLK. In this address set cycle, WADE/RX must be held high and WR/TR must be held low.
In the write address reset cycle, various write address reset modes can be set synchronously with WCLK. These reset cycles replace complicated serial address control with simple reset cycle control which requires only one WCLK cycle. It greatly facilitates memory access.

WE : Write Enable

WE is a write enable clock input. WE enables or disables both internal write address pointers and data-in buffers. When WE is high, the internal write address pointer is incremented synchronously with WCLK. When WE is low, even if WCLK is input, the internal write address pointer is not incremented.

DIN0-11 : Data-Ins

DIN0-11 are serial data-ins. Corresponding data-in-buffers are masked by IE.

WR/TR : Write Reset/Write Transfer

WR/TR is a write reset control input. Write address reset modes are defined when WR/TR level is high according to the "FUNCTION TABLE for write".
When the write operation on a line is terminated, be sure to perform a write transfer operation by WR/TR in order to store the written data in the write register to corresponding memory cells.

WXINC : Write X Address Increment

WXINC is a write X address (or line address) increment control input. In the write address reset cycle, defined by WR/TR high, the write X address (or line address) is incremented when WXINC and WADE/RX are high.

WADE/RX : Write Address Enable/Write X Address Reset Logic Function

WADE/RX is a dual functional control input. WADE, one of the two functions of WADE/RX, is a write address enable input. In the write address reset cycle, defined by WR/TR high, X address (or line address) input from WXAD is latched into internal write X address register synchronously with WCLK.

WXAD : Write X Address

WXAD is a write X address (or line address) input. WXAD specifies line address. 9 bits of write X address data are input serially from WXAD.

IE : Input Enable

IE is an input enable which controls the write operation. When IE is high, the input operation is enabled. When IE is low, the write operation is masked. When WE signal is high, and IE low, the internal serial write address pointer is incremented on the rising edge of WCLK without actual write operations. This function facilitates picture in picture function in a TV system.

OPERATION MODE

Write

1. Write operation
   Before the write operation begins, X address (or line address) must be input to set the initial bit address for the following serial write access. When WE and IE are high, a set of serial 12-bit-width write data on DIN0-11 is written into write registers attached to the DRAM memory arrays temporarily on the rising edge of WCLK.
   Following 12-bit-width serial input data is written into the memory locations in the write register designated by an internal write address pointer which is advanced by WCLK. This enables continuous serial write on a line. When write clock WCLK and read clock RCLK are tied together and are controlled by a common clock or CLK, more than two MSM548331s can be cascaded directly without any delay devices between the MSM548331s because the read timing is delayed by one CLK cycle to the write timing. When the write operation on a line is terminated, be sure to perform a write transfer operation by WR/TR in order to store the written data in the write registers to the corresponding memory cells in the DRAM memory arrays.

2. Write address pointer increment operation
   The write address pointer is incremented synchronously with WCLK when WE is high.

Relationship between the WE and IE input levels, Write Address pointer, and data input status

WCLK Rise		Internal Write Address Pointer	Data Input
WE	IE		
H	H	Incremented	Inputted
H	L		Not Inputted
L	—	Stopped	

When WE and IE are high, the write operation is enabled.
If IE level goes low while WCLK is active, the write operation is halted but the write address pointer will continue to advance. That is, IE enables a write mask function. When WE goes low, the write address pointer stops without WCLK.

Read

1. Read operation
   Before the read operation begins, the X address (or line address) must be input for setting initial bit address for the following serial read access.
   When both RE and OE are high, a set of serial 12-bit-width read data on DO0-11 pins is read from read registers attached to DRAM memory arrays on the rising edge of RCLK.
   Each access time is specified by the rising edges of RCLK.

2. Read address pointer increment operation
   The read address pointer is incremented synchronized with RCLK when OE level is high.

Relationship between the RE and OE input levels,
Read Address pointer, and data output status

RCLK Rise		Internal Read Address Pointer	Data Output
RE	OE		
H	H	Incremented	Outputted
H	L		Hi-Z
L	H	Stopped	Outputted
L	L		Hi-Z

When each read address pointer reaches the last address of a line, it stops at the last address and no address increment occurs.

Initial Address Setting (Write/Read Independent)

Any read operations are prohibited in the read initial address set period. Similarly, any write operations are prohibited in the write initial address set period. Note that read initial address set and write initial address set can occur independently. Similarly, read access can be achieved independently from write initial address set period and write access can be achieved independently from read initial address set cycles.

1. Write address setting
   WADE/RX enables initial read address inputs. When WADE/RX is high, 9 bits of serial X address (or line address) are input from WXAD.
   The operations above enable selection of specific lines randomly and enables the start of serial write access synchronized with write clock WCLK. Address for each line must be input between each line access. In other words, MSM548331's write is achieved in a "line by line" manner. Any write operations are prohibited in the initial write address set periods.
   Serial write input enable time t_{SWE} must be kept for starting a serial write just after the initial write address set period.

2. Read address setting
   RADE/RX enables initial read address inputs.
   When RADE/RX is high, 9 bits of serial X address (or line address) are input from RXAD.
   The operations above enable selection of specific lines randomly and enables the start of serial read access synchronized with read clocks, RCLK. Address for each line must be input between each line access. In other words, MSM548331's read operation is achieved in "line by line" manner.
   Any read operations are prohibited in the initial read address set periods. Serial read operations are prohibited while RADE/RX is high. Serial read port enable time t_{SRE} must be kept for starting a serial read just after the initial read address set period.

Initial Address Reset Modes (Write/Read Independent)

The initial address reset modes replace complicated read or write initial address settings with simple reset cycles. Initial address reset modes are selected by RR high during read and WR/TR high during write. As in normal read or write address settings, any read operations are prohibited in the read address reset cycles. Similarly, any write operations are prohibited in the initial write address reset cycles. Note that read initial address reset and write initial address reset can occur independently. Similarly, read access can be achieved independently from write initial address reset cycles and write

access can be achieved independently from read initial address reset cycles.
Input addresses are stored into address registers which are connected with address counter which controls address pointer operation. In the serial access operation, the input address into the address registers are kept.
Serial write data input enable time t_{SWE} and serial read port read enable time t_{SRE} must be kept for starting serial read or write just after the initial read or write address reset cycles.
Refer to the "FUNCTION TABLE" shown later.

1. Line hold operation (read only)
   By the "Line hold operation" logic which is composed by a combination of control inputs' level, access is executed starting from the first word on the current line.

2. Original address reset operation
   By the "Original address reset" logic, the address counter is reset to (0,0). After the reset mode, serial access starts from the address (0,0) .
   The address counter is reset by this reset mode but the address register, which stored input address in the previous address reset cycle or address set cycle, is not reset. The non-initialized address can be used as a preset address in "address jump reset" mode.

3. Line increment operation
   By the "Line increment operation" logic, the X address counter is incremented by one from the current X address. That is, serial access from the Y = (0) on the next line is enabled.

4. Address jump operation
   By the "Address jump operation" logic, a jump may be caused to the initialized line address.

Note : During one reset setting cycle, a plurality of resets cannot be set.

Power ON
Power must be applied to RCLK, RE, OE, WCLK, WE and IE input signals to pull them "Low" before or when the V_{CC} supply is turned on.
After power-up, the device is designed to begin proper operation in at least 200 µs after V_{CC} has reached the specified voltage. After 200 µs, a minimum of one line dummy write operation and read operation is required according to the address setting mode, because the read and write address pointers are not valid after power-up.

New Data Read Access
In order to read out "new data', the delay between the beginning of a write address setting cycle and read address setting cycle must be at least two lines.

Old Data Read Access
In order to read out "old data", the delay between the beginning of a write address setting cycle and read address setting cycle must be more than 0 but less than a half line.

FUNCTION TABLE

1. Write

Mode	No.	Description of Operation	WR/TR	WXINC	WADE/RX	Internal Address Pointer
Address Reset Mode	1	Write Transfer	H	L	L	
	2	Reset	H	L	H	X address cleared to (0, 0)
	3	Line Increment	H	H	L	X address increment to (Xn + 1, 0)
	4	Address Jump	H	H	H	X address jump to (Xi, 0)
Address Setting Mode	—	First Address Setting	L	L	H	X address set

Note : For write, Line hold is not provided.

2. Read

Mode	No.	Description of Operation	RR	RXINC	RADE/RX	Internal Address Pointer
Address Reset Mode	1	Line Hold	H	L	L	X address holde to (Xn, 0)
	2	Reset	H	L	H	X address cleared to (0, 0)
	3	Line Increment	H	H	L	X address increment to (Xn + 1, 0)
	4	Adress Jump	H	H	H	X address jump to (Xi, 0)
Address Setting Mode	—	First Address Setting	L	L	H	X address set

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating
Pin Voltage	V_T	Ta = 25°C, with respect to V_{SS}	–0.5 to 4.6 V
Short Circuit Output Current	I_{OS}	Ta = 25°C	50 mA
Power Dissipation	P_D	Ta = 25°C	1 W
Operating Temperature	T_{opr}	—	0 to 70°C
Storage Temperature	T_{stg}	—	–55 to 150°C

Recommended Operating Conditions

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Power Supply Voltage	V_{SS}	0	0	0	V
"H" Input Voltage	V_{IH}	2.1	V_{CC}	V_{CC} + 0.3	V
"L" Input Voltage	V_{IL}	–0.5	0	0.8	V

DC Characteristics

(V_{CC} = 3.0 to 3.6 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition		Min.	Max.	Unit
"H" Output Voltage	V_{OH}	I_{OH} = –0.1 mA		2.2	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 0.1 mA		—	0.6	V
Input Leakage Current	I_{LI}	0 < V_I < V_{CC} Other input voltage 0 V		–10	10	µA
Output Leakage Current	I_{LO}	0 < V_O < V_{CC}		–10	10	µA
Power Supply Current (During Operation)	I_{CC1}	min. cycle	-50	—	50	mA
Power Supply Voltage (During Standby)	I_{CC2}	Input pin = V_{IL}/V_{IH}		—	10	mA

Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance	C_I	7	pF
Output Capacitance	C_O	7	pF

AC Characteristics (1/2)

Measurement Conditions: (V_{CC} = 3.3 V ±0.3 V, Ta = 0 to 70°C)

Parameter	Symbol	Min.	Max.	Unit
WCLK Cycle Time	t_{WCLK}	30	—	ns
WCLK "H" Pulse Width	t_{WWCLH}	13	—	ns
WCLK "L" Pulse Width	t_{WWCLL}	13	—	ns
Serial Write Address Input Active Setup Time	t_{WAS}	5	—	ns
Serial Write Address Input Active Hold Time	t_{WAH}	7	—	ns
Serial Write Address Input Inactive Hold Time	t_{WADH}	7	—	ns
Serial Write Address Input Inactive Setup Time	t_{WADS}	7	—	ns
Write Transfer Instruction Setup Time	t_{WTRS}	5	—	ns
Write Transfer Instruction Hold Time	t_{WTRH}	7	—	ns
Write Transfer Instruction Inactive Hold Time	t_{WTDH}	7	—	ns
Write Transfer Instruction Inactive Setup Time	t_{WTDS}	7	—	ns
Serial Write X Address Setup Time	t_{WXAS}	5	—	ns
Serial Write X Address Hold Time	t_{WXAH}	7	—	ns
Serial Write Data Input Enable Time	t_{SWE}	3000	—	ns
Write Instruction Setup Time	t_{WES}	5	—	ns
Write Instruction Hold Time	t_{WEH}	7	—	ns
Write Instruction Inactive Hold Time	t_{WEDH}	7	—	ns
Write Instruction Inactive Setup Time	t_{WEDS}	7	—	ns
Input Data Setup Time	t_{DS}	5	—	ns
Input Data Hold Time	t_{DH}	12	—	ns
WR/TR-WCLK Active Setup Time	t_{WRS}	5	—	ns
WR/TR-WCLK Active Hold Time	t_{WRH}	7	—	ns
WR/TR-WCLK Inactive Hold Time	t_{WRDH}	7	—	ns
WR/TR-WCLK Inactive Setup Time	t_{WRDS}	7	—	ns
WXINC-WCLK Active Setup Time	t_{WINS}	5	—	ns
WXINC-WCLK Active Hold Time	t_{WINH}	7	—	ns
WXINC-WCLK Inactive Hold Time	t_{WINDH}	7	—	ns
WXINC-WCLK Inactive Setup Time	t_{WINDS}	7	—	ns
WADE/RX-WCLK Active Setup Time	t_{WRXS}	5	—	ns
WADE/RX-WCLK Active Hold Time	t_{WRXH}	7	—	ns
WADE/RX-WCLK Inactive Hold Time	t_{WRXDH}	7	—	ns
WADE/RX-WCLK Inactive Setup Time	t_{WRXDS}	7	—	ns
IE Enable Setup Time	t_{IES}	5	—	ns
IE Enable Hold Time	t_{IEH}	7	—	ns
IE Disable Setup Time	t_{IEDS}	7	—	ns
IE Disable Hold Time	t_{IEDH}	7	—	ns

AC Characteristics (2/2)

Measurement Conditions: (V_{CC} = 3.3 V ±0.3 V, Ta = 0 to 70°C)

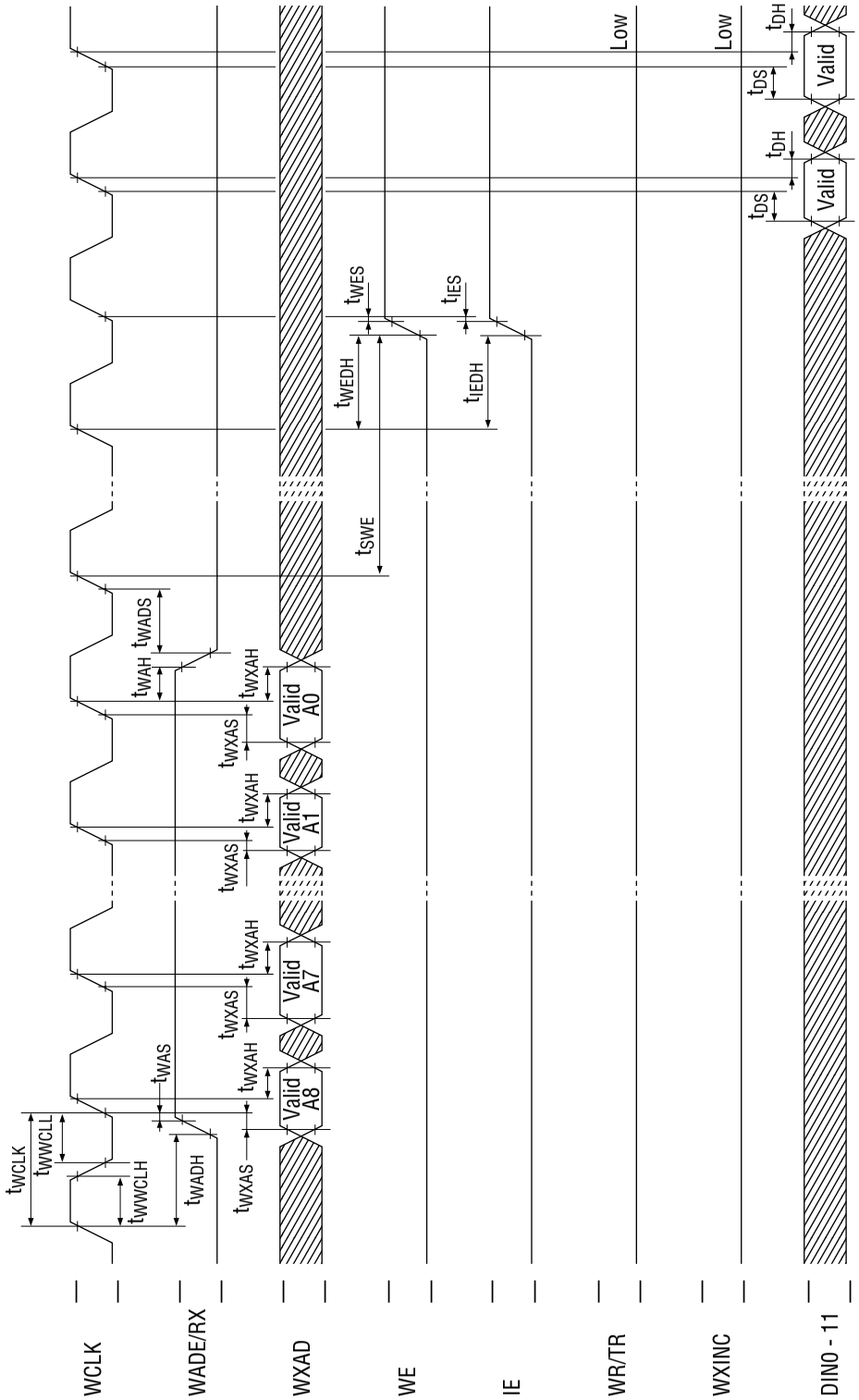
Parameter	Symbol	Min.	Max.	Unit
RCLK Cycle Time	t_{RCLK}	30	—	ns
RCLK "H" Pulse Width	t_{WRCLH}	13	—	ns
RCLK "L" Pulse Width	t_{WRCLL}	13	—	ns
Serial Read Address Input Active Setup Time	t_{RAS}	5	—	ns
Serial Read Address Input Active Hold Time	t_{RAH}	7	—	ns
Serial Read Address Input Inactive Hold Time	t_{RADH}	7	—	ns
Serial Read Address Input Inactive Setup Time	t_{RADS}	7	—	ns
Serial Read X Address Setup Time	t_{RXAS}	5	—	ns
Serial Read X Address Hold Time	t_{RXAH}	7	—	ns
RE Enable Setup Time	t_{RES}	5	—	ns
RE Enable Hold Time	t_{REH}	7	—	ns
RE Disable Hold Time	t_{REDH}	7	—	ns
RE Disable Setup Time	t_{REDS}	7	—	ns
Read Port Read Enable Time	t_{SRE}	3000	—	ns
Read Port Read Data Hold Time	t_{OH}	12	—	ns
Access Time from RCLK	t_{AC}	—	30	ns
Read Data Hold Time from OE	t_{DDOE}	2	—	ns
Access Time from OE	t_{DEOE}	—	20	ns
RR-RCLK Active Setup Time	t_{RRS}	5	—	ns
RR-RCLK Active Hold Time	t_{RRH}	7	—	ns
RR-RCLK Inactive Hold Time	t_{RRDH}	7	—	ns
RR-RCLK Inactive Setup Time	t_{RRDS}	7	—	ns
RXINC-RCLK Active Setup Time	t_{RINS}	5	—	ns
RXINC-RCLK Active Hold Time	t_{RINH}	7	—	ns
RXINC-RCLK Inactive Hold Time	t_{RINDH}	7	—	ns
RXINC-RCLK Inactive Setup Time	t_{RINDS}	7	—	ns
RADE/RX-RCLK Active Setup Time	t_{RRXS}	5	—	ns
RADE/RX-RCLK Active Hold Time	t_{RRXH}	7	—	ns
RADE/RX-RCLK Inactive Setup Time	t_{RRXDS}	7	—	ns
RADE/RX-RCLK Inactive Hold Time	t_{RRXDH}	7	—	ns
Transition Time (Rise and Fall)	t_T	2	30	ns

Note : Measurement conditions

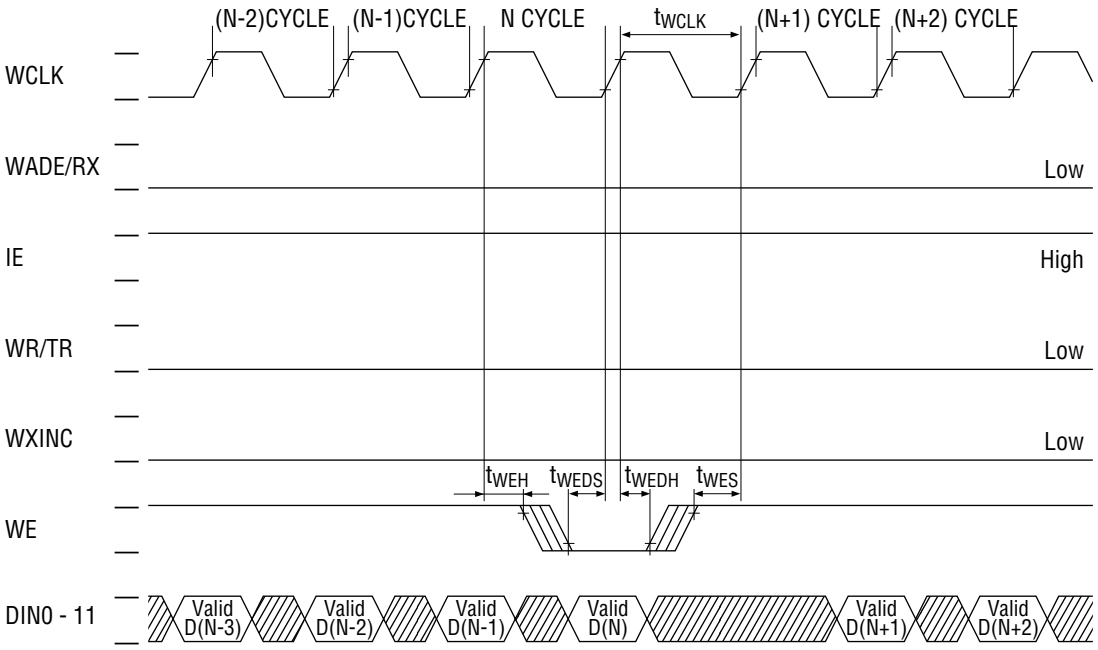
Input pulse level	: V_{IH} = 2.1 V, V_{IL} = 0.8 V
Input timing reference level	: V_{IH} = 2.1 V, V_{IL} = 0.8 V
Output timing reference level	: V_{OH} = 2.2 V, V_{OL} = 0.6 V
Input rise/fall time	: 2 ns
Load condition	: CL = 30 pF (Oscilloscope and tool capacity included)

TIMING WAVEFORM

Write Cycle (Address Setting Cycle)

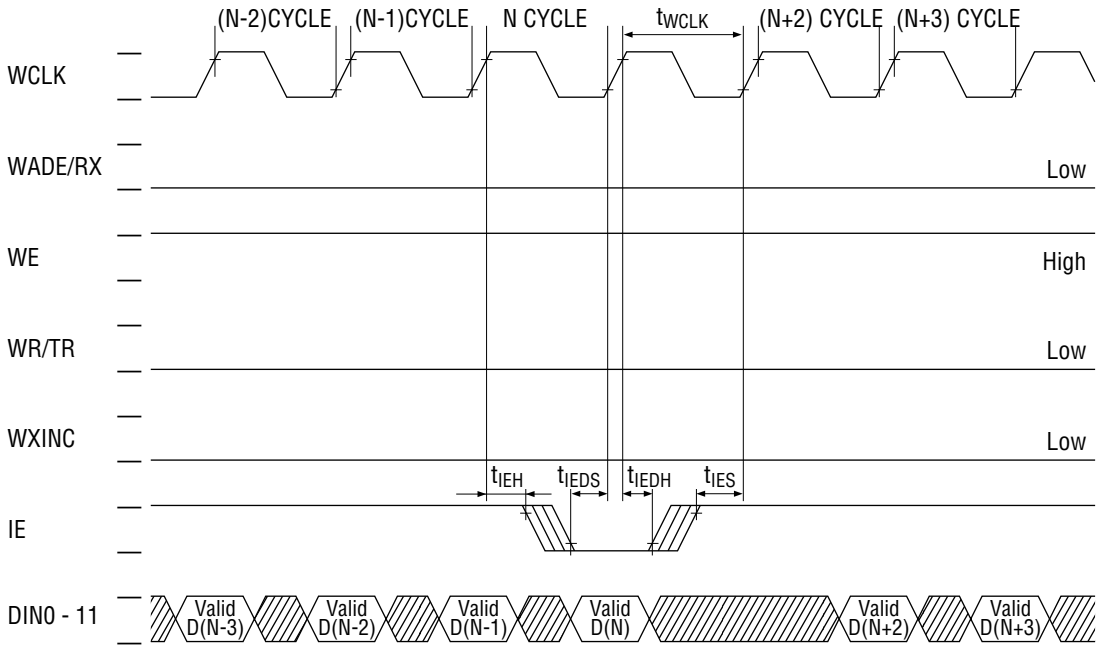


Write Cycle (WE Control)



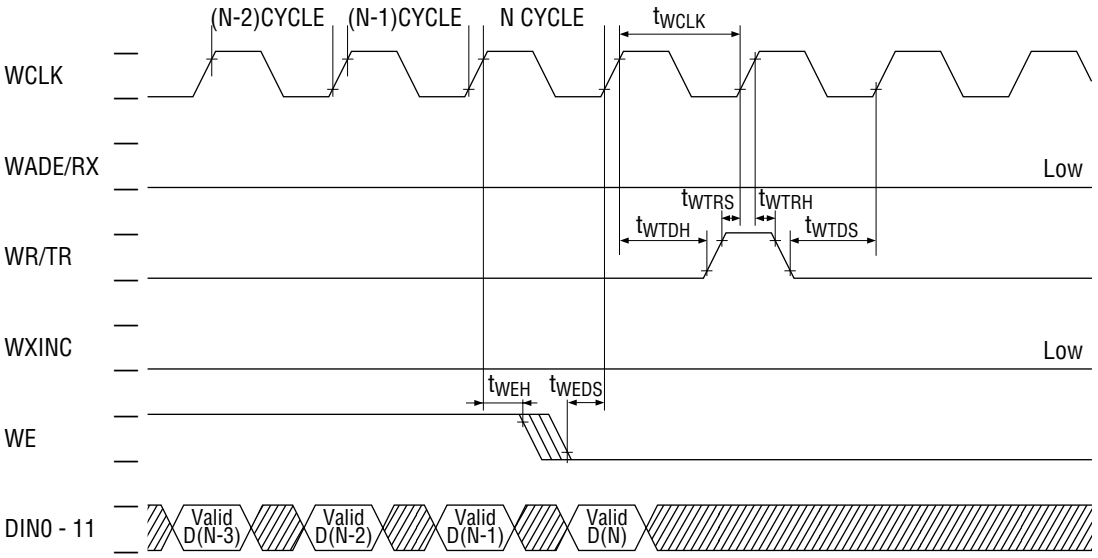
Note : In the WE = "L" cycle, the write address pointer is not incremented and no DIN data is written.

Write Cycle (IE Control)



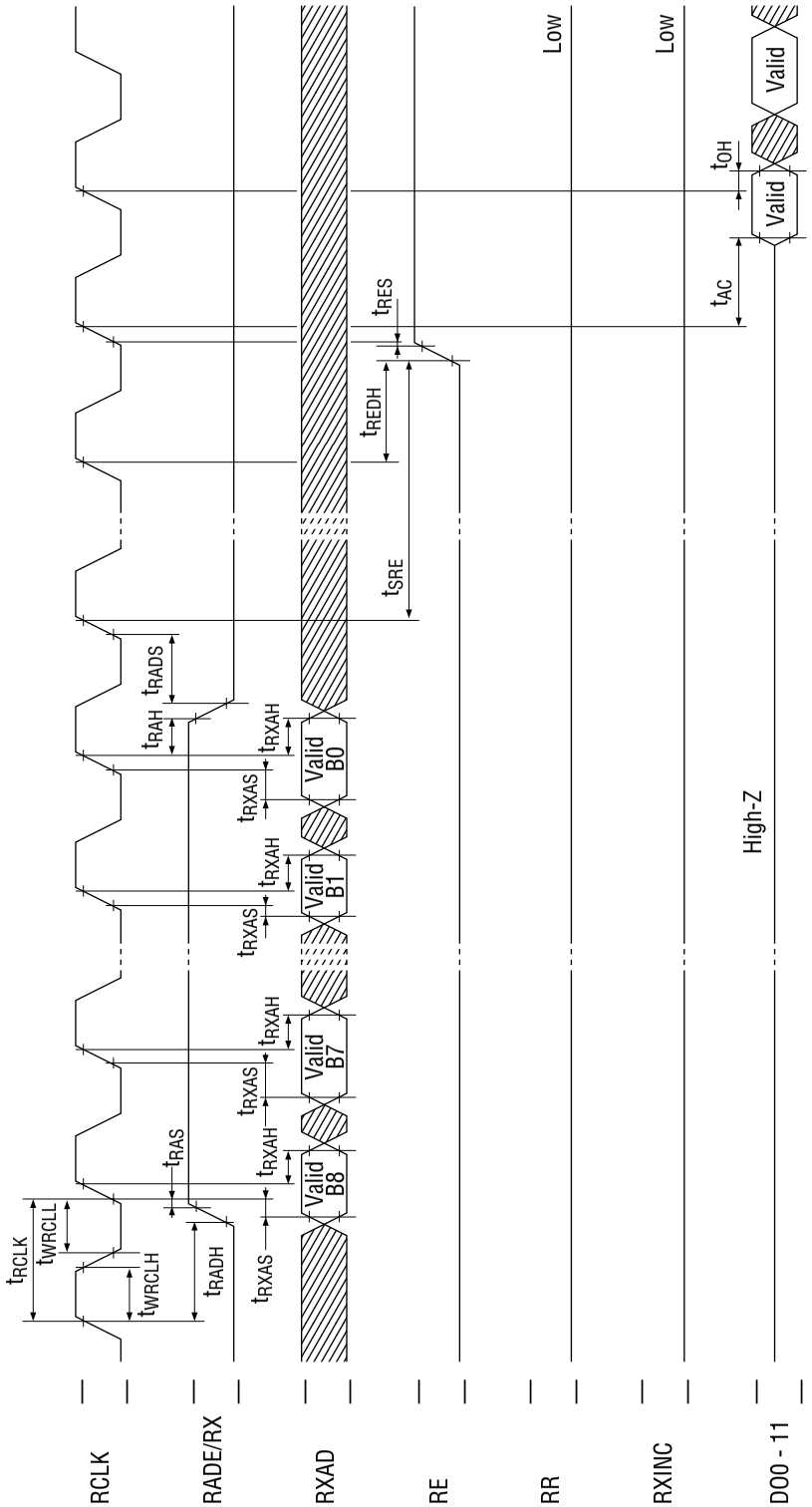
Note : In the IE = "L" cycle, the write address pointer is incremented, though no DIN data is written and the memory data is held.

Write Cycle (Write Transfer)

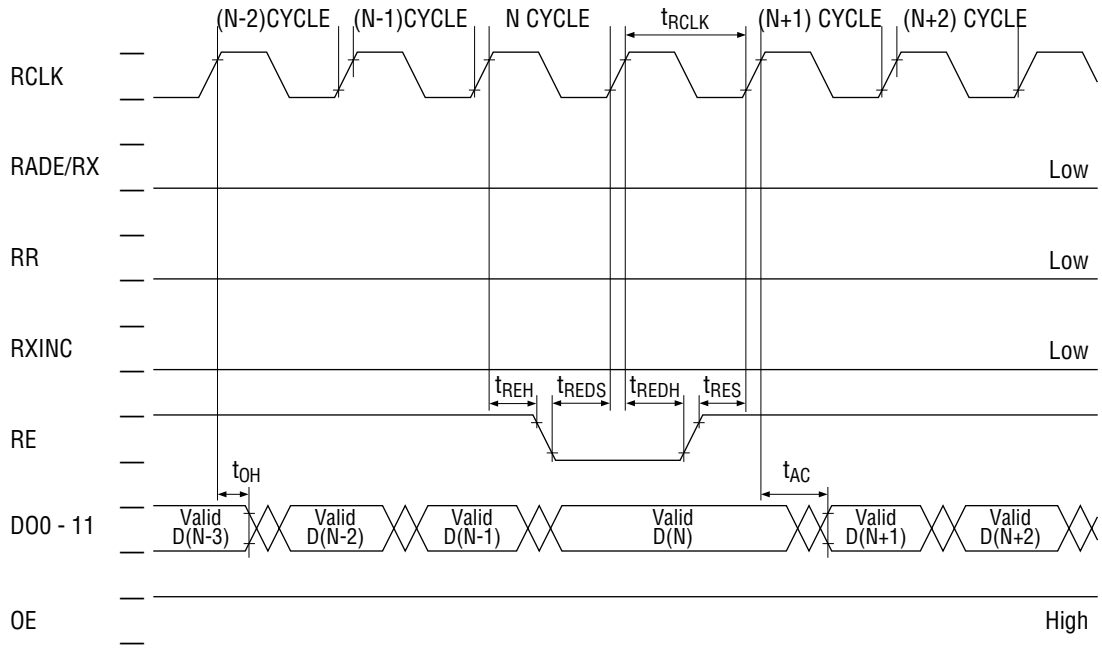


Note : When finishing the write operation on a line, be sure to perform a write transfer operation because the write data on the line is stored in the memory cell.

Read Cycle (Address Setting Cycle)

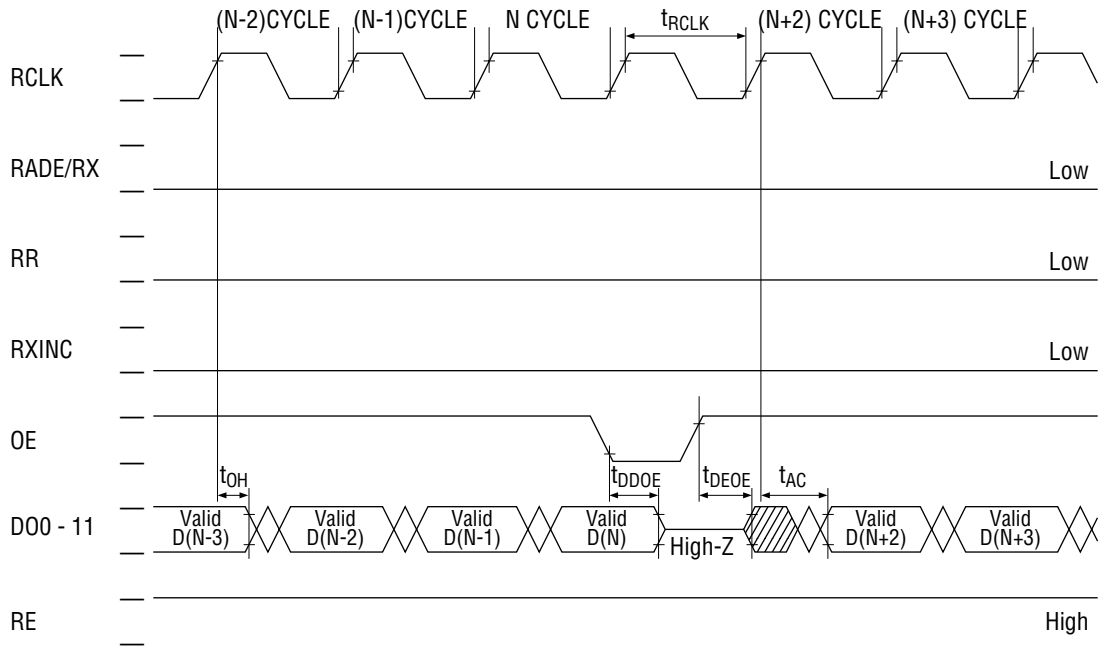


Read Cycle (RE Control)



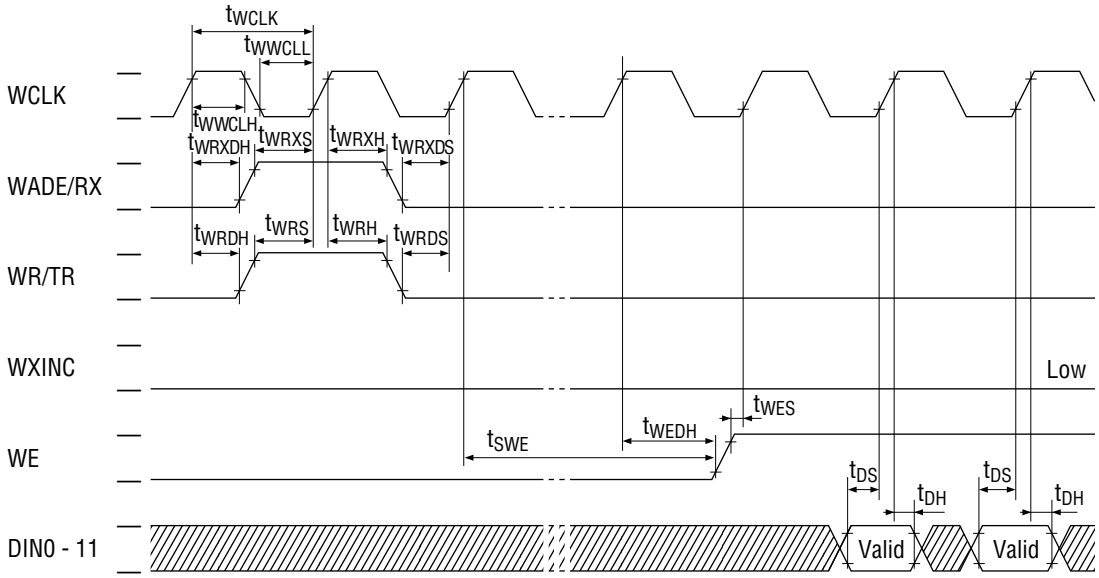
Note : In the cycle of RE = "L", the read address pointer is not incremented and the data at the address is output continuously.

Read Cycle (OE Control)



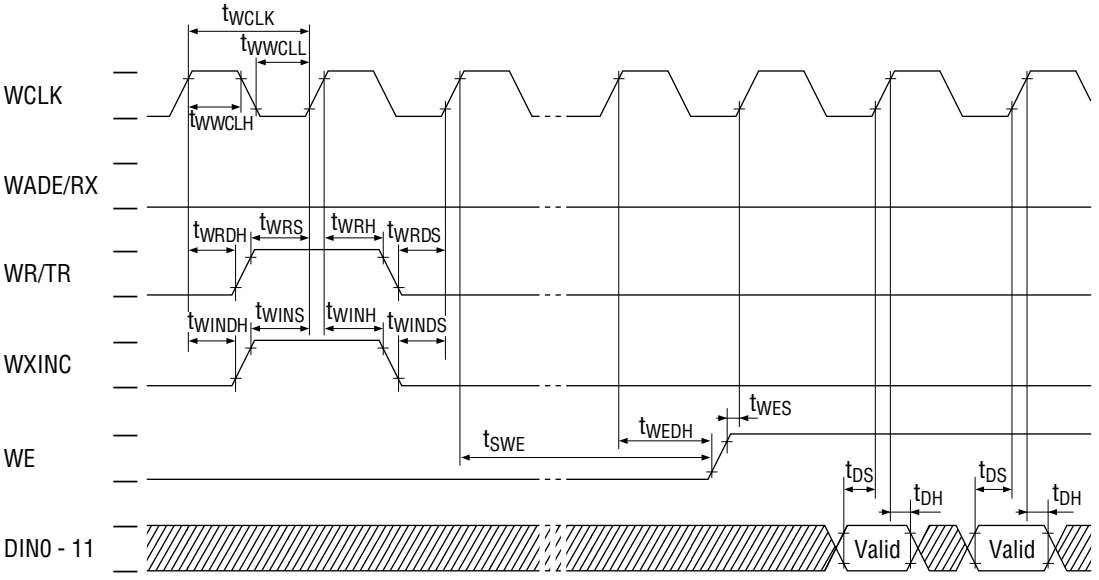
Note : In the cycle of OE = "L", the read address pointer is incremented and the output enters the high impedance state.

Write Reset Mode



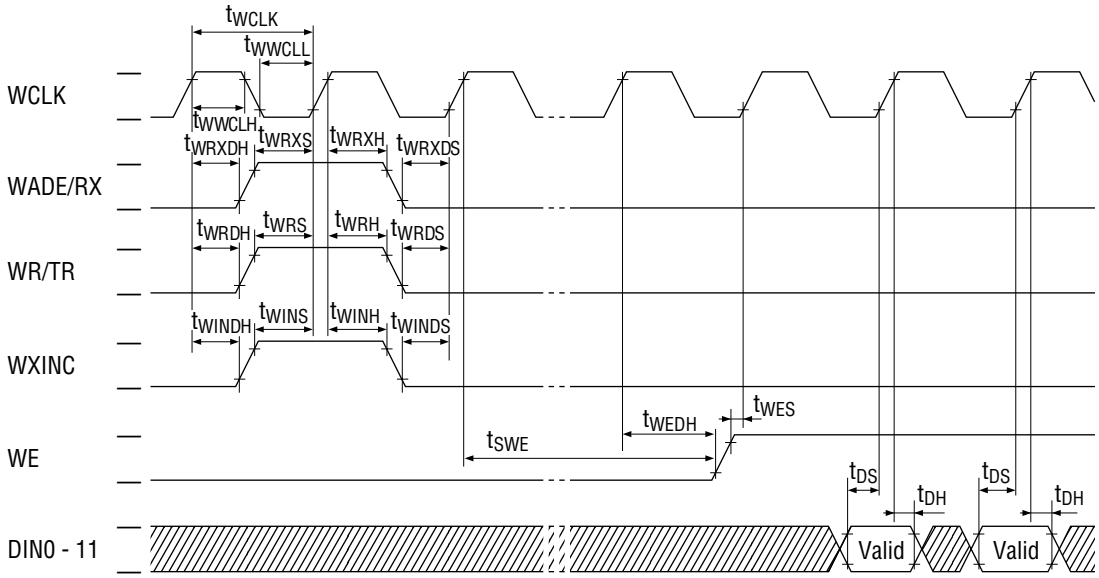
Note : Both the line address and word address are reset to 0.

Write Line Increment Mode



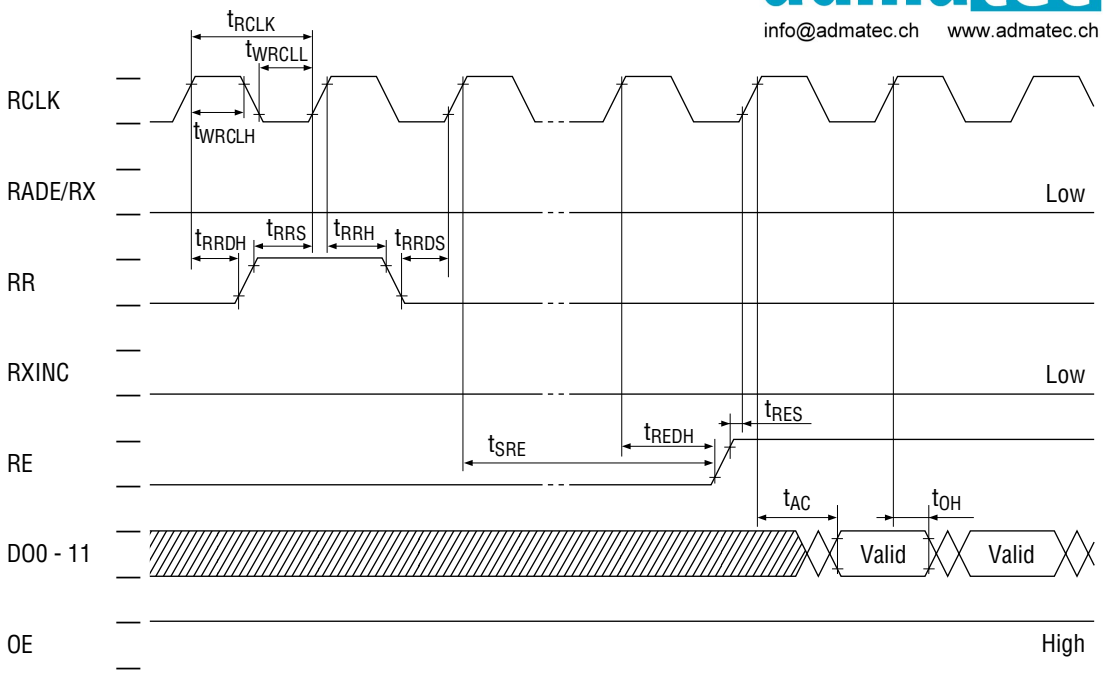
Note : The line address is incremented by 1 and the word address is reset to 0.

Write Address Jump Mode



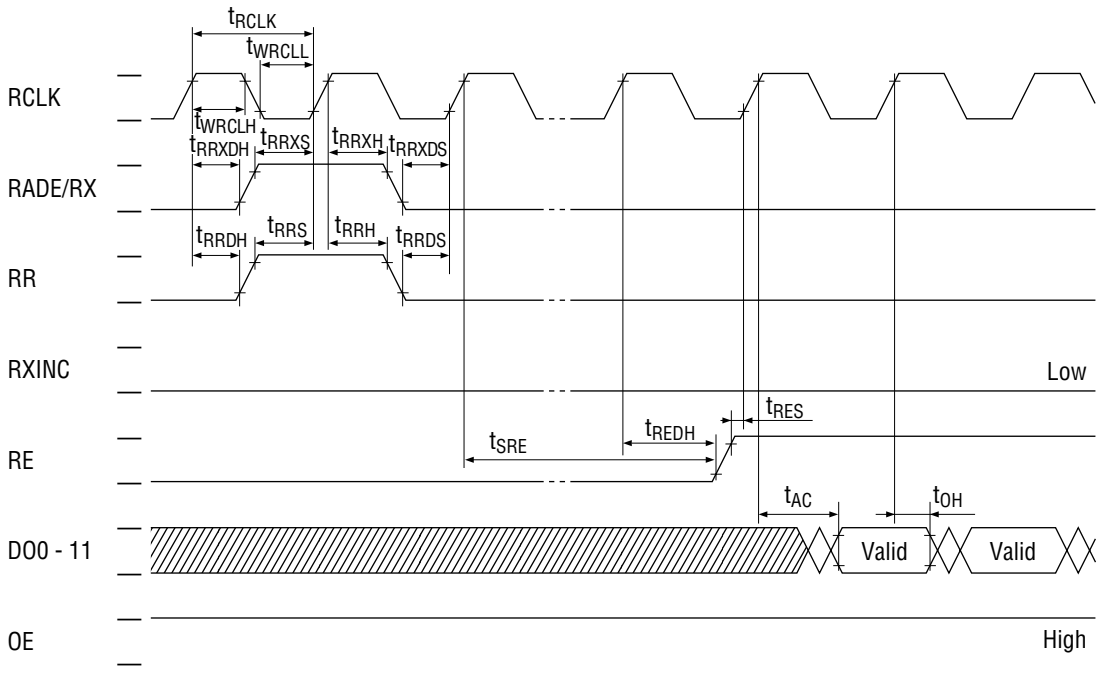
Note : The line address is reset to the initialized addresses and the word address is reset to 0.

Read Line Hold Mode



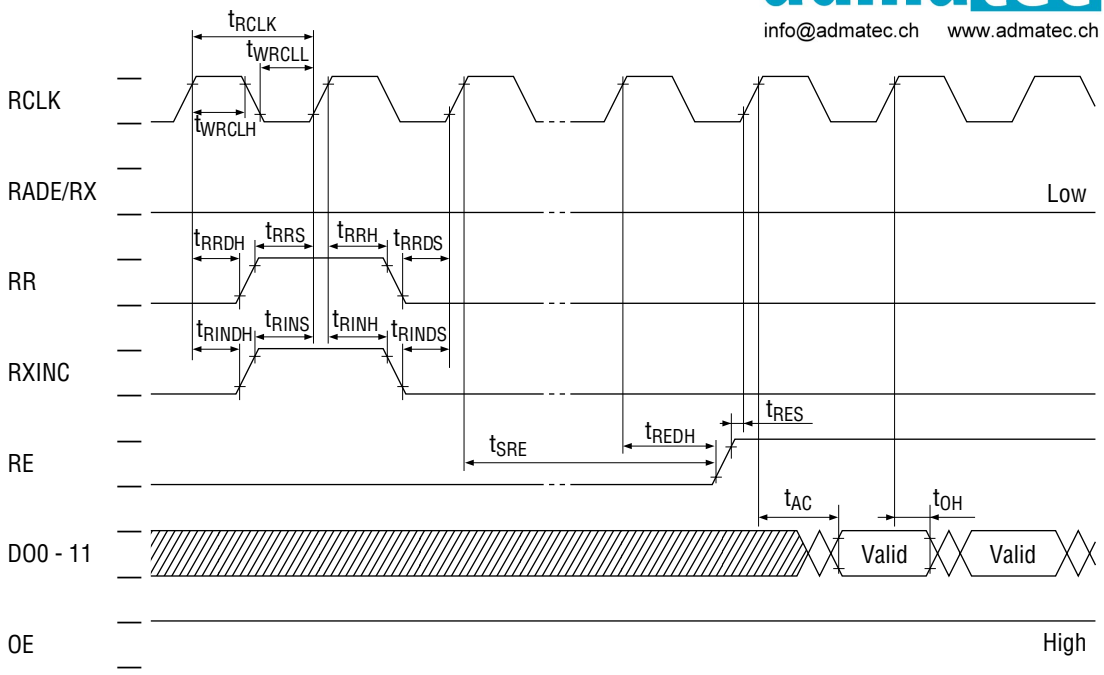
Note : The line address is held and the word address is reset to 0.

Read Reset Mode



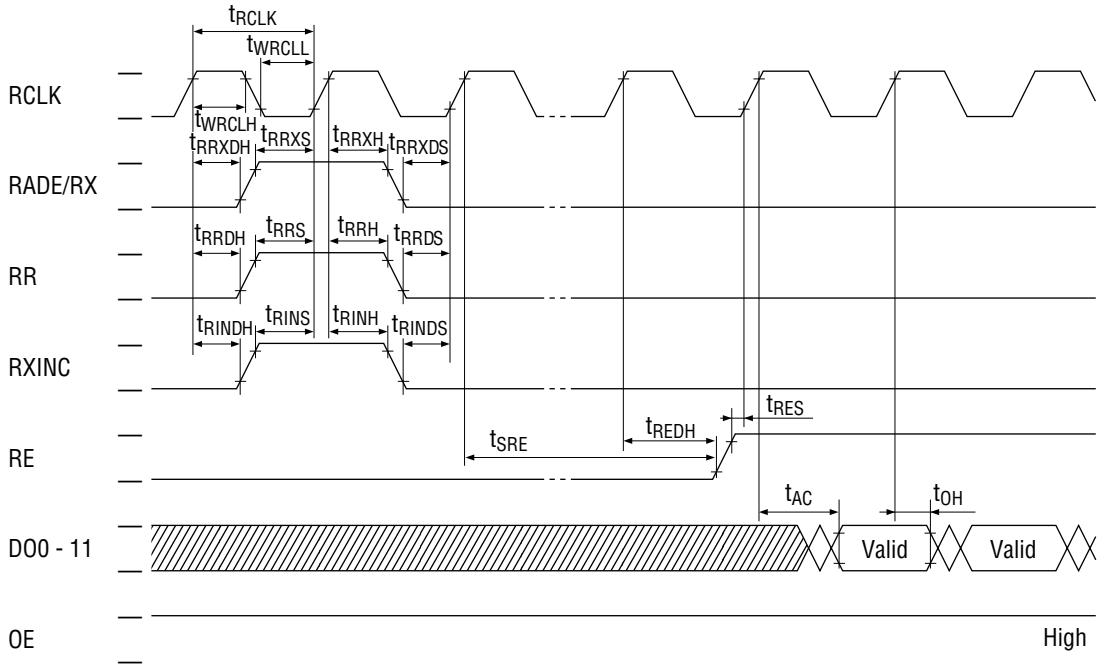
Note : Both the line address and word address are reset to 0.

Read Line Increment Mode



Note : The line address is incremented by 1 and the word address is reset to 0.

Read Address Jump Mode

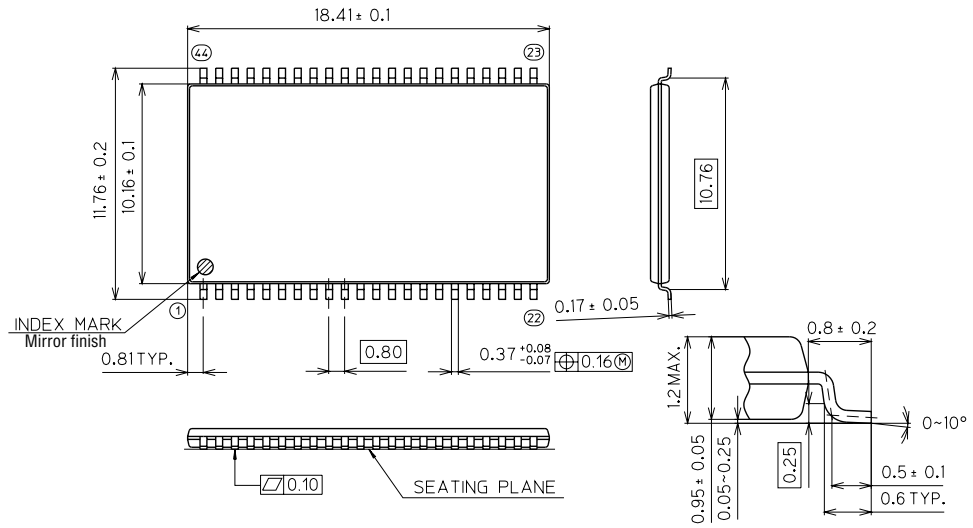


Note : The line address is reset to the initialized addresses and the word address is reset to 0.

PACKAGE DIMENSIONS

(Unit : mm)

TSOPII44-P-400-0.80-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.54 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).