**OKI** Semiconductor

# MSM514212

**5,048-Word × 8-Bit Line Memory**

## DESCRIPTION

The OKI MSM514212 is a high-performance serial-line memory. It is designed for use in NTSC, PAL or SECAM Video line buffer applications such as digital comb filters in TVs/VTRs, IDTV (Improved Definition Television), time based correction, or other applications that use serial data including facsimiles, digital copy machines, etc.  High-reliability and low-power consumption are accomplished by using CMOS dynamic memory cells.

It has separate 8-bit-wide serial input and serial output ports that use independent data clocks to support asynchronous read and write operations.  Different clock rates are also supported that allow alternate data rates between input and output data streams.

A wide range of variable delay bits (40 bits to 5,048 bits) are supported offering greater design flexibility.  Internal logic keeps all asynchronous accesses from being delayed by arbitrating the data storage, and data retrieval requirements to provide maximum performance at all times.

All input and output signals are TTL compatible, and the MSM514212 is packaged in a standard 400 mil 28-pin plastic ZIP.

## FEATURES

- Single power supply: 5 V ±10%
- Capacity: 5,048 words × 8 bits
- Access: I/O asynchronous
- Access time: 28 ns (min.)
- Cycle time : 28 ns (min.)
- Delay bits:  Variable (40 to 5,048)
- Low current consumption: 30 mA (max.)
- Operating voltage range: 4.5 V to 5.5 V
- Operating temperature range : 0°C to 70°C
- Package :
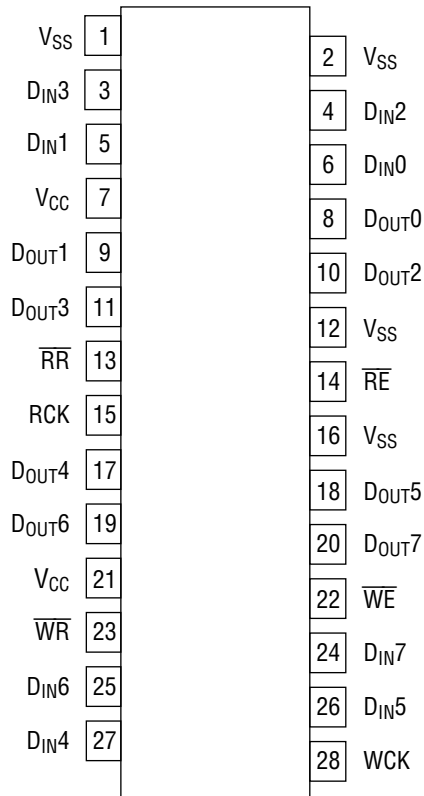  28-pin 400 mil plastic ZIP        (ZIP28-P-400-1.27)        (Product : MSM514212-xxZS)
                                                               xx indicates speed rank.

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## PRODUCT FAMILY

| Family | Cycle Time (Min.) | Access Time (Min.) | Power Dissipation (Max.) |
|---|---|---|---|
| MSM514212-28 | 28 ns | 28 ns | 230 mA |
| MSM514212-34 | 34 ns | 34 ns | 200 mA |
| MSM514212-50 | 50 ns | 40 ns | 170 mA |

## PIN CONFIGURATION (TOP VIEW)

| Pin (left) | # | | # | Pin (right) |
|---|---|---|---|---|
| $V_{SS}$ | 1 | | 2 | $V_{SS}$ |
| $D_{IN}3$ | 3 | | 4 | $D_{IN}2$ |
| $D_{IN}1$ | 5 | | 6 | $D_{IN}0$ |
| $V_{CC}$ | 7 | | 8 | $D_{OUT}0$ |
| $D_{OUT}1$ | 9 | | 10 | $D_{OUT}2$ |
| $D_{OUT}3$ | 11 | | 12 | $V_{SS}$ |
| $\overline{RR}$ | 13 | | 14 | $\overline{RE}$ |
| RCK | 15 | | 16 | $V_{SS}$ |
| $D_{OUT}4$ | 17 | | 18 | $D_{OUT}5$ |
| $D_{OUT}6$ | 19 | | 20 | $D_{OUT}7$ |
| $V_{CC}$ | 21 | | 22 | $\overline{WE}$ |
| $\overline{WR}$ | 23 | | 24 | $D_{IN}7$ |
| $D_{IN}6$ | 25 | | 26 | $D_{IN}5$ |
| $D_{IN}4$ | 27 | | 28 | WCK |

28-Pin Plastic ZIP

| Pin Name | Function |
|---|---|
| WCK | Write Clock |
| $\overline{WR}$ | Write Address Reset |
| $\overline{WE}$ | Write Enable |
| $D_{IN}0$ - 7 | Data Input |
| RCK | Read Clock |
| $\overline{RR}$ | Read Address Reset |
| $\overline{RE}$ | Read Enable |
| $D_{OUT}0$ - 7 | Data Output |
| $V_{CC}$ | Power Supply (5 V) |
| $V_{SS}$ | Ground (0 V) |

Note:     The same power supply voltage must be provided to every $V_{CC}$ pin, and the same GND voltage level must be provided to every $V_{SS}$ pin.

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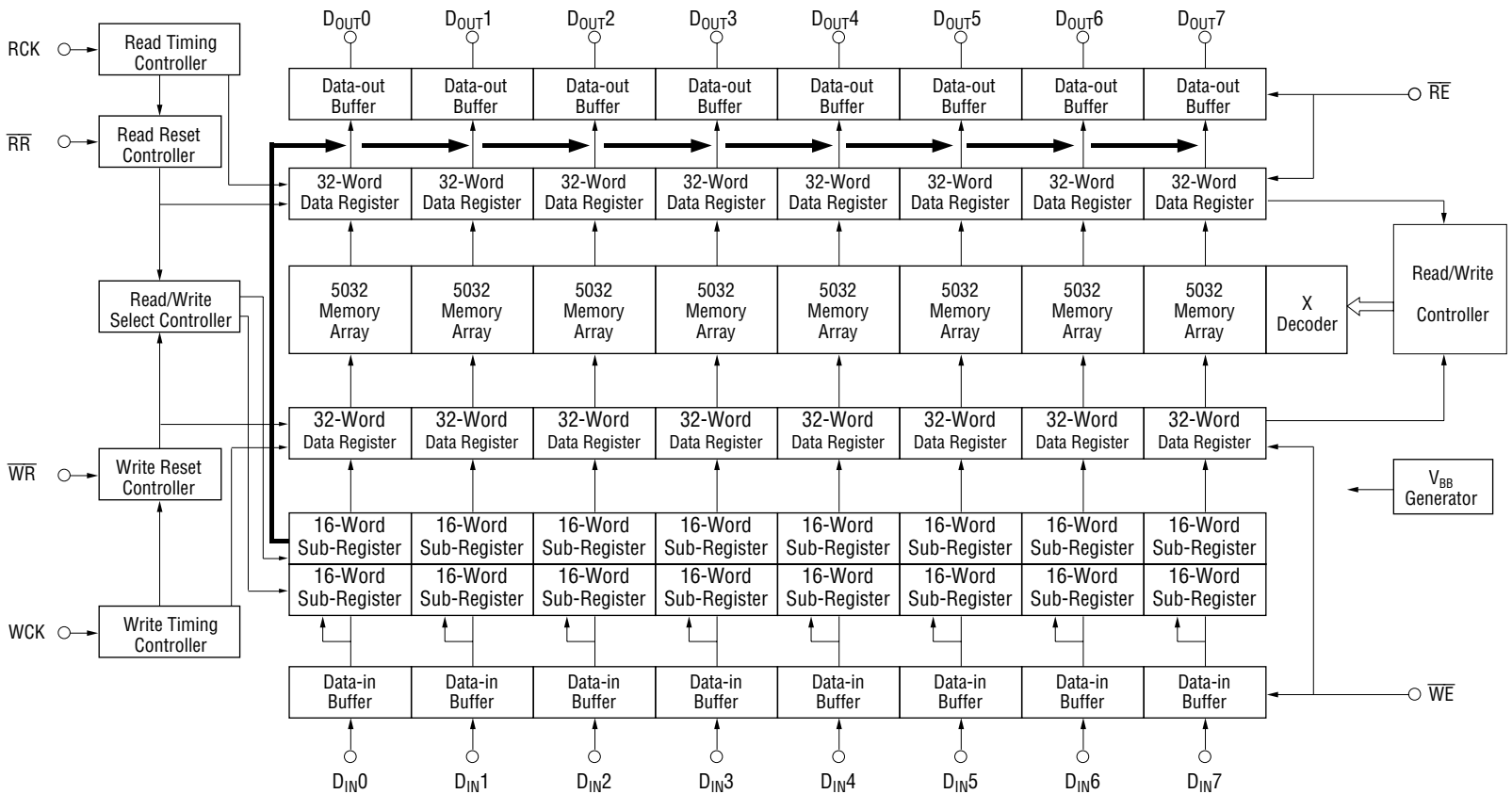
# ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Pin Voltage Relative to Vss | $V_T$ | at Ta = 25°C, Vss | −1.0 to 7.0 | V |
| Power Supply Voltage | $V_{CC}$ | at Ta = 25°C, Vcc | −1.0 to 7.0 | V |
| Circuit Output Current | $I_O$ | Ta = 25°C | 20 | mA |
| Operating Temperature | $T_{opr}$ | — | 0 to 70 | °C |
| Storage Temperature | $T_{stg}$ | — | −55 to 150 | °C |

## Recommended Operating Conditions

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | — | 4.5 | 5.0 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | — | 2.4 | — | 5.5 | V |
| Input Low Voltage | $V_{IL}$ | — | −1.5 | — | 0.8 | V |
| Temperature Around | Ta | — | 0 | — | 70 | °C |

## DC Characteristics (On the Recommended Operating Conditions)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power Supply Current | $I_{CC}$ | — | — | — | 30 | mA |
| Input Leakage Current | $I_I$ | $V_I$ = 0 to Vcc, Other pins are 0 V | −10 | — | 10 | µA |
| Output Leakage Current | $I_O$ | $V_O$ = 0 to 5.5 V, $D_{OUT}$ high impedance | −10 | — | 10 | µA |
| Output High Level Voltage | $V_{OH}$ | $I_{OH}$ = −1 mA | 2.4 | — | — | V |
| Output Low Level Voltage | $V_{OL}$ | $I_{OL}$ = 2 mA | — | — | 0.4 | V |

## Capacitance

$$(V_{CC} = 5 \text{ V} \pm 10\%, Ta = 25°C, f = 1 \text{ MHz})$$

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_I$ | — | — | — | 5 | pF |
| Output Capacitance | $C_O$ | — | — | — | 7 | pF |

## AC Characteristics (On the Recommended Operating Conditions)

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| Parameter | Symbol | -28 | | -34 | | -50 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Write Clock Cycle Time | $t_{WCK}$ | 28 | 1980 | 34 | 1980 | 50 | 1980 | ns |
| Write Clock Pulse Width | $t_{WCW}$ | 11 | — | 14 | — | 20 | — | ns |
| Write Clock Precharge Time | $t_{WCP}$ | 11 | — | 14 | — | 20 | — | ns |
| Read Clock Cycle Time | $t_{RCK}$ | 28 | 1980 | 34 | 1980 | 50 | 1980 | ns |
| Read Clock Pulse Width | $t_{RCW}$ | 11 | — | 14 | — | 20 | — | ns |
| Read Clock Precharge Time | $t_{RCP}$ | 11 | — | 14 | — | 20 | — | ns |
| Access Time | $t_{AC}$ | — | 28 | — | 34 | — | 40 | ns |
| Cycle Access Time Right After Reset | $t_{ACR}$ | — | 28 | — | 34 | — | 40 | ns |
| Output Hold Time | $t_{OH}$ | 5 | — | 5 | — | 5 | — | ns |
| Output Hold Time Right After Reset | $t_{OHR}$ | 5 | — | 5 | — | 5 | — | ns |
| Output Low Impedance Period | $t_{LZ}$ | 5 | 28 | 5 | 34 | 5 | 40 | ns |
| Output High Impedance Period | $t_{HZ}$ | 5 | 28 | 5 | 34 | 5 | 40 | ns |
| Input Data Setup Time | $t_{DS}$ | 11 | — | 14 | — | 15 | — | ns |
| Input Data Hold Time | $t_{DH}$ | 5 | — | 5 | — | 5 | — | ns |
| $\overline{WR}/\overline{RR}$ Setup Time from WCK/RCK | $t_{RS}$ | 11 | — | 14 | — | 15 | — | ns |
| $\overline{WR}/\overline{RR}$ Hold Time from WCK/RCK | $t_{RH}$ | 5 | — | 5 | — | 5 | — | ns |
| $\overline{WR}/\overline{RR}$ Nonselective Time 1 from WCK/RCK | $t_{RN1}$ | 5 | — | 5 | — | 5 | — | ns |
| $\overline{WR}/\overline{RR}$ Nonselective Time 2 from WCK/RCK | $t_{RN2}$ | 11 | — | 14 | — | 15 | — | ns |
| $\overline{WE}$ Setup Time from WCK | $t_{WES}$ | 11 | — | 14 | — | 15 | — | ns |
| $\overline{WE}$ Hold Time from WCK | $t_{WEH}$ | 5 | — | 5 | — | 5 | — | ns |
| $\overline{WE}$ Nonselective Time 1 from WCK | $t_{WEN1}$ | 5 | — | 5 | — | 5 | — | ns |
| $\overline{WE}$ Nonselective Time 2 from WCK | $t_{WEN2}$ | 11 | — | 14 | — | 15 | — | ns |
| $\overline{RE}$ Setup Time from RCK | $t_{RES}$ | 11 | — | 14 | — | 15 | — | ns |
| $\overline{RE}$ Hold Time from RCK | $t_{REH}$ | 5 | — | 5 | — | 5 | — | ns |
| $\overline{RE}$ Nonselective Time 1 from RCK | $t_{REN1}$ | 5 | — | 5 | — | 5 | — | ns |
| $\overline{RE}$ Nonselective Time 2 from RCK | $t_{REN2}$ | 11 | — | 14 | — | 15 | — | ns |
| $\overline{WE}$ High Level Period | $t_{WEW}$ | 0 | — | 0 | — | 0 | — | ns |
| $\overline{RE}$ High Level Period | $t_{REW}$ | 0 | — | 0 | — | 0 | — | ns |
| $\overline{WR}$ Low Level Period (Write Reset Period) | $t_{RSTW}$ | 0 | — | 0 | — | 0 | — | ns |
| $\overline{WR}$ Low Level Period (Read Reset Period) | $t_{RSTR}$ | 0 | — | 0 | — | 0 | — | ns |
| Transition Time | $t_{T}$ | 3 | 35 | 3 | 35 | 3 | 35 | ns |

Notes:   1.  The input voltage reference levels stipulated in the timing specification are $V_{IH}$ = 3.0 V and $V_{IL}$ = 0 V.  The $t_T$ is the transition time between $V_{IH}$ = 3.0 V and $V_{IL}$ = 0 V.

2.  Rise and fall time $t_T$ of all the cycles is specified as 5 ns.

3.  During asynchronous execution of write and read operation, the difference between the write address and read address must be greater than 40.

4.  Since the MSM514212 uses a dynamic memory cell, it can read the data of the written address within 10 ms after the write cycle at that address is completed.

5.  The load condition for measurement is based on 1 TTL + 30 pF.

6.  All the potential to the power supply/grounding terminals needs to be supplied.

## SIGNAL DESCRIPTIONS

### Data Inputs (D$_{IN}$0 - D$_{IN}$7)

Data on these inputs is shifted in on the rising edge of WCK while $\overline{WE}$ is held at a low level. The data setup and hold times t$_{DS}$ and t$_{DH}$ are referenced to the rising edge of WCK.

### Data Outputs (D$_{OUT}$0 - D$_{OUT}$7)

Data is shifted out on these outputs during the rising edge of RCK while $\overline{RE}$ is held at a low level. The data becomes valid after the access time interval t$_{AC}$ which begins at the rising edge of RCK.

### Write Address Pointer Reset ($\overline{WR}$)

If $\overline{WR}$ is brought to a low level, the next rising edge of WCK resets the write address pointer to the first address location. The write address pointer is automatically reset when the last address location (5048) is clocked. The $\overline{WR}$ setup, and hold times t$_{RS}$ and t$_{RH}$ are referenced to the rising edge of WCK. Each write operation, which begins after $\overline{WR}$, must contain at least 18 active write cycles, i.e. WCK cycles while $\overline{WE}$ is high.

### Read Address Pointer Reset ($\overline{RR}$)

If $\overline{RR}$ is brought to a low level, the next rising edge of RCK resets the read address pointer to the first address location. The read address pointer is automatically reset when the last address location (5048) is clocked. The $\overline{RR}$ setup, and hold times t$_{RS}$ and t$_{RH}$ are referenced to the rising edge of WCK. Each read operation, which begins after $\overline{RR}$, must contain at least 18 active read cycles, i.e. RCK cycles while $\overline{RE}$ is high.

### Write Enable ($\overline{WE}$)

This pin is used as a gating function for the WCK input. If $\overline{WE}$ is held low, normal write cycles can occur. If $\overline{WE}$ is brought to a high level before the next rising edge of WCK, all subsequent write cycles will be inhibited, and the write address pointer remains unchanged. The $\overline{WE}$ setup and hold times t$_{WES}$ and t$_{WEH}$ are referenced to the rising edge of WCK.

### Read Enable ($\overline{RE}$)

This pin is used as a gating function for the RCK input. If RE is brought to a high level before the next rising edge of RCK, all subsequent read cycles are inhibited, and the read address pointer remains unchanged. The data outputs will tri-state after the output buffer turn off delay time t$_{HZ}$, which begins at the rising edge of RCK. After the disabled cycles are completed, and the RE signal is brought back to a low level, the data output buffers are re-enabled by the next rising edge of RCK. The RE setup, and hold times t$_{RES}$ and t$_{REH}$ are referenced to the rising edge of $\overline{RCK}$.

### Write Clock (WCK)

The rising edge of the WCK input latches the data into the internal registers, and also increments the write address pointer when WE is held low.

### Read Clock (RCK)

The rising edge of the RCK input shifts out the data from the internal registers and increments the read address pointer when $\overline{RE}$ is held low.

## OPERATION MODE

### Write Cycle

When $\overline{\text{WE}}$ input is enabled (at the "L" level), the write cycle is executed by synchronizing it with the WCK clock input. Read and write data is processed by the same clock in the write cycle to carry out the video processing. Data is input after a delay of oneline (5048 bits) is input at the rising edge of the clock in the write cycle.

In addition, when the length of the delay is controlled by $\overline{\text{WE}}$, the value of the delay bits is from 40 to 5048. The $\overline{\text{WR}}$ operation must be performed now to write the last data to memory cell.

### Read Cycle

When $\overline{\text{RE}}$ input is enabled (at the "L" level), the read cycle is executed by synchronizing it with the RCK clock input. Data is output at $t_{AC}$ (or $t_{ACR}$). In addition, when the length of the delay is controlled by $\overline{\text{RE}}$, the value of the delay bits is from 40 to 5048.

### Write Reset Cycle
### Read Reset Cycle

When the power supply is on, the address values of the read and write address pointers are at random. Thus, each pointer must be initialized by the $\overline{\text{RR}}$ signal and the $\overline{\text{WR}}$ signal beforehand. Data can be input (to address 0) with the first cycle after this reset operation.

### Power-up and Initialization

On power-up, the device is designed to begin proper operation after at least 100 µs after $V_{CC}$ has stabilized to a value within the range of recommended operating conditions. After this 100 µs stabilization interval, the following initialization sequence must be performed.
Because the read and write address counters are not valid after power-up, a minimum of 18 dummy write operations (WCK cycles) and read operations (RCK cycles) must be performed, followed by a $\overline{\text{WR}}$ operation and an $\overline{\text{RR}}$ operation, to properly initialize the write and the read address pointer. Dummy write cycles/$\overline{\text{WR}}$ and dummy read cycles/$\overline{\text{RR}}$ may occur simultaneously. If these dummy read and write operations start while $V_{CC}$ and/or the substrate voltage has not stabilized, it is necessary to perform an $\overline{\text{RR}}$ operation plus a minimum of 18 RCK cycles plus another $\overline{\text{RR}}$ operation, and a $\overline{\text{WR}}$ operation plus a minimum of 18 WCK cycles plus another $\overline{\text{WR}}$ operation to properly initialize read and write address pointers.
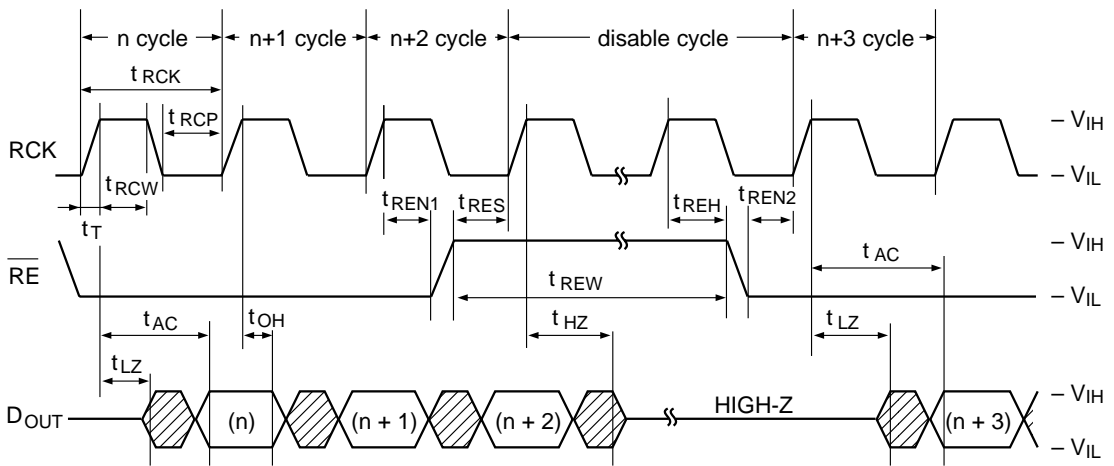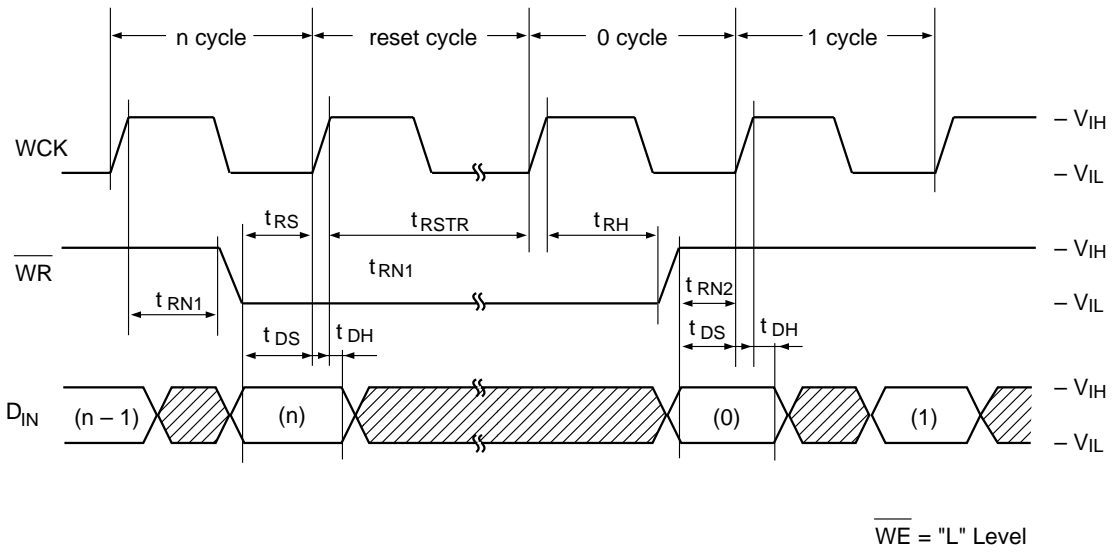
## TIMING WAVEFORM

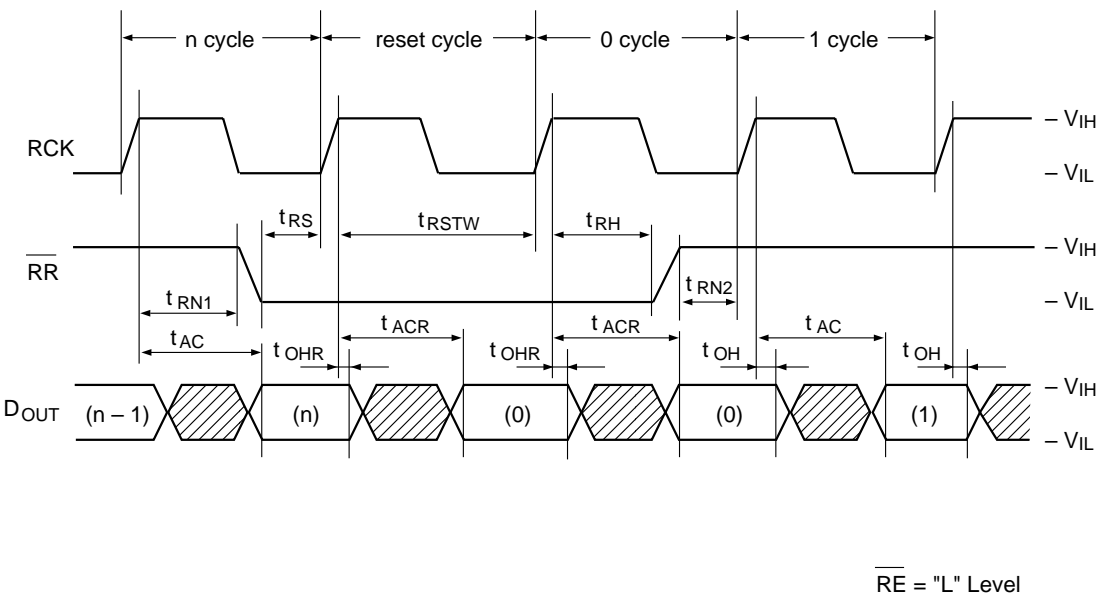### Write Cycle
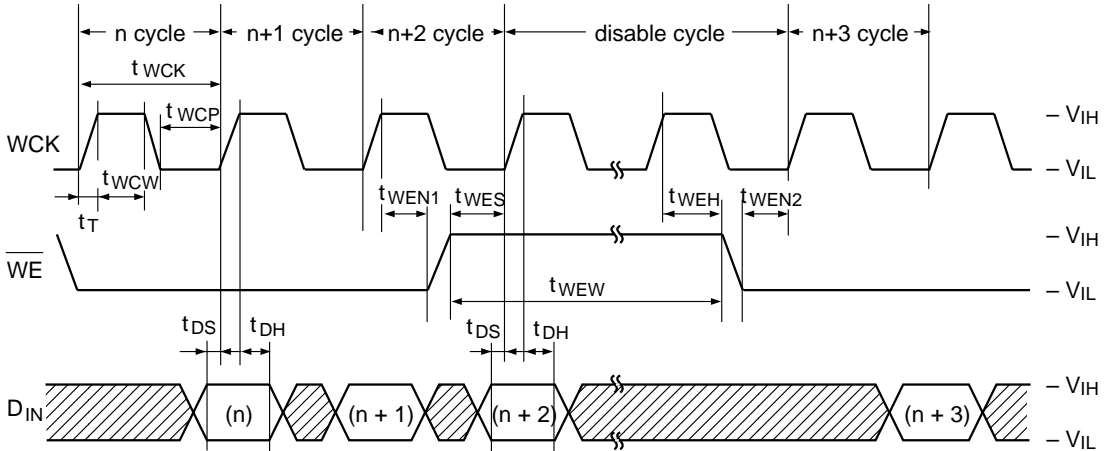


$\overline{WR}$ = "H" Level

### Read Cycle



$\overline{RR}$ = "H" Level

## Write Reset Cycle


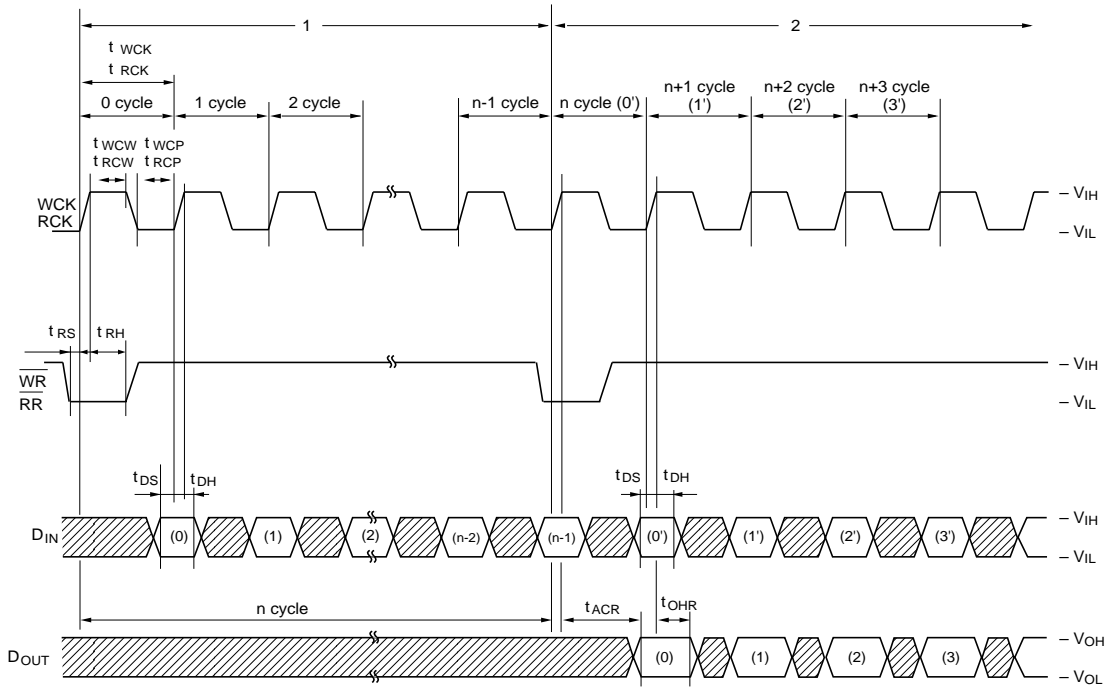
$\overline{WE}$ = "L" Level
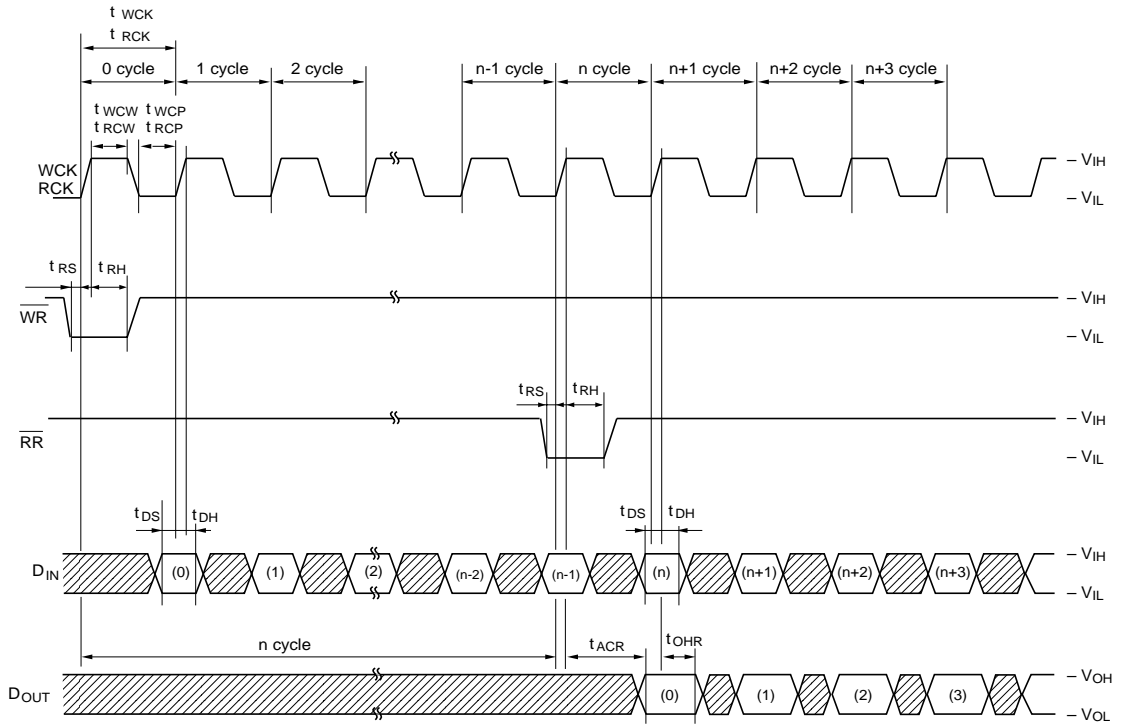
## Read Reset Cycle



$\overline{RE}$ = "L" Level

**Note:** In the write reset and read reset cycles, the reset cycle (for the duration of $t_{RSTW}$, $t_{RSTR}$) is not necessarily required for the reset operation.
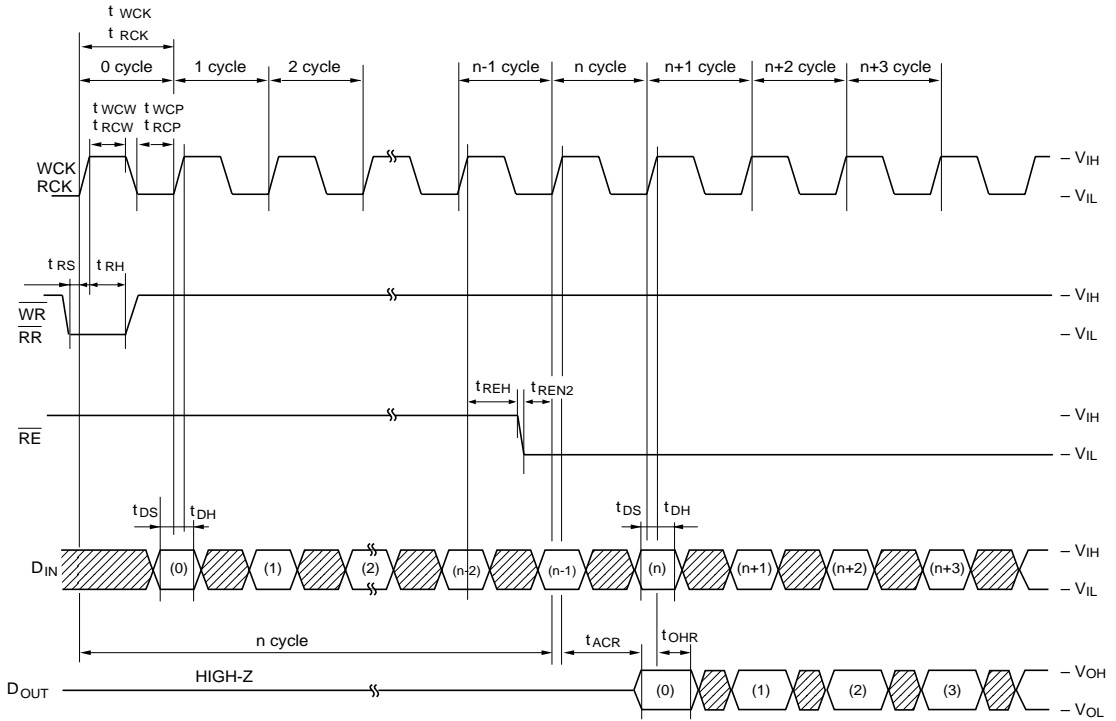
## n Bit Delay Line Timing (1)



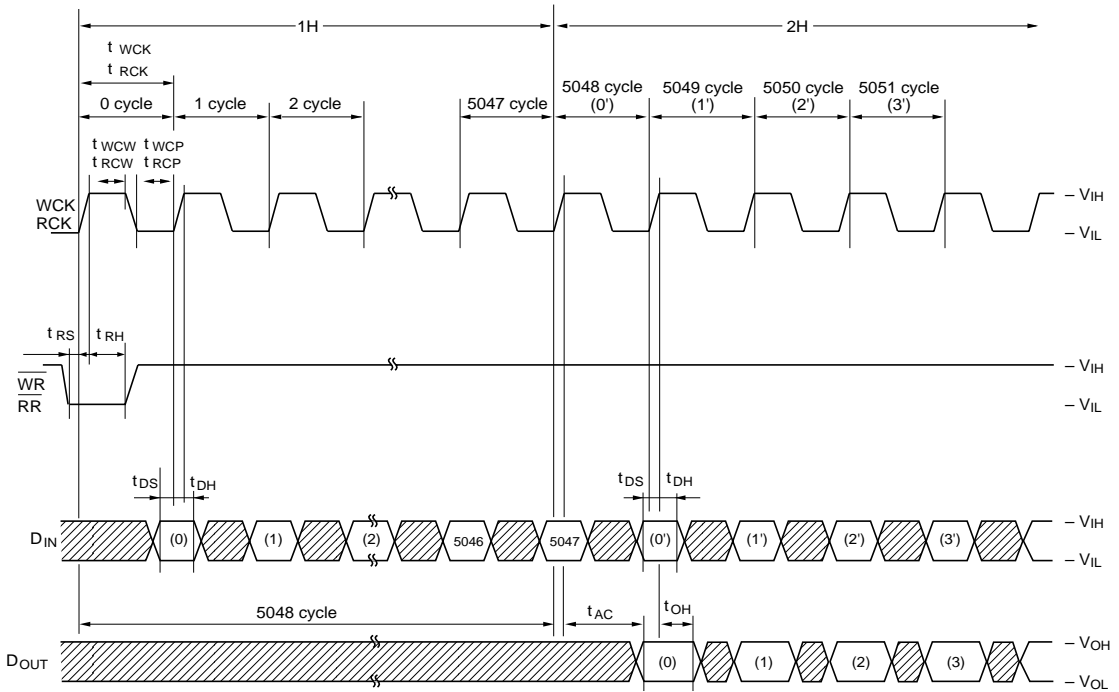$\overline{RE}, \overline{WE}$ = "L" Level

## n Bit Delay Line Timing (2)

$\overline{RE}$, $\overline{WE}$ = "L" Level

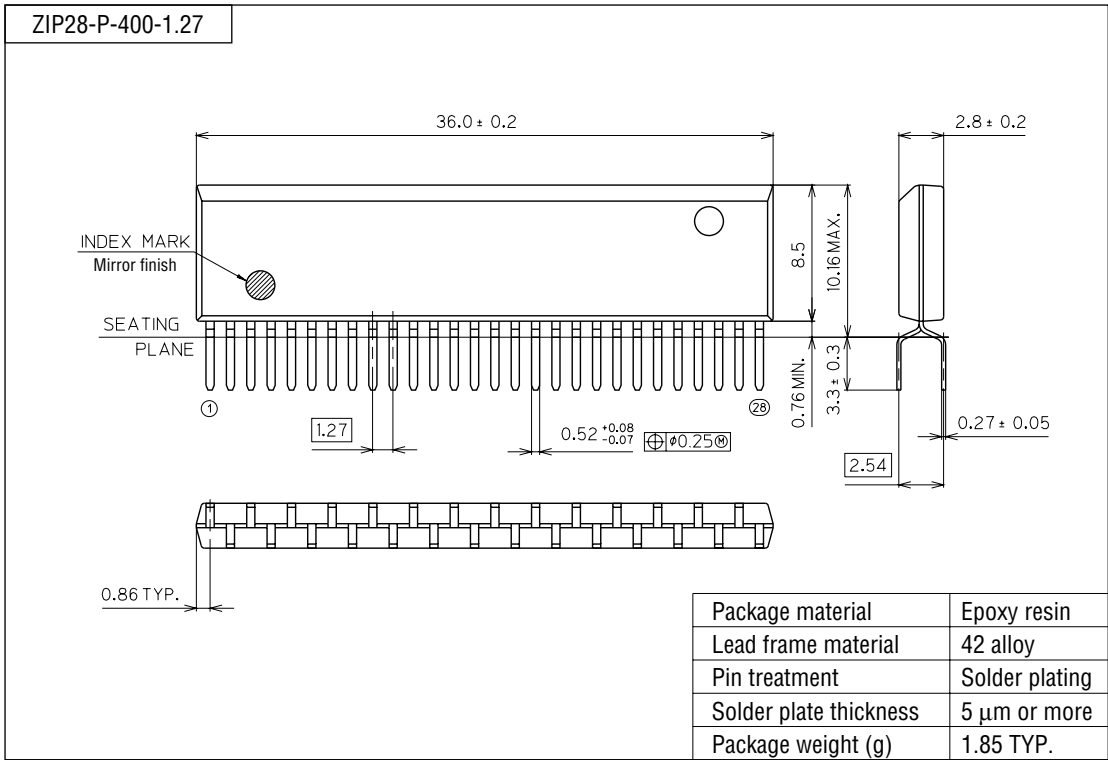## n Bit Delay Line Timing (3)

$\overline{WE}$ = "L" Level

## 1 H Delay Line Timing

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$\overline{RE}$, $\overline{WE}$ = "L" Level

## PACKAGE DIMENSIONS

(Unit : mm)

ZIP28-P-400-1.27

INDEX MARK
Mirror finish

SEATING
PLANE

36.0 ± 0.2

2.8 ± 0.2

8.5

10.16 MAX.

0.76 MIN.

3.3 ± 0.3

0.27 ± 0.05

1.27

0.52 $^{+0.08}_{-0.07}$　⊕ φ0.25Ⓜ

2.54

①

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0.86 TYP.

| Package material | Epoxy resin |
|---|---|
| Lead frame material | 42 alloy |
| Pin treatment | Solder plating |
| Solder plate thickness | 5 μm or more |
| Package weight (g) | 1.85 TYP. |