

Oki,	Network Solutions
	for a Global Society

PEDL9361-01 Issue Date:Dec. 12, 2002

Preliminary

128-Channel Organic EL Anode Driver

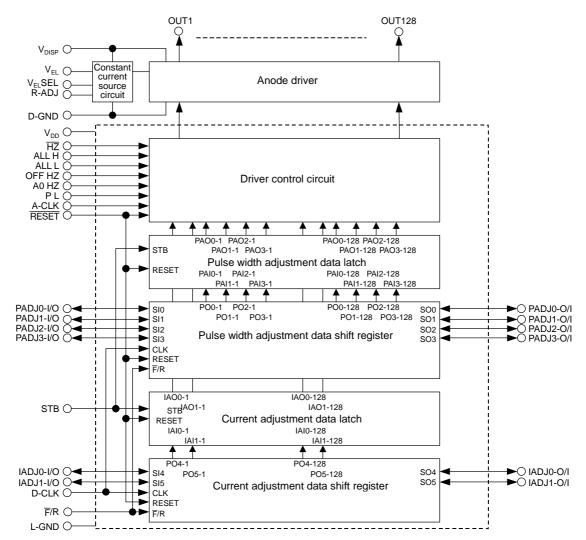
GENERAL DESCRIPTION

The ML9361 is an organic EL anode driver LSI with 128 drivers. The anode driver is constant current output type and allows adjustment of current and pulse width for each output. Since this LSI has the output condition setting function, which allows setting of all outputs High, all outputs Low, and all outputs High Impedance, the user can set driving methods suited to the characteristics of individual organic EL panel. When combined with ML9371 the organic EL cathode driver, the ML9361 can drive a 64 × 128 full-dot panel.

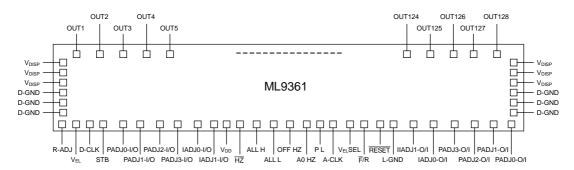
FEATURES

- : 3.0 to 5.5 V Logic power supply voltage EL drive voltage : 8.0 to 30 V (max.) • Anode outputs : 128 outputs • Anode high output current : -1.0 mA (constant current output, current adjustment range = at • 100%) • Anode low output current : 40 mA (max.) Anode low ON-resistance : 500Ω (max.) • Anode output current adjustment range : 0%, 33%, 66%, and 100% (for each output) . : Adjustable in 16 different degrees (adjusted by external clock input, • Output pulse width adjustment for each output) All outputs High, all outputs Low, and all outputs High Impedance can be set as output conditions : Gold bump chip (TCP is tailored for each customer requirement)
- Package

BLOCK DIAGRAM



PIN CONFIGURATION (Gold bump chip)



PIN DESCRIPTION

Mos Power supply DegNo DegNo <thdegno< th=""> <thdegno< th=""> <thdegno< th=""> <</thdegno<></thdegno<></thdegno<>	Symbol	I/O	Connected to	Description
V _{pc} — Power suppy U _c is the logic circuit power suppy pin. D-GND — Power suppy D-GND is a ground pin for logic circuit. D-GND is a ground pin for logic circuit. U-GND is a ground pin for logic circuit. D-GND and L-GND should be connected outside the LSI. Via. I Power suppy D'UT to CUT128 output current adjusting voltage input pin. Via. I Power suppy Pin for selecting the output current adjusting voltage input pin. Via. I Microcontroller When this pin is low, LSI's internal voltage (S V) is selected. R-ADJ I Resistor OUT1 to CUT128 output current adjusting voltage input on the Via. pin is selected. R-ADJ I Resistor OUT1 to CUT128 output current adjusting at POn-128 toward POn-128. (n = 1 to 5) IADJ0-IO Via Microcontroller When this pin is high, data is transferred starting at POn-128 toward POn-128. (n = 1 to 5) IADJ0-IO Via Microcontroller. When the FR pin is log, these pins are input pins and data is read into at the rising edge of D-CLK. PADJ0-IO Via Microcontroller. Anode output current adjusting data input-output pins. PADJ0-OI Via	VDISP			V_{DISP} is a power supply pin for anode driver circuit and constant current source circuit.
D-SND — Power supply U-GND D-SND is a ground pin for logic circuit. L-GND and L-GND should be connected outside the LSI. Vet. 1 Power supply DUTTs output current sating voltage input pin. Vet. 1 Power supply DUTTs output a voltage within the guaranteed operating range. Vet.SEL 1 Microcontroller When this pin is enabled when Vs_SEL is high, and disabled when it is low. R-ADJ 1 Resistor OUTT to OUT28 output current adjusting voltage for anode driver circuit. Pin for selecting the output current adjusting voltage (V) is selected. •When this pin is high, the input voltage to the current adjusting data shift register and the voltage is the voltage is selected. F/R 1 Microcontroller •When this pin is high, these pins are input pins. r/ADJ0-I/O I/O Microcontroller •When the F/R pin is logid tata input-output pins. r/ADJ0-0/O 0/I Microcontroller •Circl.K. When the F/R pin is high, these pins are input pins and data is read into at the rising edge di D-CLK. PADJ0-1/O 0/I Microcontroller Anode output pulse width adjusting data input-output pins. PADJ0-1/O 0/I Microcontroller F			_	
L-GND L-GND is a gloudo pin for logic circuit. U-GND is a gloudo pin for logic circuit. D-GND and L-GND Should be connected outside the LSI. Vet. 1 Power supply Input voltage to this pin is enabled when V_SEL is high, and disabled when it is low. Leave this pin copen or input a voltage within the guaranteed operating range. Vet.SEL 1 Microcontroller •When this pin is low, LSI's internal voltage (5V) is selected. R-ADJ 1 Resistor OUT1 to OUT128 output current adjusting data shift register. •When this pin is low, Lat is transferred starting at POn-1 toward POn-128. (n = 1 to 5) IADJ0-I/O I/O Outfload as the transferred starting at POn-1 toward POn-128. (n = 1 to 5) IADJ0-I/O I/O Wincrocontroller, or ML381 on the F/R pin is low, these pins are input pins and that is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins. PADJ0-I/O O/I Microcontroller, or ML381 on next stage Anode output use with adjusting data input-output pins. PADJ2-I/O O/I Anode output use with adjusting data input-output pins. PADJ2-O/I O/I Anode output use with adjusting data input-output pins. PADJ2-O/I O/I Anode output us		_	Power supply	
Vel. I Develop and compare volume of controlling voltage input pin. Vel. I Power supply Power supply Vel.SEL I Microcontroller Yes between this pin is enabled when Velse (Lishigh, and disabled when it is low. Leave this pin open or input a voltage within the guaranteed operating range. Phi for selecting the output current adjusting voltage (5 V) is selected. R-ADJ I Resistor OUT1 to OUT128 output current adjusting voltage (5 V) is selected. F/R I Microcontroller When this pin is high, the input voltage at the Vel protocomposition pin. IADJ0-VO IOT OUT18 output current adjusting data infit register and pulse width adjusting data is hift register. IADJ0-VO I/O Nicrocontroller When this pin is ligh, these pins are output pins. Microcontroller node output current adjusting data input-output pins. When the F/R pin is high, these pins are output pins and the output status changes at the falling edge of D-CLK. PADJ0-VO I/O Nicrocontroller Anode output urrent adjusting data input-output pins. PADJ0-VO I/O Nicrocontroller Anode output use width adjusting data input-output pins. PADJ0-VO I/O Nicrocontroller <td>-</td> <td></td> <td></td> <td>5 1 5</td>	-			5 1 5
V _{Et} I Power supply Leave this pin open or input a voltage within the guaranteed operating range. Leave this pin open or input a voltage within the guaranteed operating range. V _{E3} SEL I Microcontroller •When this pin is pin, LSS internal voltage (5 V) is selected. R-ADJ I Resistor OUT1 to UT128 output current adjusting voltage (5 V) is selected. F/R I Microcontroller •When this pin is low, these pins are input pin for current adjusting data shift register and Data transfer direction select signal input pin for current adjusting data shift register and within the sustain select starting at POn-128 toward POn-128. (n = 1 to 5) IADJ0-V0 IADJ1-V0 I/O Microcontroller •When this pin is low, data is transferred starting at POn-128 toward POn-128. (n = 1 to 5) IADJ0-V0 IADJ1-V0 I/O Microcontroller, or ML3361 on or ML3361 on	L-OND			
Leave this pin open or input a voltage within the guaranteed operating range. Pin for selecting the output current adjusting voltage for anode driver circuit. Wicrocontroller • When this pin is high, the input voltage at the X-gua pin is selected. R-ADJ I Resistor OUT1 to OUT128 output current setting resistor connection pin. Bin Data transfer direction select sign and provide the X-guaranteed operating at POn-1 to ward POn-128. In = 1 to 5) IADJO-I/O V/O Microcontroller • When this pin is low, data is transferred starting at POn-1 toward POn-128. In = 1 to 5) IADJO-I/O V/O Microcontroller • When the F/R pin is high, data is transferred starting at POn-128 toward POn-1. (In = 1 to 5) IADJO-I/O V/O Microcontroller • When the F/R pin is high, data is transferred starting at POn-128 toward POn-1. (In = 1 to 5) IADJO-0/I V/O Microcontroller • When the F/R pin is high, these pins are output pins and data is read into at the rising edge of D-CLK. When the F/R pin is high, these pins are output pins. PADJ-1/O V/O Microcontroller • Anode output pulse width adjusting data input-output pins. PADJ-1/O V/O Microcontroller • Anode output pulse width adjusting data and anode output pins and the output status othaga set the failing edge of D-CLK. <				
V _{R.} SEL I Microcontroller When this pin is low, LSF is internal voltage (5 V) is selected. R-ADJ I Resistor OUT I to OUT128 output current setting resistor connection pin. Detains Data transfer direction select signal input pin for current adjusting data shift register and pulse width adjusting data sith register. IADJ0-I/O I/O Data transfer direction select signal input pin for current adjusting data sith register and pulse width adjusting data input-output pins. IADJ0-I/O I/O Anode output current adjusting data input-output pins. IADJ0-I/O I/O Microcontroller When the F/R pin is low, these pins are input pins and data is read into at the rising edge of D-CLK. IADJ0-0/I On I/O Microcontroller Ch-CK when the F/R pin is low, these pins are input pins and data is read into at the rising edge of D-CLK. PADJ0-1/O On Microcontroller Anode output pulse width adjusting data input-output pins. PADJ0-0/I PADJ2-0/I I/O Anode output pulse width adjusting data input-output pins. PADJ2-0/I O/I Microcontroller Anode output pulse width adjusting data input-output pins. <	V _{EL}	I	Power supply	Input voltage to this pin is enabled when V_{EL} SEL is high, and disabled when it is low.
V _{RL} SEL I Microcontroller •When this pin is low, LSTs internal voltage (5 V) is selected. R-ADJ I Resistor OUT1 to OUT128 output current sating resistor connection pin. F/R I Microcontroller Data transfer direction select signal input pin for current adjusting data shift register. IADJ0-I/O I/O Microcontroller Data transfer direction select signal input pin for current adjusting data shift register. IADJ0-I/O I/O Anode output current adjusting data input-output pins. Anode output current adjusting data input-output pins. IADJ0-I/O I/O Anode output current adjusting data input-output pins. Anode output current adjusting data input-output pins. IADJ0-I/O O/I Nicrocontroller Anode output current adjusting data input-output pins. PADJ0-I/O O/I Nicrocontroller Anode output current adjusting data input-output pins. PADJ0-I/O Nicrocontroller Anode output pulse width adjusting tai anput-output pins. PADJ0-I/O Nicrocontroller Anode output pulse width adjusting data input-output pins. PADJ0-I/O Nicrocontroller CLK. When the F/R pin is low, these pins are output pins and the output status chanast seed into at the rising edge of D-CLK. <				
			Missessatusllau	5 1 , 5 5
R-ADJ I Resistor OUT1 to OUT128 output current setting resistor connection pin. Data transfer direction select signal inputs with adjusting data shift register. •When this pin is low, data is transferred starting at POn-1 toward POn-128. (n = 1 to 5) IADJ0-I/O IADJ1-I/O V/O •When this pin is low, data is transferred starting at POn-128 toward POn-128. (n = 1 to 5) IADJ0-I/O IADJ1-I/O V/O Microcontroller •When this pin is low, thats is transferred starting at POn-128 toward POn-128. (n = 1 to 5) IADJ0-I/O IADJ1-O1 V/O Microcontroller, or Microsontroller, device and be output set state the falling edge of D-CLK. PADJ-01/O V/O Microcontroller, device and be output current adjusting data input-output pins. PADJ-01/O Microsontroller, or Microsontroller, or Microsontroller, or Microsontroller, or Microsontroller, device and be output set state and be output state state and be output strestand be adjusting data input-output pins. <td>VELSEL</td> <td>I</td> <td>Wicrocontroller</td> <td>3 ()</td>	VELSEL	I	Wicrocontroller	3 ()
F/R I Data transfer direction select signal input pin for current adjusting data shift register. IADJ0-I/C I/C When this pin is low, data is transferred starting at POn-1 toward POn-16. (n = 1 to 5) IADJ0-I/C I/C Microcontroller, or ML9361 on the F/R pin is low, these pins are input pins. When the F/R pin is low, these pins are output pins. IADJ0-0/I I/C Microcontroller, or CLK. When the F/R pin is high, these pins are output pins. When the F/R pin is high, these pins are output pins. IADJ0-0/I O/I Microcontroller, or CLK. When the F/R pin is low, these pins are output pins. When the F/R pin is low, these pins are output pins. PADJ0-1/O PADJ0-1/O I/C Anode output current adjusting data input-output pins. When the F/R pin is low, these pins are output pins and the output status changes at the falling edge of D-CLK. PADJ0-1/O I/O Microcontroller, or ML9361 on next stage Anode output pulse width adjusting data input-output pins. PADJ3-0/I O/I Microcontroller, or ML9361 on next stage Anode output urrent adjusting data and anode output pins and the output status changes at the falling edge of D-CLK. PADJ3-0/I O/I Microcontroller, or ML9361 on next stage Anode output urrent adjusting data and anode output urrent adjusting data and anode output urrent adjusting data and anode out				
F/R I Microcontroller pulse width adjusting data shift register. IADJ0-I/O I/O Microcontroller When this pin is kow, data is transferred starting at POn-1 toward POn-128. (n = 1 to 5) IADJ0-I/O I/O Microcontroller Numen this pin is low, these pins are input pins and data is read into at the rising edge of D-CLK. IADJ0-O/I O/I mext stage When the F/R pin is low, these pins are output pins. VADJ0-I/O next stage When the F/R pin is low, these pins are output pins. PADJ1-I/O O/I Microcontroller, the H/R pin is low, these pins are output pins and data is read into at the rising edge of D-CLK. PADJ0-I/O PADJ2-I/O Microcontroller, the F/R pin is low, these pins are output pins and the output status changes at the falling edge of D-CLK. PADJ2-OI O/I Microcontroller, the F/R pin is low, these pins are input pins and the output status changes at the falling edge of D-CLK. PADJ2-OI O/I Node output pulse width adjusting data input-output pins. PADJ2-OI O/I Anode output current adjusting data and anode output pins. PADJ2-OI O/I Anode output current adjusting data and anode output pins. PADJ3-OI Microcontroller Anode output current adjusting data	R-ADJ		Resistor	
F/R 1 Microcontroller • When this pin is low, data is transferred starting at POn-128 toward POn-12. (n = 1 to 5) IADJ0-I/O I/O Microcontroller, then this pin is loigh, data is transferred starting at POn-128 toward POn-1. (n = 1 to 5) IADJ0-I/O I/O Microcontroller, then this pin is loigh, data is transferred starting at POn-128 toward POn-1. (n = 1 to 5) IADJ0-O/I O/I Microcontroller, the F/R pin is low, these pins are input pins and data is read into at the rising edge of D-CLK. When the F/R pin is high, these pins are output pins and the output status changes at the falling edge of D-CLK. PADJ0-I/O O/I Microcontroller, or ML9361 on next stage Microcontroller, the F/R pin is high, these pins are output pins. PADJ0-I/O PADJ3-OI O/I Nicrocontroller, or ML9361 on next stage Anode output pulse width adjusting data input-output pins. PADJ3-OI O/I Nicrocontroller, or ML9361 on next stage Anode output pulse width adjusting data input-output pins. PADJ3-OI O/I Nicrocontroller, or doe output pulse width adjusting data and anode output pins and the output status changes at the falling edge of D-CLK. PADJ3-OI O/I Nicrocontroller Anode output current adjusting data and anode output pins and data is read into at the rising edge of D-CLK. PADJ3-OI I <td< td=""><td>_</td><td></td><td></td><td></td></td<>	_			
IADJ0-I/O IADJ1-I/O I/O IADJ1-I/O •When this pin is high, data is transferred starting at POn-128 toward POn-1. (n = 1 to 5) IADJ0-I/O IADJ1-I/O I/O Microcontroller, or ML3361 on next stage Anode output current adjusting data input-output pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and the output status changes at the falling edge of D-CLK. PADJ3-0/I O/I Microcontroller Anode output current adjusting data input-output pins. PADJ3-0/I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data transfer clock input pin (Schmitt input) STB I Microcontroller Anode output current adjusting data and anode output pulse width adjus	F/R	I	Microcontroller	
IADJ0-I/O I/O IADJ1-I/O I/O IADJ1-I/O I/O IADJ1-I/O I/O IADJ0-O/I O/I IADJ0-O/I O/I IADJ0-O/I O/I IADJ0-O/I O/I IADJ1-O/I O/I PADJ0-O/I O/I PADJ0-O/I O/I PADJ0-O/I PADJ1-I/O PADJ0-I/O PADJ1-I/O PADJ0-I/O PADJ3-I/O PADJ0-O/I Microcontroller, or MLS361 on next stage PADJ0-O/I Microcontroller, or MLS361 on next stage PADJ3-O/O Microcontroller, or MLS361 on next stage Anode output pulse width adjusting data input-output pins. PADJ3-O/I Microcontroller, or MLS361 on next stage Anode output pulse width adjusting data input-output pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and data is read into at the rising edge of D-CLK. PADJ3-O/I Microcontroller Anode output current adjusting data input-output pins and data is read into at the rising edge of D-CLK. PLCLK I				
IADJ0-I/O I/O Microcontroller, or ML381 on next stage When the F/R pin is low, these pins are input pins and data is read into at the rising edge of D-CLK. PADJ1-0/1 O/1 O/1 D+CLK. When the F/R pin is high, these pins are output pins and the output status of D+CLK. When the F/R pin is high, these pins are output pins and the output status of D+CLK. When the F/R pin is high, these pins are output pins and the output status of D+CLK. When the F/R pin is high, these pins are output pins and the output status of D+CLK. When the F/R pin is high, these pins are output pins and the output status of D+CLK. When the F/R pin is high, these pins are output pins and the output status of D+CLK. When the F/R pin is high, these pins are output pins and the output status of D+CLK. When the F/R pin is high, these pins are output pins and the output status of D+CLK. When the F/R pin is high, these pins are output pins and the output status of D+CLK. When the F/R pin is high, these pins are output pins. PADJ1-0/1 O/1 Microcontroller, or ML3981 on next stage Anode output pulse width adjusting data input-output pins. PADJ2-01 Microcontroller Anode output current adjusting data and anode output pins and the output status of D+CLK. When the F/R pin is low, these pins are output pins and the output status of D+CLK. PADJ3-01 Microcontroller Anode output current adjusting data and anode output pulse width adjusting data transfer clock input pin (Schmitt input). PALK Microcontroller Anode output sail alten outputs: "high inpedance". Microcontroller Microcontroller				
IADJ1-I/O Wicrocontroller, or ML3961 on Next stage of D-CLK. When the F/R pin is high, these pins are output pins. IADJ0-0/I O/I on de output current adjusting data input-output pins. PADJ0-I/O PADJ0-I/O PADJ0-I/O I/O PADJ0-I/O I/O PADJ0-I/O I/O PADJ3-I/O I/O PADJ3-I/O I/O PADJ0-O/I or ML3961 on next stage PADJ0-O/I or ML3961 on next stage PADJ3-O/I next stage PADJ3-O/I node output current adjusting data input-output pins and the output status changes at the falling edge of D-CLK. PADJ3-O/I Microcontroller Anode output current adjusting data and anode output pins and the output status changes at the falling edge of D-CLK. D-CLK I Microcontroller Anode output current adjusting data and anode output pins and the output status changes athe falling edge of D-CLK.	IADJ0-I/O	1/0		
IADJ0-0/I IADJ1-0/I Orl UL381 on ext stage Chardee sat the failing edge of D-CLK. When the F/R pin is high, these pins are input pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and the output status changes at the falling edge of D-CLK. PADJ0-I/O PADJ2-I/O PADJ2-I/O PADJ2-I/O PADJ3-I/O PADJ3-I/O PADJ3-O/I I/O Microcontroller, or ML9361 on next stage Anode output pulse width adjusting data input-output pins. PADJ1-0/I PADJ3-0/I Microcontroller, or ML9361 on next stage Anode output pulse width adjusting data input-output pins. PADJ3-0/I PADJ3-0/I Microcontroller, or ML9361 on next stage Anode output pulse width adjusting data input-output pins. PADJ3-0/I PADJ3-0/I Microcontroller, of D-CLK. When the F/R pin is log, these pins are input pins and data is read into at the rising edge of D-CLK. When the F/R pin is log, these pins are output pins and the output status changes at the falling edge of D-CLK. PADJ3-0/I PADJ3-0/I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data transfer clock input pin (Schmit input) STB I Microcontroller Anode drive signal input pin. RESET I Microcontroller Anode drive signal outputs control signal. NHE I Microcontroller Input pin for anode drive signal output control signal. HZ <	IADJ1-I/O	1/0	Microcontrollor	of D-CLK. When the F/R pin is high, these pins are output pins and the output status
IADJ0-0/I IADJ1-0/I or/l Anode output current adjusting data input-output pins. When the F/R pin is high, these pins are nutput pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and the output status changes at the falling edge of D-CLK. PADJ0-I/O PADJ1-IO PADJ2-IO PADJ2-IO PADJ2-IO PADJ2-IO PADJ2-O/I I/O Anode output pulse width adjusting data input-output pins. When the F/R pin is high, these pins are output pins and the output status changes at the falling edge of D-CLK. PADJ2-O/I PADJ2-O/I PADJ2-O/I PADJ2-O/I of D-CLK. When the F/R pin is high, these pins are output pins and the output status changes at the falling edge of D-CLK. PADJ3-O/I of D-CLK. When the F/R pin is low, these pins are output pins and the output status changes at the falling edge of D-CLK. D-CLK I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data transfer clock input pin (Schmitt input) STB I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data latch strobe signal outputs: all "low" RESET I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data latch strobe signal outputs: all "low" ALL H I Microcontroller Shift register outputs and latch outputs: all "low" ALL H I Microcontroller Input pin for ano			,	changes at the falling edge of D-CLK.
MD0-0/I Ori When the F/R pin is high, these pins are input pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and the output status changes at the falling edge of D-CLK. PADJ0-I/O Microcontroller, or ML3361 on next stage Anode output pulse width adjusting data input-output pins. PADJ0-O/I Microcontroller, or ML3361 on next stage Anode output pulse width adjusting data input-output pins. PADJ0-O/I PADJ0-O/I Microcontroller, or ML3361 on next stage Anode output pulse width adjusting data input-output pins. PADJ2-O/I O/I Nicrocontroller, or ML3361 on next stage Anode output pulse width adjusting data input-output pins. PADJ3-O/I O/I Nicrocontroller, or ML3361 on next stage Anode output pulse width adjusting data input-output pins. PADJ3-O/I Microcontroller, or MLS and the input pin Som data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and the output status phab. PADJ3-O/I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data transfer clock input pin. STB I Microcontroller Anode output rurrent adjusting data and anode output pulse width adjusting data states: • Shift register outputs and latch outputs: "high impedance." Input pin for anode drive signal outputs: "high impedance." <tr< td=""><td></td><td></td><td></td><td>Anode output current adjusting data input-output pins.</td></tr<>				Anode output current adjusting data input-output pins.
IADJ1-0/I Microcontroller, PADJ0-I/O PADJ1-I/O PADJ1-I/O PADJ1-I/O PADJ1-I/O Microcontroller, PADJ2-I/O or Microcontroller, or PADJ2-I/O O/I PADJ2-I/O or PADJ2-I/O or PADJ2-O/I nitrocontroller <td>IADJ0-0/I</td> <td>0/1</td> <td>next stage</td> <td>When the F/R pin is high, these pins are input pins and data is read into at the rising edge</td>	IADJ0-0/I	0/1	next stage	When the F/R pin is high, these pins are input pins and data is read into at the rising edge
PADJ0-I/O PADJ1-V/O PADJ2-V/O PADJ2-V/O PADJ3-V/O V/O PADJ3-V/O Anode output pulse width adjusting data input-output pins. When the F/R pin is low, these pins are input pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and the output status PADJ3-O/I PADJ3-O/I PADJ2-O/I PADJ2-O/I PADJ3-O/I O/I Anode output pulse width adjusting data input-output pins. When the F/R pin is low, these pins are output pins and the output status PADJ3-O/I D-CLK I Microcontroller O/I Anode output current adjusting data and anode output pins and the output status PADJ3-O/I D-CLK I Microcontroller O-CLK. When the F/R pin is low, these pins are output pins and the output status changes at the falling edge of D-CLK. D-CLK I Microcontroller Microcontroller Anode output current adjusting data and anode output pulse width adjusting data transfer clock input pin. STB I Microcontroller Anode output strument adjusting data and anode output pulse width adjusting data latch strobe signal input pin. RESET I Microcontroller Nonde drive signal outputs: all 'inw' - All anode drive signal outputs control signal. ALL H <td>IADJ1-0/I</td> <td>0/1</td> <td></td> <td>of D-CLK. When the F/R pin is low, these pins are output pins and the output status</td>	IADJ1-0/I	0/1		of D-CLK. When the F/R pin is low, these pins are output pins and the output status
PADJ1-I/O I/O PADJ2-I/O I/O Microcontroller Microcontroller PADJ3-I/O Microcontroller O/I next stage PADJ3-O/I Microcontroller Anode output pulse width adjusting data input-output pins. When the F/R pin is high, these pins are input pins and data is read into at the rising edge of D-CLK. PADJ3-O/I Anode output current adjusting data and anode output pulse width adjusting data transfer clock input pin (Schmitt input) STB I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data latch strobe signal input pin. When the signal input pin. When this pin is set low, the LSI enters the following initial setting states: • Shift register outputs and latch outputs: all "low" • All anode drive signal output control signal. HZ I Microcontroller Input pin for anode drive signal output control signal. HZ I Microcontroller Input pin for anode drive signal output control signal.				changes at the falling edge of D-CLK.
PADJ2-I/O I/O PADJ3-I/O Microcontroller, or ML9361/0 Microcontroller, or ML9361/0 Microcontroller, or ML9361/0 Microcontroller, or ML9361/0 Microcontroller, or ML9361/0 Microcontroller Anode output pulse width adjusting data input-output pins. When the F/R pin is high, these pins are output pins and the output status changes at the falling edge of D-CLK. D-CLK I Microcontroller Anode output pulse width adjusting data and anode output pulse width adjusting data transfer clock input pin (Schmitt input) STB I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data latch strobe signal input pin (Schmitt input) RESET I Microcontroller Anode output eurrent adjusting data and anode output pulse width adjusting data latch strobe signal input pin (Schmitt input) IIII Microcontroller Initialization signal input pin (Schmitt input) Initialization signal input pin (Schmitt input) RESET I Microcontroller Input pin for anode drive signal outputs: and lato outputs are constant current output. HZ I Microcontroller Input pin for anode drive signal output control signal. Microcontroller ALL H I Microcontroller Input pin for anode drive signal output control signal. Mi	PADJ0-I/O			Anode output pulse width adjusting data input-output pins.
PADJ2-I/O Microcontroller, PADJ3-I/O Microcontroller, or ML9361 on next stage Microcontroller, or ML9361 on next stage Microcontroller, PADJ-O/I Microcontroller, PADJ2-O/I Anode output pulse width adjusting data input-output pins. PADJ3-O/I O/I Microcontroller, PADJ3-O/I Microcontroller, PADJ3-O/I Anode output pulse width adjusting data input-output pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pulse width adjusting data transfer clock input pin (Schmitt input) STB I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data latch strobe signal input pin (Schmitt input) RESET I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data latch strobe signal input pin (Schmitt input) MEX I Microcontroller Ned output current adjusting data and anode output pulse width adjusting data latch strobe signal outputs: "high impedance" HZ I Microcontroller Input pin for anode drive signal outputs: "high impedance" HZ I Microcontroller Input pin for anode drive signal output control signal. When this pin is high, all anode drive signal outputs are high impedance. HZ I Microcontroller Input pin for anode drive signal output control signal. When this pin is high, anole drive signal output control signal.	PADJ1-I/O	1/0		When the \overline{F}/R pin is low, these pins are input pins and data is read into at the rising edge
Holdsolve or ML39361 on next stage Anode output pulse width adjusting data input-output pins. PADJ2-0/I O/I Anode output pulse width adjusting data input-output pins. When the F/R pin is high, these pins are input pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and the output status changes at the falling edge of D-CLK. D-CLK I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data transfer clock input pin (Schmitt input) STB I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data latch strobe signal input pin (Schmitt input) RESET I Microcontroller Institut register outputs and latch outputs: all "low" • All anode drive signal outputs: "high impedance" Input pin for anode drive signal output control signal. MLL H I Microcontroller Input pin for anode drive signal output control signal. (Schmitt input). ALL H I Microcontroller Input pin for anode drive signal output control signal. Vhen this pin is high, all anode drive signal outputs are high impedance. Input pin for anode drive signal output control signal. ALL H I Microcontroller Input pin for anode drive signal output control signal. OFF HZ	PADJ2-I/O	1/0		of D-CLK. When the F/R pin is high, these pins are output pins and the output status
PADJ0-O/I PADJ1-O/I PADJ3-O/I O/I Inext stage Anode output pulse width adjusting data input-output pins. When the F/R pin is high, these pins are input pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and the output status changes at the falling edge of D-CLK. D-CLK I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data transfer clock input pin (Schmitt input) STB I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data latch strobe signal input pin (Schmitt input) RESET I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data latch strobe signal input pin (Schmitt input) HZ I Microcontroller Anode drive signal outputs: "high impedance" HZ I Microcontroller Input pin for anode drive signal output control signal. When this pin is low, all anode drive signal outputs are constant current output. ALL H I Microcontroller Input pin for anode drive signal output control signal (Schmitt input). When this pin is high, all anode drive signal output control signal (Schmitt input). When this pin is high, all anode drive signal output control signal. ALL H I Microcontroller Input pin for anode drive signal output control signal.	PADJ3-I/O			changes at the falling edge of D-CLK.
PADJ1-0/I PADJ2-0/I PADJ2-0/I O/I IteXt stage Andoe output plase within adjusting data input-output plass. When the F/R pin is high, these pins are input pins and data is read into at the rising edge of D-CLK. When the F/R pin is low, these pins are output pins and the output status changes at the falling edge of D-CLK. D-CLK I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data transfer clock input pin (Schmitt input) STB I Microcontroller Anode output current adjusting data and anode output pulse width adjusting data latch strobe signal input pin (Schmitt input) RESET I Microcontroller Initialization signal input pin (Schmitt input) MET I Microcontroller Initialization signal outputs: migh impedance" HZ I Microcontroller Input pin for anode drive signal outputs: migh impedance. HZ I Microcontroller Input pin for anode drive signal outputs are constant current output. HZ I Microcontroller Input pin for anode drive signal outputs are constant current output. HZ I Microcontroller Input pin for anode drive signal output control signal. When this pin is high, all anode drive signal outputs are high impedance. ML H I Microcontroller Input pin for anode	PADJ0-0/I			
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P L I Microcontroller Input pin for anode drive signal output control signal (Schmitt input). Used to set the anode drive signal output condition at the time that dot is OFF to either low or high impedance with the combination of OFF HZ, A0 HZ, and anode output pulse width adjusting data. A-CLK I Microcontroller Anode output pulse width adjusting clock input pin (Schmitt input). OUT 1 to O Organic EL Anode drive signal output pins for organic El	A0 HZ	I	Microcontroller	Used to set the anode drive signal output condition at the time that dot is OFF to either
P L I Input pin for anode drive signal output control signal (Schmitt input). Used to set the anode drive signal output condition at the time that dot is OFF to either low or high impedance with the combination of OFF HZ, A0 HZ, and anode output pulse width adjusting data. A-CLK I Microcontroller Anode output pulse width adjusting clock input pin (Schmitt input). OUT 1 to O Organic EL Anode drive signal output pins for organic El				
P L I Microcontroller Used to set the anode drive signal output condition at the time that dot is OFF to either low or high impedance with the combination of OFF HZ, A0 HZ, and anode output pulse width adjusting data. A-CLK I Microcontroller Anode output pulse width adjusting clock input pin (Schmitt input). OUT 1 to O Organic EL Anode drive signal output pins for organic El				
A-CLK I Microcontroller Anode output pulse width adjusting data. OUT 1 to O Organic EL Anode drive signal output pins for organic El			Mioroocataalla	
A-CLK I Microcontroller Anode output pulse width adjusting clock input pin (Schmitt input). OUT 1 to O Organic EL Anode drive signal output pins for organic El	ΡL		wicrocontroller	low or high impedance with the combination of OFF HZ, A0 HZ, and anode output pulse
OUT 1 to Organic EL Anode drive signal output pins for organic EL				
	A-CLK	I	Microcontroller	Anode output pulse width adjusting clock input pin (Schmitt input).
	OUT 1 to	0	Organic EL	Anodo drivo signal output nino for organia El
		0		Anoue unve signal output pins for organic EL.

FUNCTION TABLE

- 1. Operation during Transfer of Anode Output Current Adjusting Data and Anode Output Pulse Width Adjusting Data
 - When \overline{F}/R is low

	Inpu	ut			Sh	ift R	egister				Late	ch		Output
		PADJ							PAO	PAO		PAO	PAO	PADJ
RESET	D-CLK	m-I/O,	STB	PO	PO		PO	PO	m-1,	m-2,		m-127,	m-128,	m-O/I,
RESET	D-CLK	IADJ	315	k-1	k-2		k-127	k-128	IAO	IAO		IAO	IAO	IADJ
		n-I/O							n-1	n-2		n-127	n-128	n-O/I
L	Х	Х	Х	L	L		L	L	L	L		L	L	L
	_				L PO PO PO					la.	vori	abla		Invariable
		L	L	L	k-1 k-126 k-127 Invariable								Invariable	
		н		н	PO		PO	PO		Invariable				
			L		k-1		k-126	k-127		In	van	able		Invariable
							iable			l.a		PO		
Н	▼_	L	L		I	nvar	lable			In	van	able		k-128
										1		abla		PO
		Н	L		I	nvar	iable			In	vari	able		k-128
			L	Invariable						In	vari	able		Invariable
	L	х		Invariable				PO	PO		PO	PO	Inveriable	
			Н	Invariable					k-1	k-2		k-127	k-128	Invariable

m = 0 to 3 n = 0, 1 k = 0 to 5

- 2. Operation during Transfer of Anode Output Current Adjusting Data and Anode Output Pulse Width Adjusting Data
 - \bullet When \overline{F}/R is high

	Inp	ut			Shift Register						Lato	h		Output
		PADJ							PAO	PAO		PAO	PAO	PADJ
RESET	D-CLK	m-O/I,	STB	PO	PO		PO	PO	m-128,	m-127,		m-2,	m-1,	m-I/O,
RESET	D-CLK	IADJ	315	k-128	k-127		k-2	k-1	IAO	IAO		IAO	IAO	IADJ
		n-O/I							n-128	n-127		n-2	n-1	n-I/O
L	х	Х	х	L	L		L	L	L	L		L	L	L
					L PO PO PO					In		able		Inveriable
		L	L	L	L k-128 k-3 k-2						vana		Invariable	
		Н		Н	PO PO PO Invariable						Inveriable			
		н	L	п	k-128		k-3	k-2		In	varia	adie		Invariable
Н	_				Inv	: .	hla			In		able		PO
п		L	L		Inv	ana	lible			In	vana	able		k-1
					L									PO
		Н	L		Invariable					in	varia	able		k-1
			L		Invariable					In	varia	able		Invariable
	L	х			Invariable				PO	PO		PO	PO	las se nie la la
			Н		Invariable				k-128	k-127		k-2	k-1	Invariable

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3. Operation of Output Section

ΗZ	ALL H	ALL L	OFF HZ	A0 HZ	ΡL	COMP OUTn	PWM Data n	OUTn
L	Х	Х	Х	Х	Х	Х	Х	High impedance
	Н	Х	Х	Х	Х	Х	Х	Constant current output
		Н	Х	Х	Х	х	Х	Low
					L	Н	Х	Constant current output
						L	Х	Low
			L	х	н	н	One of PWM data n is "H"	Low
						L	All "L"	High impedance
						Н	Х	Constant current output
					L	L	One of PWM data n is "H"	High impedance
Н	L			L			All "L"	Low
	L	L			н	Н	One of PWM data n is "H"	Low
			н			L	All "L"	High impedance
			П			Н	Х	Constant current output
					L	L	One of PWM data n is "H"	High impedance
				Н			All "L"	High impedance
					н	Н	One of PWM data n is "H"	Low
						L	All "L"	High impedance

Note: When setting the STB pin to a high level, do so only when both the \overline{HZ} pin and the ALL L pin are high or both are low.

OUTPUT WAVEFORMS

1. When OFF HZ, A0 HZ, and P L are all low

RESET											
HZ											
ALL H											
ALL L											
OFF HZ	L										
A0 HZ	L										
ΡL	L										
PWM DATAm			Data: 4	D	ata: 4			Da	ata: 4	_	
PWM DATAn			Data: 15	D	ata: 0			Da	ata: 0		
D-CLK											
STB							\Box				
A-CLK						,					
OUTm	_	ΗZ			L		L		L	 _ н	
OUTn		ΗZ				L	L	L		Н	
					1						

2. When OFF HZ is high and A0 HZ and P L are low

RESET HZ									
ALL H									
ALL L									
OFF HZ	Н								
A0 HZ	L								
ΡL	L								
PWM DATAm			Data: 4	Data: 4			Data: 4		
PWM DATAn			Data: 15	Data: 0			Data: 0		
D-CLK									
STB			Γ						
A-CLK									
OUTm		ΗZ		HZ		L	HZ	Н	
OUTn		ΗZ			HZ	L	L	н	

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RESET								
HZ								
ALL H								
ALL L								
OFF HZ	н							
A0 HZ	Н							
ΡL	L							
PWM DATAm			Data: 4	Data: 4		Data: 4		
PWM DATAn			Data: 15	Data: 0		Data: 0		
D-CLK								
STB								
A-CLK								
OUTm		ΗZ		HZ	L	HZ	н	
OUTn		ΗZ		HZ	L	HZ	н	

3. When OFF HZ and A0 HZ are high and P L is low

4. When OFF HZ and A0 HZ are low and P L is controlled by pulse

RESET												
ΗZ												
ALL H												
ALL L												
OFF HZ	L											
A0 HZ	L											
ΡL	L											
PWM DATAm			Data: 4	Da	ata: 4				Da	ata: 4		
PWM DATAn			Data: 15	Da	ata: 0				Da	ata: 0		
D-CLK												
STB												
A-CLK												
OUTm		ΗZ			L		L	L		L	н	
OUTn		ΗZ				L	L	ΗZ	L		н	

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RESET ΗZ ALL H ALL L OFF HZ н A0 HZ L Γ ΡL L Data: 4 Data: 4 Data: 4 **PWM DATAm** Data: 15 Data: 0 Data: 0 PWM DATAn D-CLK STB A-CLK OUTm ΗZ ΗZ L ΗZ Н ΗZ OUTn Н ΗZ HZ HZ HZ

5. When OFF HZ is high, A0 HZ is low, and P L is controlled by pulse

6. When OFF HZ and A0 HZ are high and P L is controlled by pulse

RESET													
HZ													
ALL H													
ALL L													
OFF HZ	н												
A0 HZ	н												
ΡL	L												
PWM DATAm			Data: 4		Data: 4				Da	ata: 4			
PWM DATAn			Data: 15		oata: 0				Da	ata: 0			
D-CLK													
STB			Γ										
A-CLK											11111	_	
OUTm		ΗZ			HZ		ΗZ	L		ΗZ		Н	
OUTn		ΗZ				 ΗZ	ΗZ	ΗZ	ΗZ			н	
				1	1								

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Logic power supply voltage	V _{DD}	Ta = 25°C	-0.3 to +6.5	V
EL drive power supply voltage (anode)	V _{DISP}	Ta = 25°C	-0.3 to +35	V
Logic input voltage	V _{IN}	Ta = 25°C	-0.3 to V _{DD} + 0.3	V
Logic output voltage	Vout	Ta = 25°C	-0.3 to V _{DD} + 0.3	V
EL output current adjustment voltage	V _{EL}	Ta = 25°C	-0.3 to V _{DISP} + 0.3	V
EL driver output voltage	V _{OUT-EL}	Applied to OUT1 to OUT128	–0.3 to V _{DISP} + 0.3	V
EL driver output voltage (pulse) ^{*1}	V _{OUT-ELP}	Applied to OUT1 to OUT128	$-V_{\text{DISP}}$ to $2\times V_{\text{DISP}}$	V
	I _{ELH} (source)	Applied to OUT1 to	-1.5	mA
EL driver output current	I _{ELL} (sink)	OUT128	50	mA
Storage temperature	Tstg	_	-40 to +125	°C

*1 Consult Oki for customization of pulse width.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Logic power supply voltage	V _{DD}	—	3.0 to 5.5	V
EL drive power supply voltage (anode)	V _{DISP}	—	8 to 30	V
Logic input voltage	V _{IN}	—	0.0 to V_{DD}	V
EL output current adjustment voltage	V _{EL}	—	4 to $V_{\text{DISP}} - 3$	V
EL driver output current	I _{ELH} (source)	Applied to OUT1 to OUT128 Current adjustment range = 100%	-0.1 to -1.0	mA
	I _{ELL} (sink)	Applied to OUT1 to OUT128	0 to 40	mA
Junction operating temperature	Тјор	—	-40 to +125	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics 1

$V_{DD} = 3.0 \text{ to } 5.5 \text{ V}, V_{DISP} = 8 \text{ to } 30 \text{ V}, \text{ Tjop} = -40 \text{ to } +125^{\circ}$							
Parameter	Symbol	Applicable Pins	Condition	Min.	Тур.	Max.	Unit
"H" input voltage	V _{IH}	All input pins	—	$0.8V_{DD}$	_	V _{DD}	V
"L" input voltage	VIL	All input pins	—	0	—	$0.2V_{DD}$	V
Schmitt voltage width	$V_{\rm SH}$	D-CLK, A-CLK, STB, A-CLK, ALL H, ALL L	$V_{DD} = 5.0 V$	0.4	1.0	1.6	V
"H" input current	I _{IH1}	$\label{eq:linear_state} \begin{array}{l} \mbox{Inputs other than} \\ \hline \mbox{RESET}, \mbox{HZ}, \mbox{ALL H}, \\ \mbox{ALL L}, \mbox{V}_{\mbox{EL}} \mbox{SEL}, \mbox{and} \\ \hline \mbox{F/R} \end{array}$	$V_{DD} = 5.5 V$ $V_{I} = 5.5 V$	-10	_	10	μΑ
	I _{IH2}	$\overline{\text{RESET}}$, $\overline{\text{HZ}}$, ALL H, ALL L, V _{EL} SEL, $\overline{\text{F}}$ /R	$V_{DD} = 5.5 V$ $V_{I} = 5.5 V$	40	100	200	μΑ
"L" input current	I _{IL1}	Inputs other than RESET, HZ, ALL H, ALL L, V _{EL} SEL, and F/R	$V_{DD} = 5.5 V$ $V_i = 0.0 V$	-10	_	10	μA
	$I_{\rm IL2}$	$\overline{\text{RESET}}, \overline{\text{HZ}}, \text{ALL H}, \\ \text{ALL L}, V_{\text{EL}}\text{SEL}, \overline{\text{F}}/\text{R}$	$V_{DD} = 5.5 V$ $V_{I} = 0.0 V$	-10	—	10	μΑ
"H" output voltage	V _{OH}	PADJm-I/O, PADJm-O/I, IADJn-I/O, IADJn-O/I	$V_{DD} = 3.0 \text{ V}$ $I_0 = -200 \mu\text{A}$	$0.8V_{DD}$	_	_	V
"L" output voltage	V _{OL}	PADJm-I/O, PADJm-O/I, IADJn-I/O, IADJn-O/I	V_{DD} = 3.0 V I_{O} = 200 μ A	_	_	$0.2V_{DD}$	V
Anode driver ON current 1	I _{ELON1}	OUT1 to OUT128	$\begin{array}{l} V_{\text{DISP}} = 24 \ V \\ V_{\text{EL}} = V_{\text{O}} = 15 \ V \\ V_{\text{EL}} \text{SEL} = \text{high} \\ \text{R-ADJ} = 30 \ \text{k}\Omega \\ \text{Current adjustment range} \\ = 100\% \end{array}$	465 (-7%)	-500	–535 (+7%)	μΑ
Anode driver ON current 2	I _{ELON2}	OUT1 to OUT128	$V_{DISP} = 24 V$ $V_{EL} = V_O = 15 V$ $V_{EL}SEL = high$ $R-ADJ = 30 k\Omega$ Current adjustment range = 66%	306 (-7%)	-330	–353 (+7%)	μΑ
Anode driver ON current 3	I _{ELON3}	OUT1 to OUT128	$V_{DISP} = 24 V$ $V_{EL} = V_0 = 15 V$ $V_{EL}SEL = high$ $R-ADJ = 30 k\Omega$ Current adjustment range = 33%	153 (7%)	-165	-177 (+7%)	μΑ
Anode driver ON current 4	I _{ELON4}	OUT1 to OUT128	$V_{DISP} = 24 V$ $V_{EL}=V_{O} = 7.5 V$ $V_{EL}SEL = high$ $R-ADJ = 60 k\Omega$ Current adjustment range = 100%	-112 (-10%)	-125	-138 (+10%)	μΑ
Anode driver ON current 5	I _{ELON5}	OUT1 to OUT128	$V_{\text{DISP}} = 24 \text{ V}$ $V_{\text{EL}} = V_0 = 7.5 \text{ V}$ $V_{\text{EL}}\text{SEL} = \text{high}$ $R-\text{ADJ} = 60 \text{ k}\Omega$ Current adjustment range $= 66\%$	-74 (-10%)	-82.5	-91 (+10%)	μΑ
Anode driver ON current 6	I _{ELON6}	OUT1 to OUT128	$V_{\text{DISP}} = 24 \text{ V}$ $V_{\text{EL}} = V_{\text{O}} = 7.5 \text{ V}$ $V_{\text{EL}}\text{SEL} = \text{high}$ $R\text{-ADJ} = 60 \text{ k}\Omega$ Current adjustment range $= 33\%$	-37.5 (-12%)	-41.25	-46 (+12%)	μΑ

V_{DD} = 3.0 to 5.5 V, V_{DISP} = 8 to 30 V, Tjop = -40 to +125°C

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DC Characteristics 2

Parameter	Symbol	Applicable Pins	Condition	Min.	Тур.	Max.	Unit
Anode driver ON current 7	I _{ELON7}	OUT1 to OUT128	$V_{\text{DISP}} = 24 \text{ V}$ $V_{\text{O}} = 15 \text{ V}$ $V_{\text{EL}}\text{SEL} = \text{Iow}$ $\text{R-ADJ} = 10 \text{ k}\Omega$ Current adjustment range $= 100\%$	-415 (-17%)	-500	585 (+17%)	μΑ
Anode driver ON current 8	I _{ELON8}	OUT1 to OUT128	$V_{\text{DISP}} = 24 \text{ V}$ $V_{\text{O}} = 15 \text{ V}$ $V_{\text{EL}}\text{SEL} = \text{low}$ $\text{R-ADJ} = 10 \text{ k}\Omega$ Current adjustment range $= 66\%$	–274 (–17%)	-330	–386 (+17%)	μΑ
Anode driver ON current 9	I _{ELON9}	OUT1 to OUT128	$V_{\text{DISP}} = 24 \text{ V}$ $V_{\text{O}} = 15 \text{ V}$ $V_{\text{EL}}\text{SEL} = \text{Iow}$ $\text{R-ADJ} = 10 \text{ k}\Omega$ Current adjustment range $= 33\%$	-137 (-17%)	-165	-193 (+17%)	μΑ
Anode driver low output current 1	I _{ELL1}	OUT1 to OUT128	$V_{DISP} = 8 V$ $V_{O} = 8 V$	16		_	mA
Anode driver low output current 2	I _{ELL2}	OUT1 to OUT128	$V_{\text{DISP}} = 30 \text{ V}$ $V_{\text{O}} = 30 \text{ V}$	60		—	mA
Anode driver low output current 3	I _{ELL3}	OUT1 to OUT128	$V_{DISP} = 8 V$ $V_{O} = 1 V$	500	_	—	μA
V _{DISP} dependence coefficient for anode driver ON current *1	ΔI_{ELON1}	OUT1 to OUT128	$V_{DISP} = 17 \text{ to } 30 \text{ V}$ $V_{EL} = V_0 = 15 \text{ V}$ $R-ADJ = 30 k\Omega$ Current adjustment range $= 100\%$	-2.5	0	2.5	%/V
V _o dependence coefficient for anode driver ON current *2	ΔI_{ELON2}	OUT1 to OUT128	$V_{DISP} = 24 V$ $V_{EL} = 15 V$ $V_{O} = 8 \text{ to } 21 V$ $R-ADJ = 30 k\Omega$ Current adjustment range $= 100\%$	-2.5	0	2.5	%/V
Temperature coefficient for anode driver ON current	ΔI_{ELON3}	OUT1 to OUT128	$V_{DISP} = 24 V$ $V_{EL} = V_0 = 15 V$ R-ADJ = 30 kΩ Current adjustment range = 100%	-0.1	0	0.1	%/°C
Relative error between dots (excluding adjoining dots) for anode driver ON current	ΔI_{ELON4}	OUT1 to OUT128	$\begin{array}{l} V_{\text{DISP}} = 24 \text{ V} \\ V_{\text{EL}} = V_{\text{O}} = 15 \text{ V} \\ \text{R-ADJ} = 30 \text{k} \Omega \\ \text{Current adjustment range} \\ = 100\% \\ \text{OUT1 to OUT128} = "ON" \\ \text{Inside one chip.} \end{array}$	-5	0	5	%
Tilt inside chip for anode driver ON current *3	ΔI_{ELON5}	OUT1 to OUT4 OUT63 to OUT66 OUT125 to OUT128	$\label{eq:VDISP} \begin{array}{l} V_{\text{DISP}} = 24 \text{ V} \\ V_{\text{EL}} = V_{\text{O}} = 15 \text{ V} \\ \text{R-ADJ} = 30 \text{k}\Omega \\ \text{Current adjustment range} \\ = 100\% \\ \text{OUT1 to OUT128} = "\text{ON"} \\ \text{Inside one chip.} \end{array}$	-3	0	3	%
Relative error between adjoining dots for anode driver ON current *4	ΔI_{ELON6}	OUT1 to OUT128	$V_{\text{DISP}} = 24 \text{ V}$ $V_{\text{EL}} = V_{\text{O}} = 15 \text{ V}$ $\text{R-ADJ} = 30 \text{k}\Omega$ Current adjustment range $= 100\%$ OUT1 to OUT128 = "ON" Inside one chip.	-2	0	2	%

- *1 V_{DISP} dependence coefficient depends on the following conditions: $I(V_{DISP} = nV)$: Anode driver ON current at $V_{DISP} = nV$. $\Delta I_{ELON1} = [I(V_{DISP} = nV) - I(V_{DISP} = (n+1)V)]/{[I(V_{DISP} = nV) + I(V_{DISP} = (n+1)V)]/{2} \times 100}$
- *2 V_O dependence coefficient depends on the following conditions: $I(V_O = nV)$: Anode driver ON current at V_O = nV. $\Delta I_{ELON2} = [I(V_O = nV) - I(V_O = (n-1)V)]/{[I(V_O = nV) + I(V_O = (n-1)V)]/2} \times 100$
- *3 Tilt inside chip depends on the following conditions: Cave: Average output current of OUT1 to 4, OUT63 to 66, and OUT125 to 128. Lave: Average output current of OUT1 to 4. Rave: Average output current of OUT125 to 128. $\Delta I_{ELON5} = (Lave - Cave)/Cave$ $\Delta I_{ELON5} = (Rave - Cave)/Cave$
- *4 A relative error between adjoining dots depends on the following condition: $(I_{ELON(N+1)} I_{ELON(N)})I_{ELON(N)}$

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Supply Current

Parameter	Symbol	Applicable Pins	V_{DD} = 3.0 to 5.5 V, V Condition	Min.	Тур.	Max.	Unit
raianeter		Аррисаріс і ша	$V_{\text{DISP}} = 30 \text{ V}$	101111.	тур.	Max.	Onit
			$V_{\text{DISP}} = 30 \text{ V}$ $V_{\text{EL}} = 15 \text{ V}$				
			$V_{EL} = 15 V$ A-CLK = 5 MHz				
			$R-ADJ = 30 k\Omega$			5.0	mA
	I _{DISP1}	V _{DISP}		—	—		
			Current adjustment range = 100%				
			Output = open		l		
			PWM data = other than "0"				
			$V_{DD} = 0 V$				
	I _{DISP2}	V _{DISP}	$V_{\text{DISP}} = 30 \text{ V}$	-			
			V _{EL} = 15 V		—	300	μA
			R-ADJ = 30 kΩ				
Supply current			Output = open				
		V _{DD}	$V_{DD} = 5.5 V$		_	18	mA
			D-CLK = 5 MHz	_			
			DATA = "101010"				
		-	$V_{DD} = 5.5 V$		_	20	mA
	I _{DD1}	V _{DD}	D-CLK, A-CLK = 5 MHz	_			
			DATA = "101010"				
			V _{DD} = 5.5 V				mA
		V _{DD}	A-CLK = 5 MHz	_	_	5	
			DATA = "101010"				
			$V_{DD} = 5.5 V,$				
	I _{DD2} V _{DD}		D-CLK = halted				μA
		V _{DD}	RESET = 0 V	—	—	100	
		All the other inputs are also 0 V.					

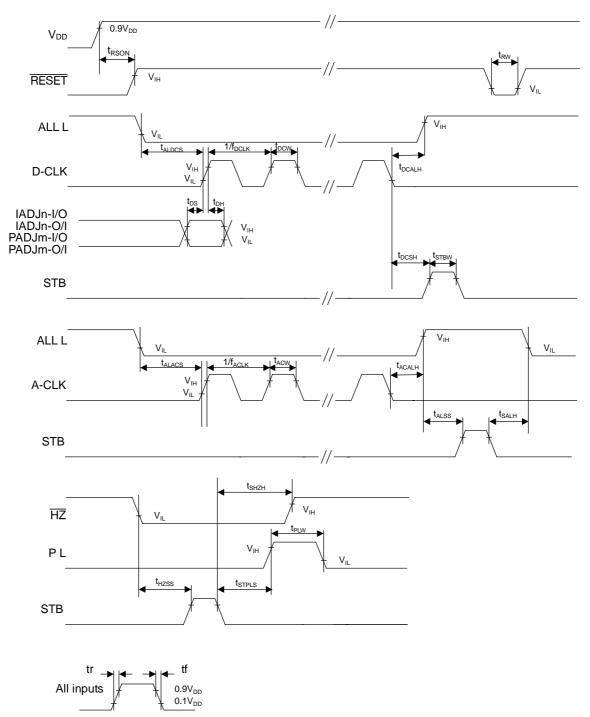
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AC Characteristics

AC Characteristics		V _{DD} = 3.0 to 5.5 V,	$V_{DISP} = 8 to$	o 30 V, Tjo	p = -40 to	o +125°C	
Parameter	Symbol	Applicable pins	Condition	Min.	Тур.	Max.	Unit
D-CLK frequency	f _{DCLK}	D-CLK	—	0		5.0	MHz
D-CLK pulse width	t _{DCW}	D-CLK	—	50		_	ns
A-CLK frequency	f _{ACLK}	A-CLK	—	0		5.0	MHz
A-CLK pulse width	t _{ACW}	A-CLK	—	50		—	ns
DATA→D-CLK setup time	t _{DS}	D-CLK IADJn-I PADJm-I	_	50	_	_	ns
D-CLK→DATA hold time	t _{DH}	D-CLK IADJn-I PADJm-I	_	50	_	_	ns
STB pulse width	t _{STBW}	STB	—	50		—	ns
ALL L→STB setup time	t _{ALSS}	ALL L, STB	_	100	_	_	ns
STB→ALL L hold time	t _{SALH}	ALL L, STB	_	100	—	_	ns
HZ→STB setup time	t _{HZSS}	HZ, STB	_	100	_	_	ns
STB→HZ hold time		HZ, STB	_	100	_	_	ns
ALL L→D-CLK setup time	t _{ALDCS}	ALL L, D-CLK	—	100	_	—	ns
D-CLK→ALL L hold time	t _{DCALH}	ALL L, D-CLK	_	100	_	—	ns
ALL L→A-CLK setup time	I talacs I AILL A-CLK		_	100	—	_	ns
$ \begin{array}{c c} A\text{-}CLK \rightarrow ALL \ L \\ hold \ time \end{array} t_{ACALH} ALL \ L, \ A\text{-}CL \\ \end{array} $		ALL L, A-CLK	_	100		_	ns
P L pulse width	t _{PLW}	PL	—	100	—	—	ns
P L→ALL L setup time	t _{PLALS}	ALL L, P L	_	100	—	_	ns
STB→P L setup time	tstpls	P L, STB	_	100	_	_	ns
D-CLK→STB hold time	D-CLK-STB		_	50	—	—	ns
RESET pulse width	RESET pulse width t _{RW} RESET		_	100		_	ns
RESET execution time	RESET execution Trees RESET		_	250		_	ns
			_	-	_	2.0	μs
Input signal rise/fall tr time tf All inputs			_		500	ns	

TIMING DIAGRAM

Data Input



DESCRIPTION OF OPERATION

Initial Settings

Following initial settings can be made by setting the $\overline{\text{RESET}}$ pin to low.

- The shift register outputs and latch circuit outputs become all low.
- Anode drive signal output pins (OUT1 to 128) become high impedance.

Anode Output Current Adjustment

- 1. Output current adjustment for entire output
 - Output current of anode drive signal output pins (OUT1 to OUT128) can be adjusted, as a batch adjustment for all the output pins. Output current is adjusted by varying the value of the resistor connected between the R-ADJ pin and GND. Output current (typ.) at the time that the $V_{EL}SEL$ pin is "high" and "low" is given by the following expressions:

[When the V_{EL}SEL pin is "high"] Output current (typ.) = V_{EL} pin voltage \div R-ADJ resistance value

[When the V_{EL}SEL pin is "low"] Output current (typ.) = 5 V \div R-ADJ resistance value

2. Output current adjustment for each output

Output current of anode drive signal output pins (OUT1 to OUT128) can be adjusted for each output pin. Adjustment of each output current is made by bit data IADJ0-n and IADJ1-n. This 2-bit data is written in the shift register at the rising edge of the D-CLK signal and latched at the rising edge of the STB signal.

Relation between IADJ0-n, IADJ1-n, and output current is shown below.

IADJ1-n	IADJ0-n	Current adjustment range
0	0	0%
0	1	33%
1	0	66%
1	1	100%

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3. Output pulse width adjustment

Output pulse width of anode drive signal output pins (OUT1 to OUT128) can be adjusted for each output pin. Adjustment of each output pulse width is made by 4-bit data PADJ0-n, PADJ1-n, PADJ2-n, and PADJ3-n. This 4-bit data is written in the shift register at the rising edge of the D-CLK signal and latched at the rising edge of the STB signal. An anode drive signal output pin is configured as constant current output until the number of A-CLK pulses becomes equal to the output data of 4 bits of PADJ0-n, PADJ1-n, PADJ2-n, and PADJ3-n. When they have matched, the output becomes low or high impedance at the rising edge of the A-CLK pulse that has matched the output data of PADJ0-n, PADJ1-n, PADJ2-n.

Relation between PADJ0-n, PADJ1-n, PADJ2-n, and PADJ3-n and output pulse width is shown below.

PADJ3-n	PADJ2-n	PADJ1-n	PADJ0-n	Output pulse width
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Setting of Output Condition When Dot is OFF

The output condition when dot is OFF is set with the combination of \overline{HZ} , ALL L, OFF HZ, A0 HZ, and P L signals. See "3. Operation of Output Section" in "FUNCTION TABLE" and the section of "OUTPUT WAVEFORMS".

Power Applying Sequence

It is possible to apply power first to V_{DD} or V_{DISP} . When power is applied to V_{DISP} , and V_{DD} is 2.5 V or less, following operating states occur.

- Constant current source circuit does not operate.
- Anode drive signal output pins (OUT1 to 128) become high impedance.

Make the $\overline{\text{RESET}}$ pin high at least 250 ns after applying power to V_{DD}. (Refer to $\overline{\text{RESET}}$ execution time in AC Characteristics.)

REVISION HISTORY

Document		Page			
No.	Date	Previous Edition	Current Edition	Description	
PEDL9361-01	Dec. 12, 2002	-	-	Preliminary edition 1	

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