OKI Semiconductor

PEDL9361-01
Issue Date:Dec. 12, 2002

ML9361 Preliminary

128-Channel Organic EL Anode Driver

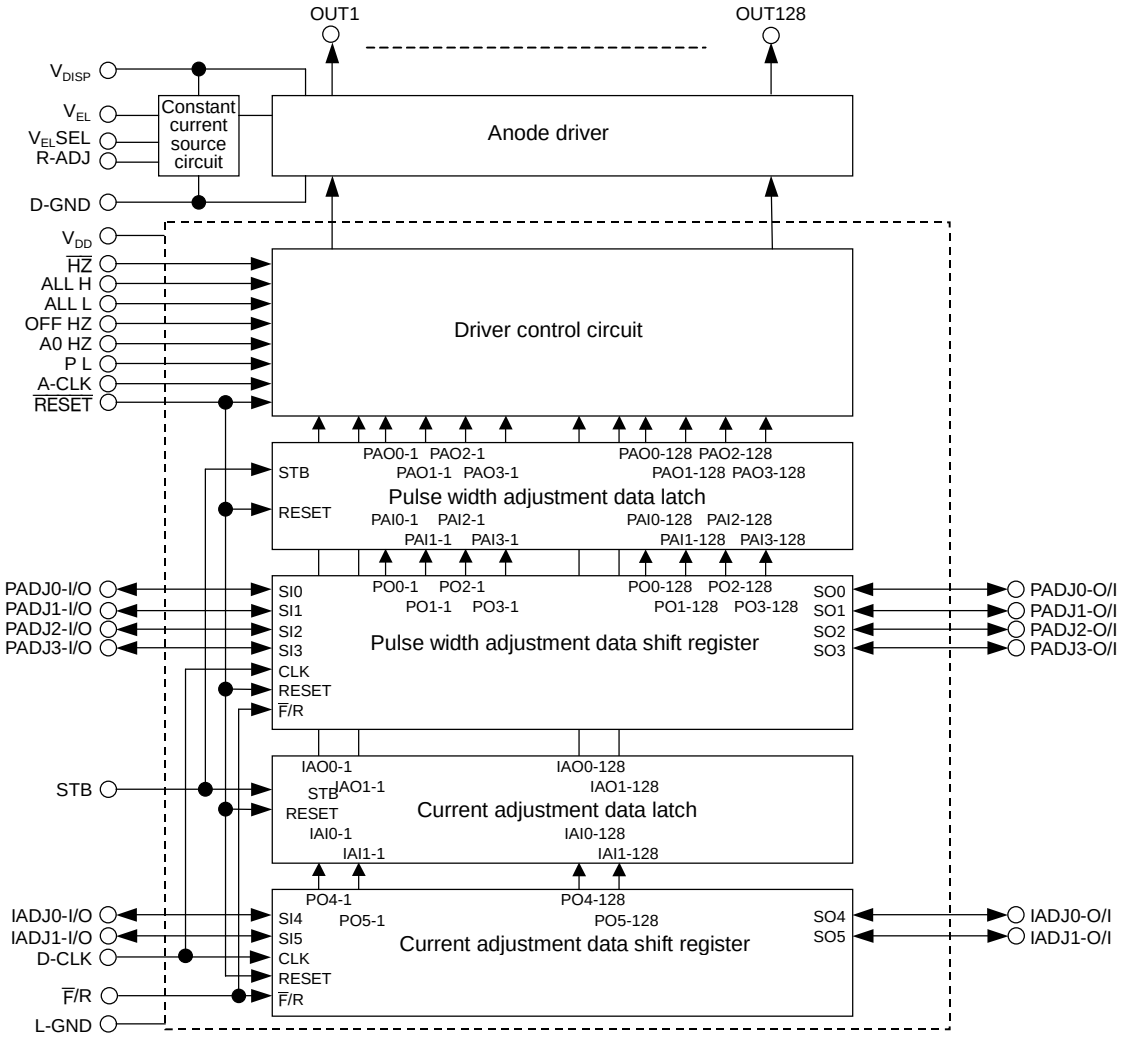
GENERAL DESCRIPTION

The ML9361 is an organic EL anode driver LSI with 128 drivers. The anode driver is constant current output type and allows adjustment of current and pulse width for each output. Since this LSI has the output condition setting function, which allows setting of all outputs High, all outputs Low, and all outputs High Impedance, the user can set driving methods suited to the characteristics of individual organic EL panel. When combined with ML9371 the organic EL cathode driver, the ML9361 can drive a 64 × 128 full-dot panel.

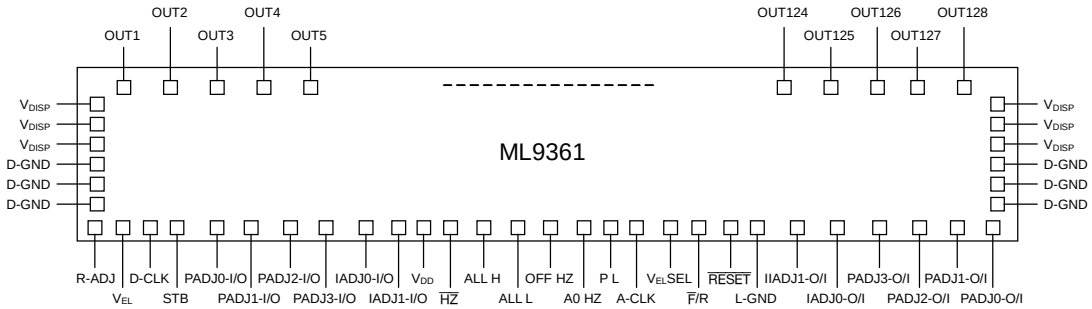
FEATURES

- Logic power supply voltage : 3.0 to 5.5 V
- EL drive voltage : 8.0 to 30 V (max.)
- Anode outputs : 128 outputs
- Anode high output current : –1.0 mA (constant current output, current adjustment range = at 100%)
- Anode low output current : 40 mA (max.)
- Anode low ON-resistance : 500Ω (max.)
- Anode output current adjustment range : 0%, 33%, 66%, and 100% (for each output)
- Output pulse width adjustment : Adjustable in 16 different degrees (adjusted by external clock input, for each output)
- All outputs High, all outputs Low, and all outputs High Impedance can be set as output conditions
- Package : Gold bump chip (TCP is tailored for each customer requirement)

BLOCK DIAGRAM



PIN CONFIGURATION (Gold bump chip)



PIN DESCRIPTION

Symbol	I/O	Connected to	Description
V_{DISP} V_{DD} D-GND L-GND	—	Power supply	V_{DISP} is a power supply pin for anode driver circuit and constant current source circuit. V_{DD} is the logic circuit power supply pin. D-GND is a ground pin for anode driver circuit and constant current source circuit. L-GND is a ground pin for logic circuit. D-GND and L-GND should be connected outside the LSI.
V_{EL}	I	Power supply	OUT1 to OUT128 output current setting voltage input pin. Input voltage to this pin is enabled when V_{EL}SEL is high, and disabled when it is low. Leave this pin open or input a voltage within the guaranteed operating range.
V_{EL}SEL	I	Microcontroller	Pin for selecting the output current adjusting voltage for anode driver circuit. • When this pin is low, LSI's internal voltage (5 V) is selected. • When this pin is high, the input voltage at the V_{EL} pin is selected.
R-ADJ	I	Resistor	OUT1 to OUT128 output current setting resistor connection pin.
$\overline{F}$/R	I	Microcontroller	Data transfer direction select signal input pin for current adjusting data shift register and pulse width adjusting data shift register. • When this pin is low, data is transferred starting at POn-1 toward POn-128. (n = 1 to 5) • When this pin is high, data is transferred starting at POn-128 toward POn-1. (n = 1 to 5)
IADJ0-I/O IADJ1-I/O	I/O	Microcontroller, or ML9361 on next stage	Anode output current adjusting data input-output pins. When the $\overline{F}$/R pin is low, these pins are input pins and data is read into at the rising edge of D-CLK. When the $\overline{F}$/R pin is high, these pins are output pins and the output status changes at the falling edge of D-CLK.
IADJ0-O/I IADJ1-O/I	O/I		Anode output current adjusting data input-output pins. When the $\overline{F}$/R pin is high, these pins are input pins and data is read into at the rising edge of D-CLK. When the $\overline{F}$/R pin is low, these pins are output pins and the output status changes at the falling edge of D-CLK.
PADJ0-I/O PADJ1-I/O PADJ2-I/O PADJ3-I/O	I/O	Microcontroller, or ML9361 on next stage	Anode output pulse width adjusting data input-output pins. When the $\overline{F}$/R pin is low, these pins are input pins and data is read into at the rising edge of D-CLK. When the $\overline{F}$/R pin is high, these pins are output pins and the output status changes at the falling edge of D-CLK.
PADJ0-O/I PADJ1-O/I PADJ2-O/I PADJ3-O/I	O/I		Anode output pulse width adjusting data input-output pins. When the $\overline{F}$/R pin is high, these pins are input pins and data is read into at the rising edge of D-CLK. When the $\overline{F}$/R pin is low, these pins are output pins and the output status changes at the falling edge of D-CLK.
D-CLK	I	Microcontroller	Anode output current adjusting data and anode output pulse width adjusting data transfer clock input pin (Schmitt input)
STB	I	Microcontroller	Anode output current adjusting data and anode output pulse width adjusting data latch strobe signal input pin (Schmitt input)
$\overline{RESET}$	I	Microcontroller	Initialization signal input pin. When this pin is set low, the LSI enters the following initial setting states: • Shift register outputs and latch outputs: all "low" • All anode drive signal outputs: "high impedance"
$\overline{HZ}$	I	Microcontroller	Input pin for anode drive signal output control signal. When this pin is low, all anode drive signal outputs are high impedance.
ALL H	I	Microcontroller	Input pin for anode drive signal output control signal (Schmitt input). When this pin is high, all anode drive signal outputs are constant current output.
ALL L	I	Microcontroller	Input pin for anode drive signal output control signal (Schmitt input). When this pin is high, anode drive signal outputs are all low.
OFF HZ	I	Microcontroller	Input pin for anode drive signal output control signal. Used to set the anode drive signal output condition at the time that is OFF to either low or high impedance with the combination of A0 HZ, P L, and anode output pulse width adjusting data.
A0 HZ	I	Microcontroller	Input pin for anode drive signal output control signal. Used to set the anode drive signal output condition at the time that dot is OFF to either low or high impedance with the combination of OFF HZ, P L, and anode output pulse width adjusting data.
P L	I	Microcontroller	Input pin for anode drive signal output control signal (Schmitt input). Used to set the anode drive signal output condition at the time that dot is OFF to either low or high impedance with the combination of OFF HZ, A0 HZ, and anode output pulse width adjusting data.
A-CLK	I	Microcontroller	Anode output pulse width adjusting clock input pin (Schmitt input).
OUT 1 to 128	O	Organic EL anode	Anode drive signal output pins for organic EL.

FUNCTION TABLE

1. Operation during Transfer of Anode Output Current Adjusting Data and Anode Output Pulse Width Adjusting Data
   • When $\overline{F}$/R is low

Input				Shift Register					Latch					Output
$\overline{RESET}$	D-CLK	PADJ m-I/O, IADJ n-I/O	STB	PO k-1	PO k-2		PO k-127	PO k-128	PAO m-1, IAO n-1	PAO m-2, IAO n-2		PAO m-127, IAO n-127	PAO m-128, IAO n-128	PADJ m-O/I, IADJ n-O/I
L	X	X	X	L	L		L	L	L	L		L	L	L
H	↑	L	L	L	PO k-1		PO k-126	PO k-127	Invariable					Invariable
		H	L	H	PO k-1		PO k-126	PO k-127	Invariable					Invariable
	↓	L	L	Invariable					Invariable					PO k-128
		H	L	Invariable					Invariable					PO k-128
	L	X	L	Invariable					Invariable					Invariable
			H	Invariable					PO k-1	PO k-2		PO k-127	PO k-128	Invariable

m = 0 to 3 n = 0, 1 k = 0 to 5

2. Operation during Transfer of Anode Output Current Adjusting Data and Anode Output Pulse Width Adjusting Data
   • When $\overline{F}$/R is high

Input				Shift Register					Latch					Output
$\overline{RESET}$	D-CLK	PADJ m-O/I, IADJ n-O/I	STB	PO k-128	PO k-127		PO k-2	PO k-1	PAO m-128, IAO n-128	PAO m-127, IAO n-127		PAO m-2, IAO n-2	PAO m-1, IAO n-1	PADJ m-I/O, IADJ n-I/O
L	X	X	X	L	L		L	L	L	L		L	L	L
H	↑	L	L	L	PO k-128		PO k-3	PO k-2	Invariable					Invariable
		H	L	H	PO k-128		PO k-3	PO k-2	Invariable					Invariable
	↓	L	L	Invariable					Invariable					PO k-1
		H	L	Invariable					Invariable					PO k-1
	L	X	L	Invariable					Invariable					Invariable
			H	Invariable					PO k-128	PO k-127		PO k-2	PO k-1	Invariable

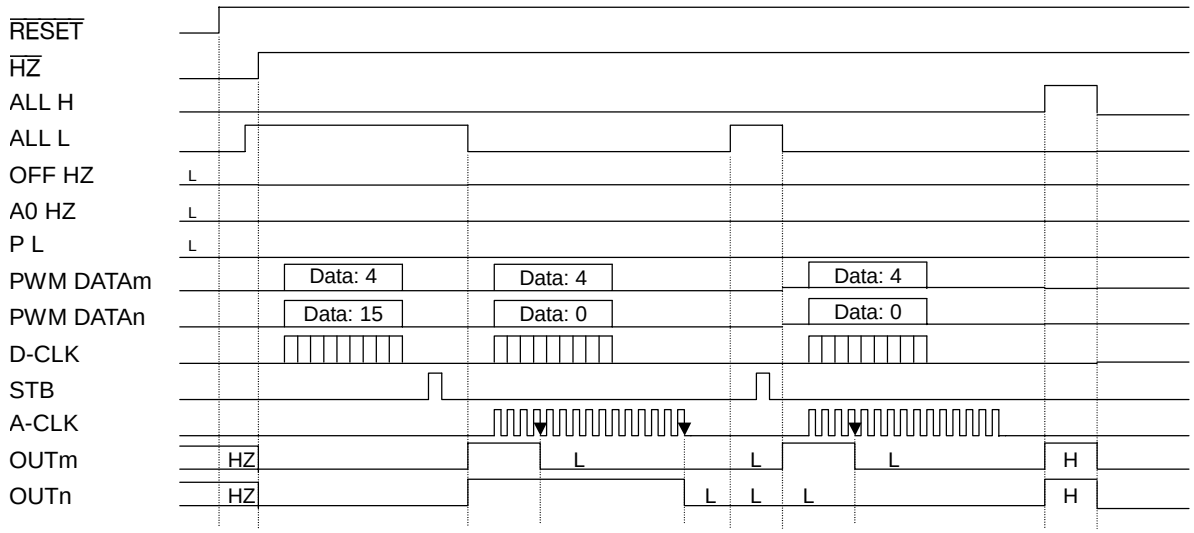
3. Operation of Output Section

$\overline{HZ}$	ALL H	ALL L	OFF HZ	A0 HZ	P L	COMP OUTn	PWM Data n	OUTn
L	X	X	X	X	X	X	X	High impedance
H	H	X	X	X	X	X	X	Constant current output
	L	H	X	X	X	X	X	Low
		L	L	X	L	H	X	Constant current output
						L	X	Low
					H	H	One of PWM data n is “H”	Low
						L	All “L”	High impedance
			H	L	L	H	X	Constant current output
						L	One of PWM data n is “H”	High impedance
							All “L”	Low
					H	H	One of PWM data n is “H”	Low
						L	All “L”	High impedance
				H	L	H	X	Constant current output
						L	One of PWM data n is “H”	High impedance
							All “L”	High impedance
					H	H	One of PWM data n is “H”	Low
						L	All “L”	High impedance

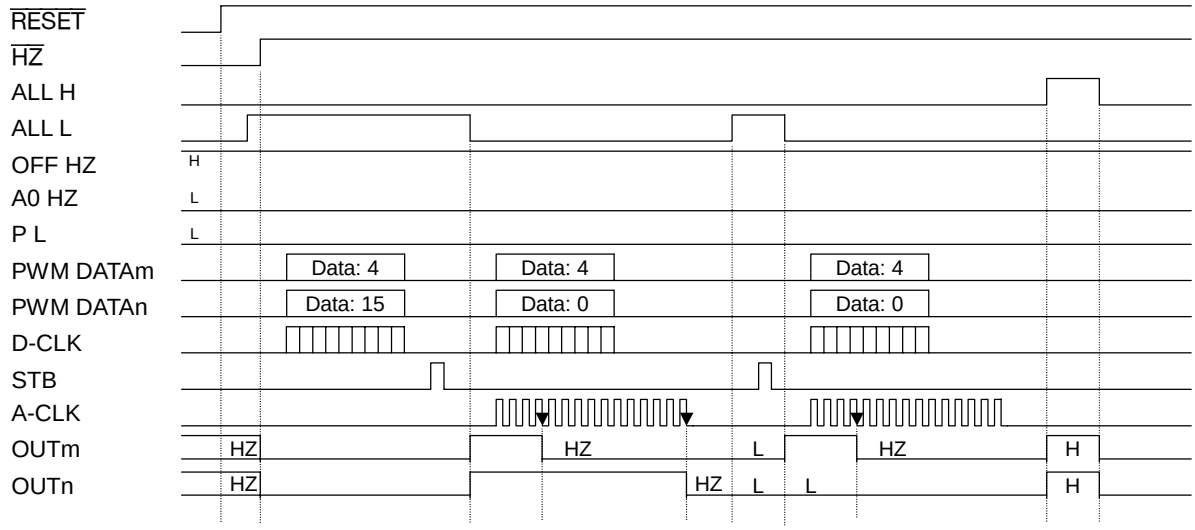
Note: When setting the STB pin to a high level, do so only when both the $\overline{HZ}$ pin and the ALL L pin are high or both are low.

OUTPUT WAVEFORMS

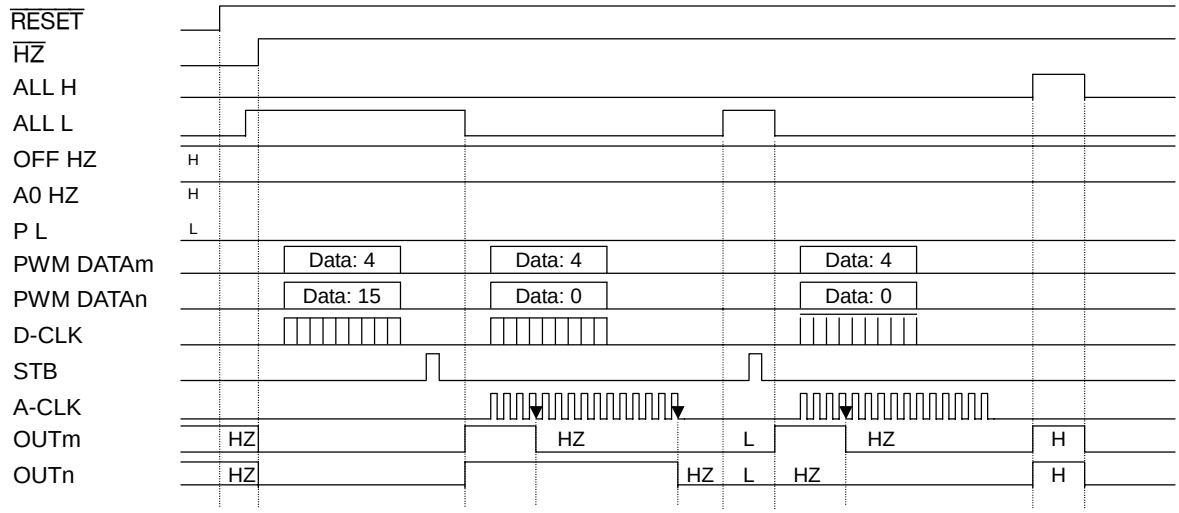
1. When OFF HZ, A0 HZ, and P L are all low



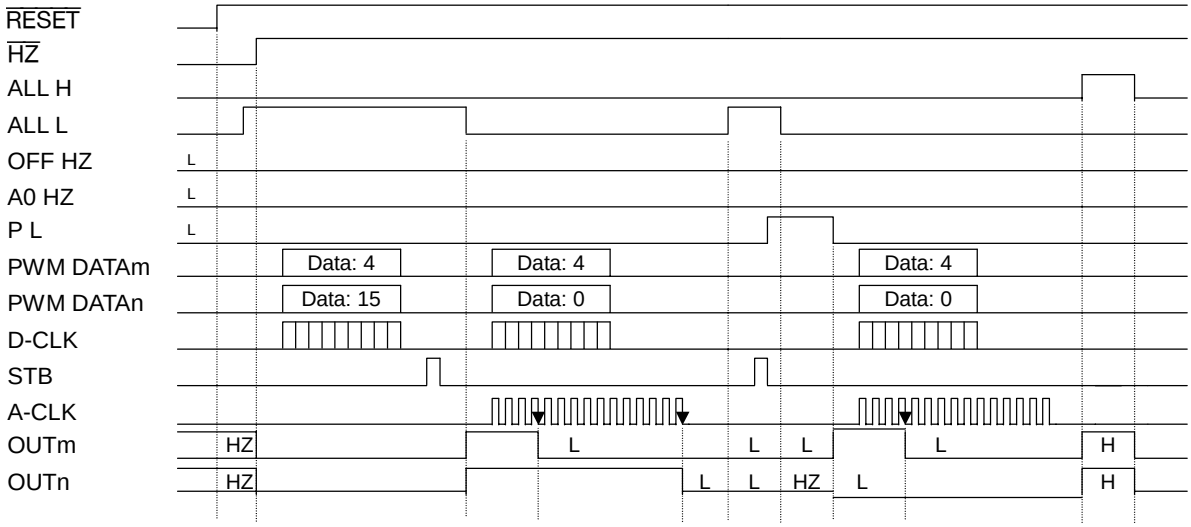
2. When OFF HZ is high and A0 HZ and P L are low



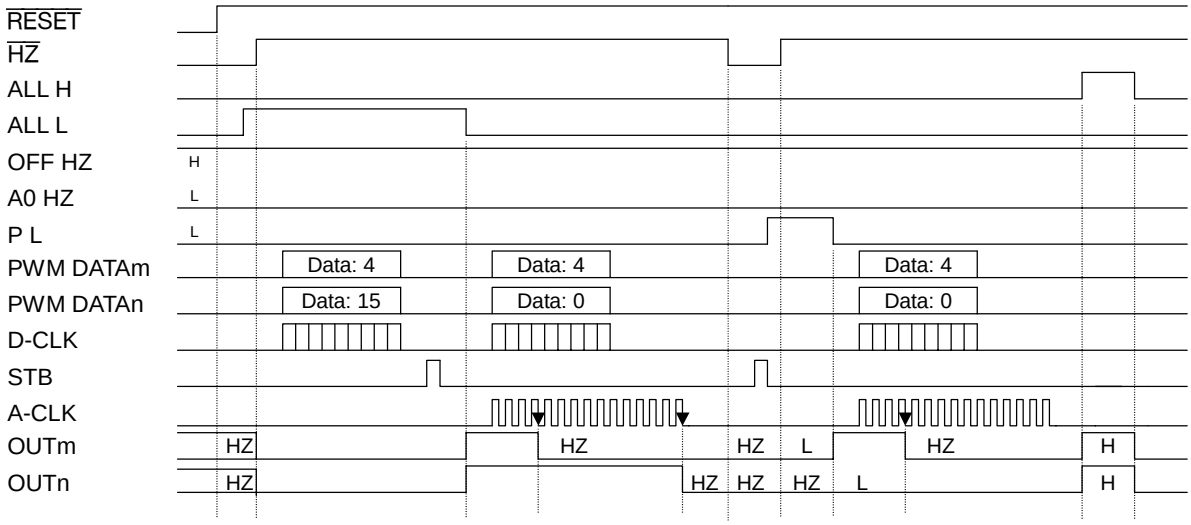
3. When OFF HZ and A0 HZ are high and P L is low



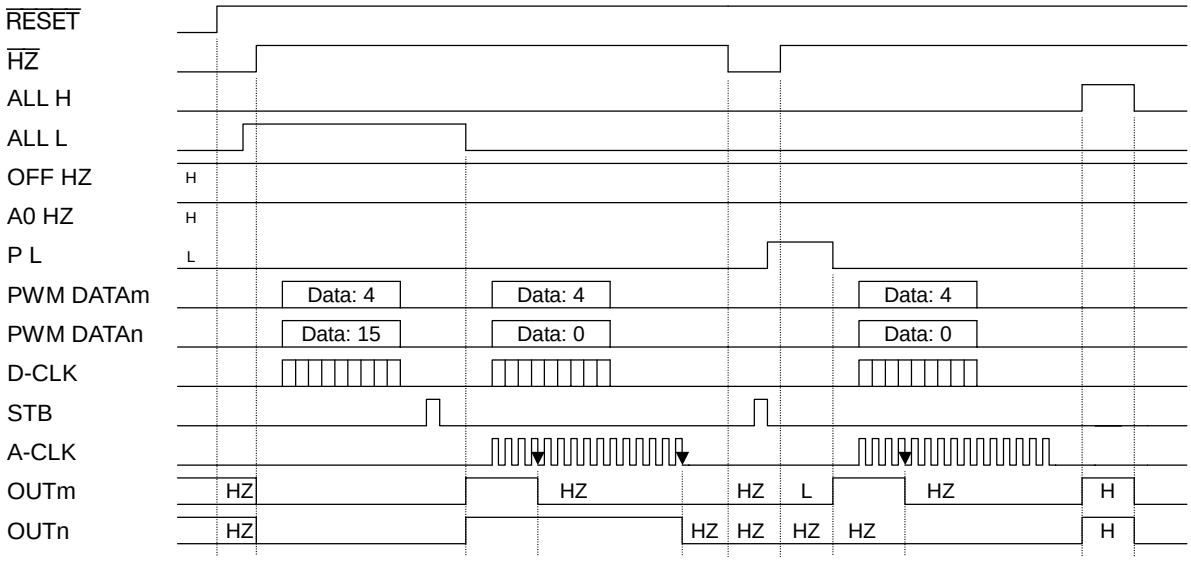
4. When OFF HZ and A0 HZ are low and P L is controlled by pulse



5. When OFF HZ is high, A0 HZ is low, and P L is controlled by pulse



6. When OFF HZ and A0 HZ are high and P L is controlled by pulse



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Logic power supply voltage	V_{DD}	Ta = 25°C	–0.3 to +6.5	V
EL drive power supply voltage (anode)	V_{DISP}	Ta = 25°C	–0.3 to +35	V
Logic input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Logic output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
EL output current adjustment voltage	V_{EL}	Ta = 25°C	–0.3 to V_{DISP} + 0.3	V
EL driver output voltage	V_{OUT-EL}	Applied to OUT1 to OUT128	–0.3 to V_{DISP} + 0.3	V
EL driver output voltage (pulse)*1	$V_{OUT-ELP}$	Applied to OUT1 to OUT128	$-V_{DISP}$ to 2 × V_{DISP}	V
EL driver output current	I_{ELH} (source)	Applied to OUT1 to OUT128	–1.5	mA
	I_{ELL} (sink)		50	mA
Storage temperature	Tstg	—	–40 to +125	°C

*1 Consult Oki for customization of pulse width.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Logic power supply voltage	V_{DD}	—	3.0 to 5.5	V
EL drive power supply voltage (anode)	V_{DISP}	—	8 to 30	V
Logic input voltage	V_{IN}	—	0.0 to V_{DD}	V
EL output current adjustment voltage	V_{EL}	—	4 to V_{DISP} – 3	V
EL driver output current	I_{ELH} (source)	Applied to OUT1 to OUT128 Current adjustment range = 100%	–0.1 to –1.0	mA
	I_{ELL} (sink)	Applied to OUT1 to OUT128	0 to 40	mA
Junction operating temperature	Tjop	—	–40 to +125	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics 1

V_{DD} = 3.0 to 5.5 V, V_{DISP} = 8 to 30 V, Tjop = –40 to +125°C

Parameter	Symbol	Applicable Pins	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	All input pins	—	$0.8V_{DD}$	—	V_{DD}	V
"L" input voltage	V_{IL}	All input pins	—	0	—	$0.2V_{DD}$	V
Schmitt voltage width	V_{SH}	D-CLK, A-CLK, STB, A-CLK, ALL H, ALL L	V_{DD} = 5.0 V	0.4	1.0	1.6	V
"H" input current	I_{IH1}	Inputs other than $\overline{RESET}$, $\overline{HZ}$, ALL H, ALL L, V_{EL}SEL, and $\overline{F}$/R	V_{DD} = 5.5 V V_I = 5.5 V	–10	—	10	µA
	I_{IH2}	$\overline{RESET}$, $\overline{HZ}$, ALL H, ALL L, V_{EL}SEL, $\overline{F}$/R	V_{DD} = 5.5 V V_I = 5.5 V	40	100	200	µA
"L" input current	I_{IL1}	Inputs other than $\overline{RESET}$, $\overline{HZ}$, ALL H, ALL L, V_{EL}SEL, and $\overline{F}$/R	V_{DD} = 5.5 V V_I = 0.0 V	–10	—	10	µA
	I_{IL2}	$\overline{RESET}$, $\overline{HZ}$, ALL H, ALL L, V_{EL}SEL, $\overline{F}$/R	V_{DD} = 5.5 V V_I = 0.0 V	–10	—	10	µA
"H" output voltage	V_{OH}	PADJm-I/O, PADJm-O/I, IADJn-I/O, IADJn-O/I	V_{DD} = 3.0 V I_O = –200 µA	$0.8V_{DD}$	—	—	V
"L" output voltage	V_{OL}	PADJm-I/O, PADJm-O/I, IADJn-I/O, IADJn-O/I	V_{DD} = 3.0 V I_O = 200 µA	—	—	$0.2V_{DD}$	V
Anode driver ON current 1	I_{ELON1}	OUT1 to OUT128	V_{DISP} = 24 V V_{EL} = V_O = 15 V V_{EL}SEL = high R-ADJ = 30 kΩ Current adjustment range = 100%	–465 (–7%)	–500	–535 (+7%)	µA
Anode driver ON current 2	I_{ELON2}	OUT1 to OUT128	V_{DISP} = 24 V V_{EL} = V_O = 15 V V_{EL}SEL = high R-ADJ = 30 kΩ Current adjustment range = 66%	–306 (–7%)	–330	–353 (+7%)	µA
Anode driver ON current 3	I_{ELON3}	OUT1 to OUT128	V_{DISP} = 24 V V_{EL} = V_O = 15 V V_{EL}SEL = high R-ADJ = 30 kΩ Current adjustment range = 33%	–153 (–7%)	–165	–177 (+7%)	µA
Anode driver ON current 4	I_{ELON4}	OUT1 to OUT128	V_{DISP} = 24 V V_{EL}=V_O = 7.5 V V_{EL}SEL = high R-ADJ = 60 kΩ Current adjustment range = 100%	–112 (–10%)	–125	–138 (+10%)	µA
Anode driver ON current 5	I_{ELON5}	OUT1 to OUT128	V_{DISP} = 24 V V_{EL} = V_O = 7.5 V V_{EL}SEL= high R-ADJ = 60 kΩ Current adjustment range = 66%	–74 (–10%)	–82.5	–91 (+10%)	µA
Anode driver ON current 6	I_{ELON6}	OUT1 to OUT128	V_{DISP} = 24 V V_{EL} = V_O =7.5 V V_{EL}SEL = high R-ADJ = 60 kΩ Current adjustment range = 33%	–37.5 (–12%)	–41.25	–46 (+12%)	µA

DC Characteristics 2

V_{DD} = 3.0 to 5.5 V, V_{DISP} = 8 to 30 V, Tjop = –40 to +125°C

Parameter	Symbol	Applicable Pins	Condition	Min.	Typ.	Max.	Unit
Anode driver ON current 7	I_{ELON7}	OUT1 to OUT128	V_{DISP} = 24 V V_O = 15 V V_{EL}SEL = low R-ADJ = 10 kΩ Current adjustment range = 100%	–415 (–17%)	–500	–585 (+17%)	μA
Anode driver ON current 8	I_{ELON8}	OUT1 to OUT128	V_{DISP} = 24 V V_O = 15 V V_{EL}SEL = low R-ADJ = 10 kΩ Current adjustment range = 66%	–274 (–17%)	–330	–386 (+17%)	μA
Anode driver ON current 9	I_{ELON9}	OUT1 to OUT128	V_{DISP} = 24 V V_O = 15 V V_{EL}SEL = low R-ADJ = 10 kΩ Current adjustment range = 33%	–137 (–17%)	–165	–193 (+17%)	μA
Anode driver low output current 1	I_{ELL1}	OUT1 to OUT128	V_{DISP} = 8 V V_O = 8 V	16	—	—	mA
Anode driver low output current 2	I_{ELL2}	OUT1 to OUT128	V_{DISP} = 30 V V_O = 30 V	60	—	—	mA
Anode driver low output current 3	I_{ELL3}	OUT1 to OUT128	V_{DISP} = 8 V V_O = 1 V	500	—	—	μA
V_{DISP} dependence coefficient for anode driver ON current *1	ΔI_{ELON1}	OUT1 to OUT128	V_{DISP} = 17 to 30 V V_{EL} = V_O = 15 V R-ADJ = 30 kΩ Current adjustment range = 100%	–2.5	0	2.5	%/V
V_O dependence coefficient for anode driver ON current *2	ΔI_{ELON2}	OUT1 to OUT128	V_{DISP} = 24 V V_{EL} = 15 V V_O = 8 to 21 V R-ADJ = 30 kΩ Current adjustment range = 100%	–2.5	0	2.5	%/V
Temperature coefficient for anode driver ON current	ΔI_{ELON3}	OUT1 to OUT128	V_{DISP} = 24 V V_{EL} = V_O = 15 V R-ADJ = 30 kΩ Current adjustment range = 100%	–0.1	0	0.1	%/°C
Relative error between dots (excluding adjoining dots) for anode driver ON current	ΔI_{ELON4}	OUT1 to OUT128	V_{DISP} = 24 V V_{EL} = V_O = 15 V R-ADJ = 30 kΩ Current adjustment range = 100% OUT1 to OUT128 = “ON” Inside one chip.	–5	0	5	%
Tilt inside chip for anode driver ON current *3	ΔI_{ELON5}	OUT1 to OUT4 OUT63 to OUT66 OUT125 to OUT128	V_{DISP} = 24 V V_{EL} = V_O = 15 V R-ADJ = 30 kΩ Current adjustment range = 100% OUT1 to OUT128 = “ON” Inside one chip.	–3	0	3	%
Relative error between adjoining dots for anode driver ON current *4	ΔI_{ELON6}	OUT1 to OUT128	V_{DISP} = 24 V V_{EL} = V_O = 15 V R-ADJ = 30 kΩ Current adjustment range = 100% OUT1 to OUT128 = “ON” Inside one chip.	–2	0	2	%

*1 V_{DISP} dependence coefficient depends on the following conditions:
$I(V_{DISP} = nV)$: Anode driver ON current at $V_{DISP} = nV$.
$\Delta I_{ELON1} = [\ I(V_{DISP} = nV) - I(V_{DISP} = (n+1)V)\ ]/\{\ [\ I(V_{DISP} = nV) + I(V_{DISP} = (n+1)V)\ ]/2\ \} \times 100$

*2 V_O dependence coefficient depends on the following conditions:
$I(V_O = nV)$: Anode driver ON current at $V_O = nV$.
$\Delta I_{ELON2} = [\ I(V_O = nV) - I(V_O = (n-1)V)\ ]/\{\ [\ I(V_O = nV) + I(V_O = (n-1)V)\ ]/2\ \} \times 100$

*3 Tilt inside chip depends on the following conditions:
Cave: Average output current of OUT1 to 4, OUT63 to 66, and OUT125 to 128.
Lave: Average output current of OUT1 to 4.
Rave: Average output current of OUT125 to 128.
ΔI_{ELON5} = (Lave – Cave)/Cave
ΔI_{ELON5} = (Rave – Cave)/Cave

*4 A relative error between adjoining dots depends on the following condition:
$(I_{ELON(N+1)} - I_{ELON(N)})I_{ELON(N)}$

Supply Current

V_{DD} = 3.0 to 5.5 V, V_{DISP} = 8 to 30 V, Tjop = –40 to +125°C

Parameter	Symbol	Applicable Pins	Condition	Min.	Typ.	Max.	Unit
Supply current	I_{DISP1}	V_{DISP}	V_{DISP} = 30 V V_{EL} = 15 V A-CLK = 5 MHz R-ADJ = 30 kΩ Current adjustment range = 100% Output = open PWM data = other than “0”	—	—	5.0	mA
	I_{DISP2}	V_{DISP}	V_{DD} = 0 V V_{DISP} = 30 V V_{EL} = 15 V R-ADJ = 30 kΩ Output = open	—	—	300	μA
	I_{DD1}	V_{DD}	V_{DD} = 5.5 V D-CLK = 5 MHz DATA = “1010.....10”	—	—	18	mA
		V_{DD}	V_{DD} = 5.5 V D-CLK, A-CLK = 5 MHz DATA = “1010.....10”	—	—	20	mA
		V_{DD}	V_{DD} = 5.5 V A-CLK = 5 MHz DATA = “1010.....10”	—	—	5	mA
	I_{DD2}	V_{DD}	V_{DD} = 5.5 V, D-CLK = halted $\overline{RESET}$ = 0 V All the other inputs are also 0 V.	—	—	100	μA

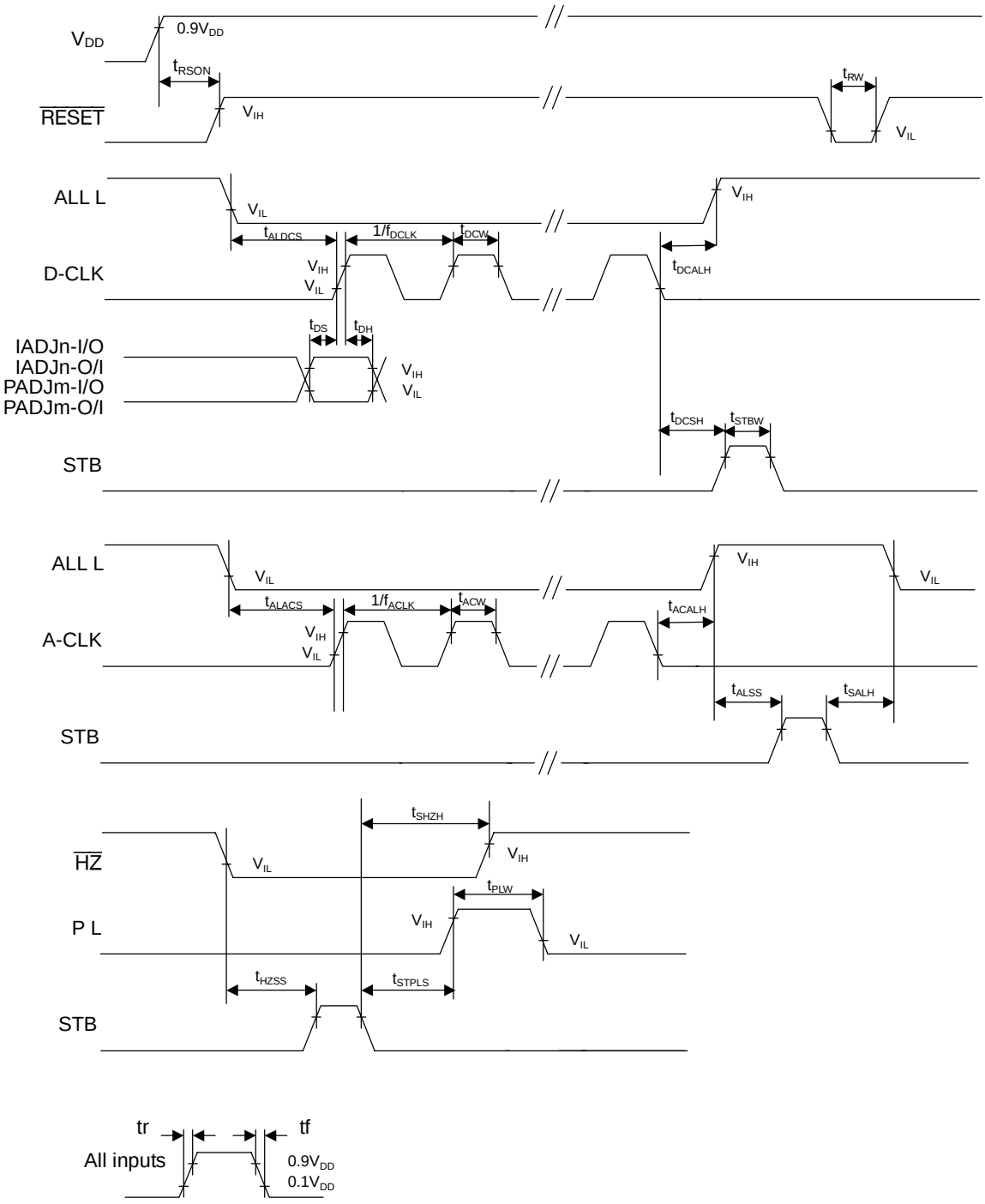
AC Characteristics

V_{DD} = 3.0 to 5.5 V, V_{DISP} = 8 to 30 V, Tjop = –40 to +125°C

Parameter	Symbol	Applicable pins	Condition	Min.	Typ.	Max.	Unit
D-CLK frequency	f_{DCLK}	D-CLK	—	0		5.0	MHz
D-CLK pulse width	t_{DCW}	D-CLK	—	50	—	—	ns
A-CLK frequency	f_{ACLK}	A-CLK	—	0		5.0	MHz
A-CLK pulse width	t_{ACW}	A-CLK	—	50	—	—	ns
DATA→D-CLK setup time	t_{DS}	D-CLK IADJn-I PADJm-I	—	50	—	—	ns
D-CLK→DATA hold time	t_{DH}	D-CLK IADJn-I PADJm-I	—	50	—	—	ns
STB pulse width	t_{STBW}	STB	—	50	—	—	ns
ALL L→STB setup time	t_{ALSS}	ALL L, STB	—	100	—	—	ns
STB→ALL L hold time	t_{SALH}	ALL L, STB	—	100	—	—	ns
$\overline{HZ}$→STB setup time	t_{HZSS}	$\overline{HZ}$, STB	—	100	—	—	ns
STB→$\overline{HZ}$ hold time	t_{SHZH}	$\overline{HZ}$, STB	—	100	—	—	ns
ALL L→D-CLK setup time	t_{ALDCS}	ALL L, D-CLK	—	100	—	—	ns
D-CLK→ALL L hold time	t_{DCALH}	ALL L, D-CLK	—	100	—	—	ns
ALL L→A-CLK setup time	t_{ALACS}	ALL L, A-CLK	—	100	—	—	ns
A-CLK→ALL L hold time	t_{ACALH}	ALL L, A-CLK	—	100	—	—	ns
P L pulse width	t_{PLW}	P L	—	100	—	—	ns
P L→ALL L setup time	t_{PLALS}	ALL L, P L	—	100	—	—	ns
STB→P L setup time	t_{STPLS}	P L, STB	—	100	—	—	ns
D-CLK→STB hold time	t_{DCSH}	D-CLK STB	—	50	—	—	ns
$\overline{RESET}$ pulse width	t_{RW}	$\overline{RESET}$	—	100	—	—	ns
$\overline{RESET}$ execution time	t_{RSON}	$\overline{RESET}$	—	250	—	—	ns
A-CLK → output delay time	$t_{D}r$ $t_{D}f$	$\overline{HZ}$, ALL H ALL L, P L A-CLK OUT1 to 128	—	—	—	2.0	μs
Input signal rise/fall time	tr tf	All inputs	—	—	—	500	ns

TIMING DIAGRAM

Data Input



DESCRIPTION OF OPERATION

Initial Settings

Following initial settings can be made by setting the $\overline{\text{RESET}}$ pin to low.

- The shift register outputs and latch circuit outputs become all low.
- Anode drive signal output pins (OUT1 to 128) become high impedance.

Anode Output Current Adjustment

1. Output current adjustment for entire output
   Output current of anode drive signal output pins (OUT1 to OUT128) can be adjusted, as a batch adjustment for all the output pins. Output current is adjusted by varying the value of the resistor connected between the R-ADJ pin and GND. Output current (typ.) at the time that the V_{EL}SEL pin is "high" and "low" is given by the following expressions:

   [When the V_{EL}SEL pin is "high"]
   Output current (typ.) = V_{EL} pin voltage ÷ R-ADJ resistance value

   [When the V_{EL}SEL pin is "low"]
   Output current (typ.) = 5 V ÷ R-ADJ resistance value

2. Output current adjustment for each output
   Output current of anode drive signal output pins (OUT1 to OUT128) can be adjusted for each output pin. Adjustment of each output current is made by bit data IADJ0-n and IADJ1-n. This 2-bit data is written in the shift register at the rising edge of the D-CLK signal and latched at the rising edge of the STB signal.

   Relation between IADJ0-n, IADJ1-n, and output current is shown below.

IADJ1-n	IADJ0-n	Current adjustment range
0	0	0%
0	1	33%
1	0	66%
1	1	100%

3. Output pulse width adjustment
   Output pulse width of anode drive signal output pins (OUT1 to OUT128) can be adjusted for each output pin. Adjustment of each output pulse width is made by 4-bit data PADJ0-n, PADJ1-n, PADJ2-n, and PADJ3-n. This 4-bit data is written in the shift register at the rising edge of the D-CLK signal and latched at the rising edge of the STB signal. An anode drive signal output pin is configured as constant current output until the number of A-CLK pulses becomes equal to the output data of 4 bits of PADJ0-n, PADJ1-n, PADJ2-n, and PADJ3-n. When they have matched, the output becomes low or high impedance at the rising edge of the A-CLK pulse that has matched the output data of PADJ0-n, PADJ1-n, PADJ2-n, and PADJ3-n.

   Relation between PADJ0-n, PADJ1-n, PADJ2-n, and PADJ3-n and output pulse width is shown below.

PADJ3-n	PADJ2-n	PADJ1-n	PADJ0-n	Output pulse width
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Setting of Output Condition When Dot is OFF

The output condition when dot is OFF is set with the combination of $\overline{HZ}$, ALL L, OFF HZ, A0 HZ, and P L signals. See “3. Operation of Output Section” in “FUNCTION TABLE” and the section of “OUTPUT WAVEFORMS”.

Power Applying Sequence

It is possible to apply power first to V_{DD} or V_{DISP}. When power is applied to V_{DISP}, and V_{DD} is 2.5 V or less, following operating states occur.

- Constant current source circuit does not operate.
- Anode drive signal output pins (OUT1 to 128) become high impedance.

Make the $\overline{RESET}$ pin high at least 250 ns after applying power to V_{DD}.
(Refer to $\overline{RESET}$ execution time in AC Characteristics.)

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL9361-01	Dec. 12, 2002	–	–	Preliminary edition 1

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