PEDL9352-01
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OKI Semiconductor

ML9352 Preliminary

128-Channel Organic EL Driver with Built-in RAM

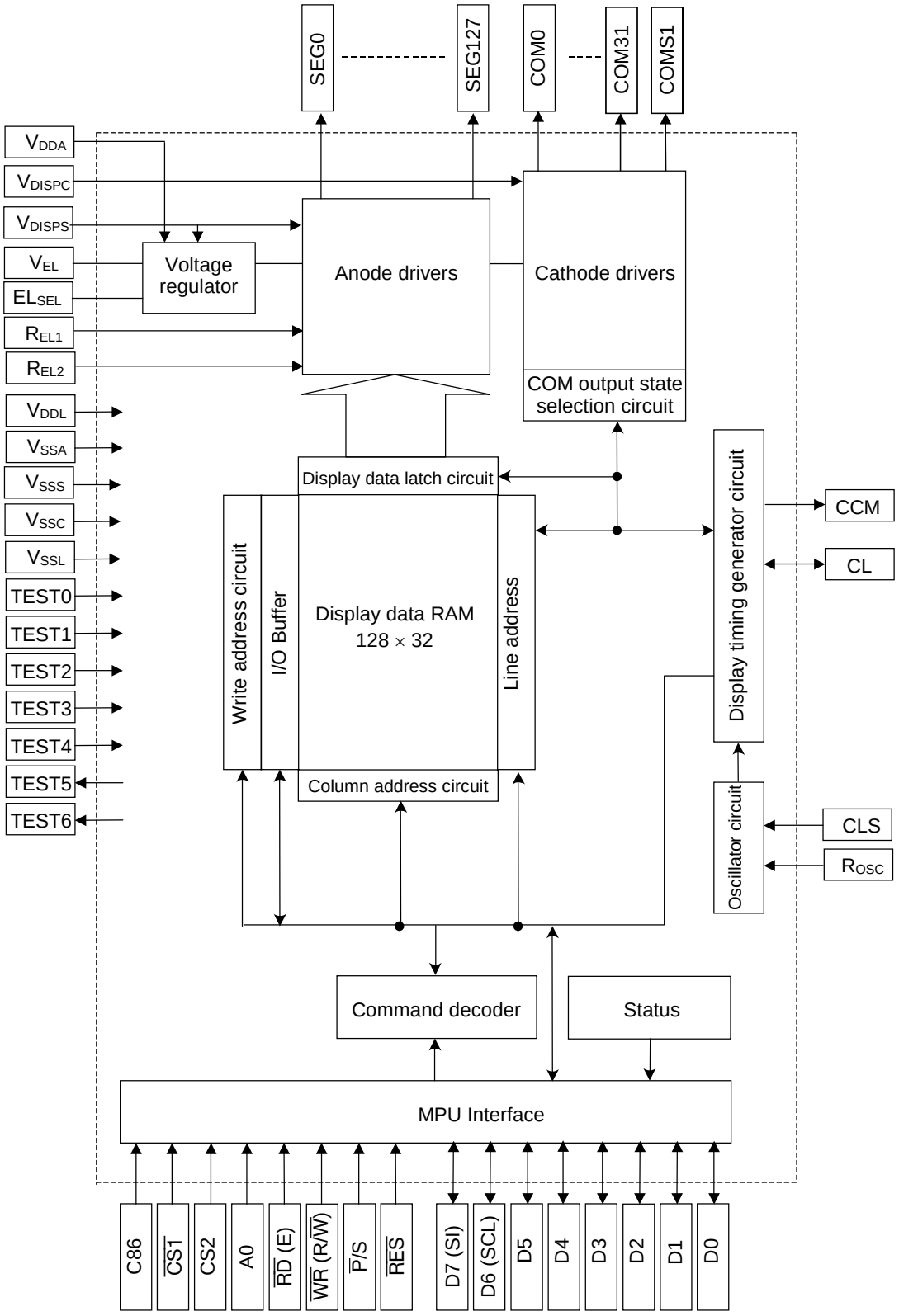
GENERAL DESCRIPTION

The ML9352 is an LSI for dot matrix graphic organic EL devices carrying out bit map display. This LSI can drive a dot matrix graphic organic EL display panel under the control of microcomputer. Since all the functions necessary for driving a bit map type organic EL device are incorporated in a single chip, using the ML9352 makes it possible to realize a bit map type dot matrix graphic organic EL display system with only a few chips.
Since the bit map method in which one bit of display RAM data turns ON or OFF one dot in the display panel, it is possible to carry out displays with a high degree of freedom such as Chinese character displays, etc. With one chip, it is possible to construct a graphic display system with a maximum of 128 × 32 dots.
Since the organic EL drive voltage of the ML9352 can range as high as 30 V, the ML9352 is suited to drive on-vehicle panels that require high luminance and panels used in audio equipment.

FEATURES

- Direct display of the RAM data using the bit map method
  Display RAM data “1” ... Dot is displayed
  Display RAM data “0” ... Dot is not displayed
- Display RAM capacity
  ML9352: 32 × 128 = 4096 dots
- Organic EL Drive circuits
  33 cathode outputs, 128 anode outputs
- Microcomputer interface: Can select an 8-bit parallel or serial interface
- Built-in oscillator circuit (Internal oscillator circuit/external clock input selectable)
- A variety of commands
  Read/write of display data, display ON/OFF, normal/reverse display, all dots ON, write address setting, scroll start line setting, fixed display line number setting, anode pulse width adjustment, etc.
- Power supply voltage
  Logic power supply: $V_{DDA} = V_{DDL}$ = 2.7 to 5.5 V
  Organic EL Drive voltage: V_{DISPS} = 18 to 30 V, V_{DISPC} = 18 to 30 V
- Package: Bare chip

BLOCK DIAGRAM



PIN DESCRIPTION

Function	Pin name	Number of pins	I/O	Description
MPU Interface	D0 to D7	8	I/O	This is an 8-bit bi-directional data bus that can be connected to an 8-bit or 16-bit standard MPU data bus. When a serial interface is selected ($\overline{P}$/S = "H"): D7: Serial data input pin (SI) D6: Serial clock input pin (SCL) In this case, D0 to D5 will be in the Hi-Z state. D0 to D7 will all be in the Hi-Z state when the chip select is in the inactive state.
	A0	1	I	Normally, the lowest bit of the MPU address bus is connected. Set this pin to "H" when writing or reading display data, and set to "L" when entering any other control command or writing any other control data.
	$\overline{RES}$	1	I	Initial setting is made by making $\overline{RES}$ = "L". The reset operation is made during the active level of the RES signal.
	$\overline{CS1}$ CS2	2	I	These are the chip select signals. The Chip Select of the LSI becomes active when $\overline{CS1}$ is "L" and also CS2 is "H" and allows the input/output of data or commands.
	$\overline{RD}$ (E)	1	I	The active level of this signal is "L" when connected to an 80-series MPU. This terminal is connected to the $\overline{RD}$ signal of the 80-series MPU, and the data bus of the ML9352 goes into the output state when this signal is "L". The active level of this signal is "H" when connected to a 68-series MPU. This pin will be the Enable clock input pin when connected to a 68-series MPU.
	$\overline{WR}$ (R/$\overline{W}$)	1	I	The active level of this signal is "L" when connected to an 80-series MPU. This terminal is connected to the $\overline{WR}$ signal of the 80-series MPU. The data on the data bus is latched into the ML9352 at the rising edge of the $\overline{WR}$ signal. When connected to a 68-series MPU, this pin becomes the input pin for the Read/Write control signal. R/$\overline{W}$ = "H": Read, R/$\overline{W}$ = "L": Write
	C86	1	I	This is the pin for selecting the MPU interface type. (This pin has a pull-down resistor.) C86 = "H": 68-Series MPU interface C86 = "L": 80-Series MPU interface

<table>
<tr><th>Function</th><th>Pin name</th><th>Number of pins</th><th>I/O</th><th>Description</th></tr>
<tr><td>MPU Interface</td><td>$\overline{P}$/S</td><td>1</td><td>I</td><td>This is the pin for selecting parallel data input or serial data input. (This pin has a pull-down resistor.)
$\overline{P}$/S= “H”: Serial data Input
$\overline{P}$/S= “L”: Parallel data input
The pins of the LSI have the following functions depending on the state of $\overline{P}$/S input.
<table>
<tr><th>$\overline{P}$/S</th><th>Data/command</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>“H”</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td rowspan="2">SCL (D6)</td></tr>
<tr><td>“L”</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td></tr>
</table>
When $\overline{P}$/S is “H”, D0 to D5 will go into the Hi-Z state. In this condition, the data on the lines D0 to D5 can be “H”, “L” or open. The pins $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) should be tied to either the “H” level or the “L” level. During serial data input, it is not possible to read the display data in the RAM.</td></tr>
<tr><td rowspan="2">Oscillator circuit</td><td>CLS</td><td>1</td><td>I</td><td>This is the pin for selecting whether to enable or disable the internal oscillator circuit for the display clock. (This pin has a pull-down resistor.)
CLS = “L”: The internal oscillator circuit is enabled.
CLS = “H”: The internal oscillator circuit is disabled (External input).
When CLS = “H”, the display clock is input at the pin CL.</td></tr>
<tr><td>R_{OSC}</td><td>1</td><td>I</td><td>This is the pin for adjusting the frequency of the internal oscillator circuit. Connecting the pin to V_{SSL} allows the oscillation frequency to be lowered by 16%. Normally, leave this pin open.</td></tr>
<tr><td rowspan="2">Display timing generator circuit</td><td>CL</td><td>1</td><td>I/O</td><td>This is the display clock input/output pin.
The function of this pin will be as follows depending on the state of and CLS signal.
<table>
<tr><th>CLS</th><th>CL</th></tr>
<tr><td>“L”</td><td>Output</td></tr>
<tr><td>“H”</td><td>Input</td></tr>
</table></td></tr>
<tr><td>CCM</td><td>1</td><td>O</td><td>Internal cathode timing output pin</td></tr>
<tr><td rowspan="12">Power supply circuit</td><td>V_{DDA}</td><td>1</td><td>—</td><td>Power supply pin for the analog circuit.*1</td></tr>
<tr><td>V_{SSA}</td><td>1</td><td>—</td><td>Ground pin for the analog circuit.*2</td></tr>
<tr><td>V_{DDL}</td><td>1</td><td>—</td><td>Power supply pin for the logic circuit.*1</td></tr>
<tr><td>V_{SSL}</td><td>1</td><td>—</td><td>Ground pin for the logic circuit.*2</td></tr>
<tr><td>V_{DISPS}</td><td>3</td><td>—</td><td>Power supply pin for the organic EL anode drive circuit.</td></tr>
<tr><td>V_{SSS}</td><td>3</td><td>—</td><td>Ground pin for the organic EL anode drive circuit.*2</td></tr>
<tr><td>V_{DISPC}</td><td>2</td><td>—</td><td>Power supply pin for the organic EL cathode drive circuit.</td></tr>
<tr><td>V_{SSC}</td><td>2</td><td>—</td><td>Ground pin for the organic EL cathode drive circuit.*2</td></tr>
<tr><td>V_{EL}</td><td>1</td><td>I</td><td>Input pin for the anode driver output current adjusting voltage.
An input voltage is effective when EL_{SEL} = “H”.</td></tr>
<tr><td>EL_{SEL}</td><td>1</td><td>I</td><td>Pin that selects anode driver output current adjusting voltage. (This pin has a pull-down resistor.)
When EL_{SEL} = “L”, the internally regulated voltage is selected; when EL_{SEL} = “H”, the V_{EL} pin voltage is selected.</td></tr>
<tr><td>$R_{EL1,2}$</td><td>2</td><td>I</td><td>Anode driver output current adjusting external resistor connection pins.</td></tr>
</table>

*1 Make V_{DDA} and V_{DDL} have the same potential.

*2 Make V_{SSA}, V_{SSL}, V_{SSS}, and V_{SSC} have the same potential.

Function	Pin name	Number of pins	I/O	Description
Organic EL drive output	SEG0 to SEG127	128	O	Anode driver output pins
	COM0 to COM31	32	O	Output pins for the cathode driver outputs for dot display
	COMS1	1	O	Output pins for the cathode driver outputs for static display
Test pin	TEST0	1	I	These pins are used to test the IC chip. Leave these pins open during normal operation.
	TEST1	1	I	
	TEST2	1	I	
	TEST3	1	I	Input pin to control the TEST5 pin (internally regulated voltage monitor pin). TEST3 has a pull-down resistor. When TEST3 is “H”, it outputs an internally regulated voltage (Vreg), and when “L” it will go into the Hi-Z state.
	TEST4	1	I	This pin is used to test the IC chip. Leave this pin open during normal operation.
	TEST5	1	O	Internally regulated voltage monitor pin
	TEST6	1	O	This pin is used to test the IC chip. Leave this pin open during normal operation.

FUNCTIONAL DESCRIPTION

MPU Interface

- Selection of interface type

The ML9352 carries out data transfer using either the 8-bit bi-directional data bus (D7 to D0) or the serial data input line (SI). Either the 8-bit parallel data input or serial data input can be selected as shown in Table 1 by setting the $\overline{P}$/S pin to the "H" or the "L" level.

Table 1

$\overline{P}$/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
L: Parallel input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
H: Serial input	$\overline{CS1}$	CS2	A0	—	—	—	SI	SCL	(HZ)

A dash (—) indicates that the pin can be tied to the "H" or the "L" level.

- Parallel interface

When the parallel interface is selected, ($\overline{P}$/S = "L"), it is possible to connect this LSI directly to the MPU bus of either an 80-series MPU or a 68-series MPU as shown in Table 2 depending on whether the pin C86 is set to "H" or "L".

Table 2

C86	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
H	H: 68-Series MPU bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D7 to D0
L	L: 80-Series MPU bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

The data bus signals are identified as shown in Table 3 below depending on the combination of the signals A0, $\overline{RD}$(E), and $\overline{WR}$(R/$\overline{W}$) of Table 2.

Table 3

	Common	68-Series	80-Series	
	A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$
Display data read	1	1	0	1
Display data write	1	0	1	0
Status read	0	1	0	1
Control data write (command)	0	0	1	0

Serial Interface

When the serial interface is selected ($\overline{P}$/S = "H"), the serial data input (SI) and the serial clock input (SCL) can be accepted if the chip is in the active state ($\overline{CS1}$ = " L" and CS2 = "H"). The serial interface consists of an 8-bit shift register and a 3-bit counter. The serial data is read in from the serial data input pin in the sequence D7, D6, ... , D0 at the rising edge of the serial clock input, and is converted into the 8-bit paralled data at the rising edge of the 8th serial clock pulse and processed further. The identification of whether the serial data is display data or command is judged based on the A0 input, and the data is treated as display data when A0 is "H" and as command when A0 is "L". The A0 input is read in and identified at the rising edge of the (8 × n) th serial clock pulse after the chip has become active. Figure 1 shows the signal chart of the serial interface. (When the chip is not active, the shift register and the counter are reset to their initial states. No data read out is possible in the case of the serial interface. It is necessary to take sufficient care about wiring termination reflection and external noise in the case of the SCL signal. We recommend verification of operation in an actual unit.)

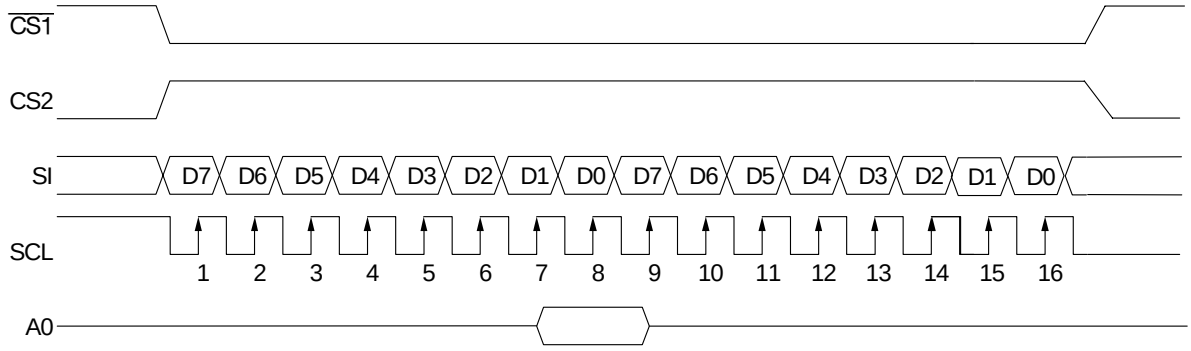


Figure 1

- Chip select

The ML9352 has the two chip select pins $\overline{CS1}$ and CS2, and the MPU interface or the serial interface is enabled only when $\overline{CS1}$ = "L" and CS2 = "H". When the chip select signals are in the inactive state, the D0 to D7 lines will be in the high impedance state and the inputs A0, $\overline{RD}$, and WR will not be effective. When the serial interface has been selected, the shift register and the counter are reset.

- Accessing the display data RAM and the internal registers

Accessing the ML9352 from the MPU side requires merely that the cycle time (t_{CYC}) be satisfied, and high speed data transfer without requiring any wait time is possible. Also, during the data transfer with the MPU, the ML9352 carries out a type of pipeline processing between LSIs via a bus holder associated with the internal data bus. For example, when the MPU writes data in the display data RAM, the data is temporarily stored in the bus holder, and is then written into the display data RAM before the next data read cycle. When the MPU reads out data in the display data RAM, read data is held in the bus holder during the first data read cycle (dummy) and is read out on the system bus from the bus holder during the next data read cycle. There is a restriction on the read sequence of the display data RAM, which is that the read instruction immediately after setting the address does not read out the data of that address, but that data is output as the data of the address specified during the second data read sequence, and hence care should be taken about this during reading. Therefore, always one dummy read is necessary immediately after setting the address or after a write cycle. This relationship is shown in Figures 2(a) and 2(b).

- Data write

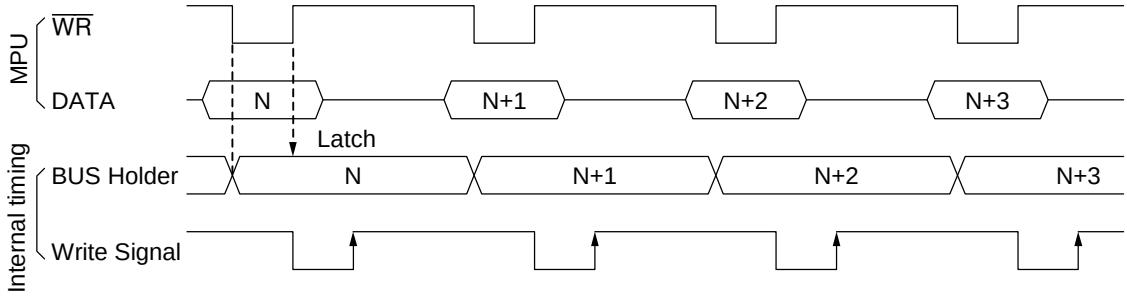


Figure 2(a)

- Data read

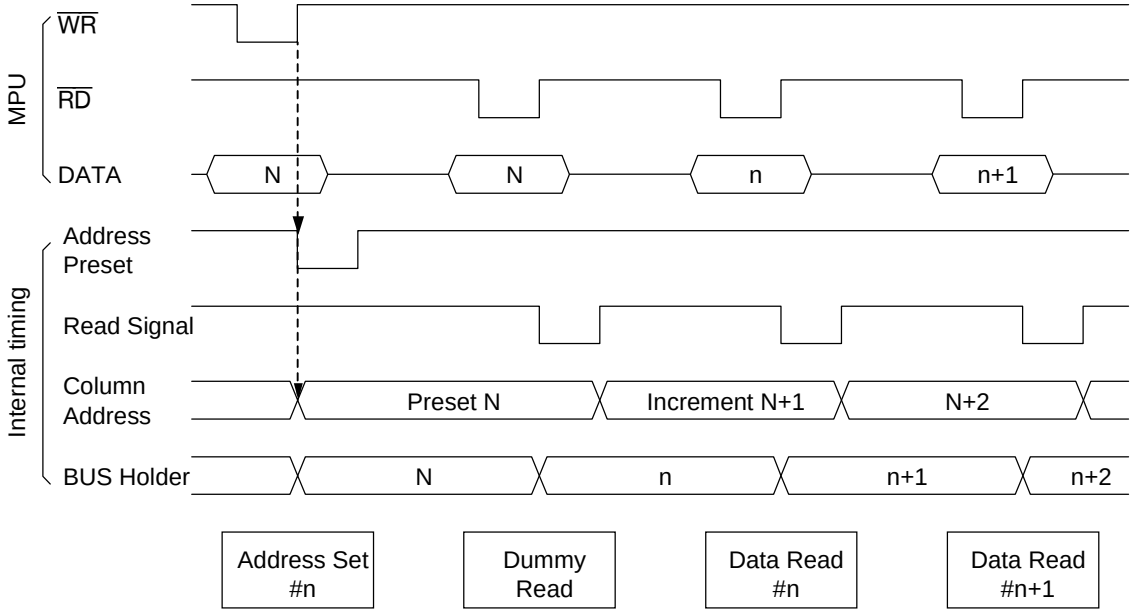


Figure 2(b)

- Busy flag

The busy flag being "1" indicates that the ML9352 is carrying out internal operations, and hence no instruction other than a status read instruction is accepted during this period. The busy flag is output at pin D7 when a status read instruction is executed. If the cycle time (t_{CYC}) is established, there is no need to check this flag before issuing every command and hence the processing performance of the MPU can be increased greatly.

Display data RAM

- Display data RAM

This is the RAM storing the dot data for display and has an organization of 32 × 128 bits. It is possible to access any required bit by specifying the write address and the column address. Since the display data D7 to D0 from the MPU corresponds to the organic EL display in the direction of the common lines as shown in Figure 3. Also, since the display data RAM read/write from the MPU side is carried out via an I/O buffer, it is done independent of the signal read operation for the organic EL drive. Consequently, the display is not affected by flickering, etc., even when the display data RAM is accessed asynchronously during the organic EL display operation.

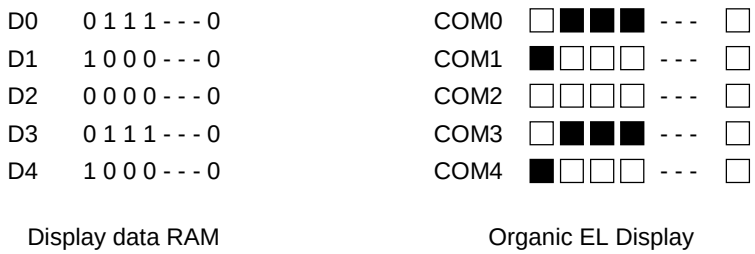


Figure 3

- Write address circuit

The write address of the display data RAM is specified using the write address set command as shown in Figures 4-1 to 4-10. Write display data in units of 8 bits in the direction of the common lines, starting at the specified write address.

- Column address circuit

The column address of the display data RAM is specified using the column address set command as shown in Figures 4-1 to 4-10. Since the specified column address is incremented (by +1) every time a display data read/write command is issued, the MPU can access the display data continuously. Further, the incrementing of the column address is stopped at the column address of 7FH. Since the column address and the write address are independent of each other, it is necessary, for example, to specify separately the new write address and the new column address when changing from column 7FH of write address 07H to column 00H of write address 08H. Also, as is shown in Table 4, it is possible to reverse the correspondence relationship between the display data RAM column address and the SEG output using the ADC command (the anode driver direction select command). This reduces the IC placement restrictions at the time of assembling organic EL modules.

Table 4

	SEG Output	
ADC	SEG0	SEG127
D0 = "0"	0(H) → Column Address → 7F(H)	
D0 = "1"	7F(H) ← Column Address ← 0(H)	

- Line address circuit

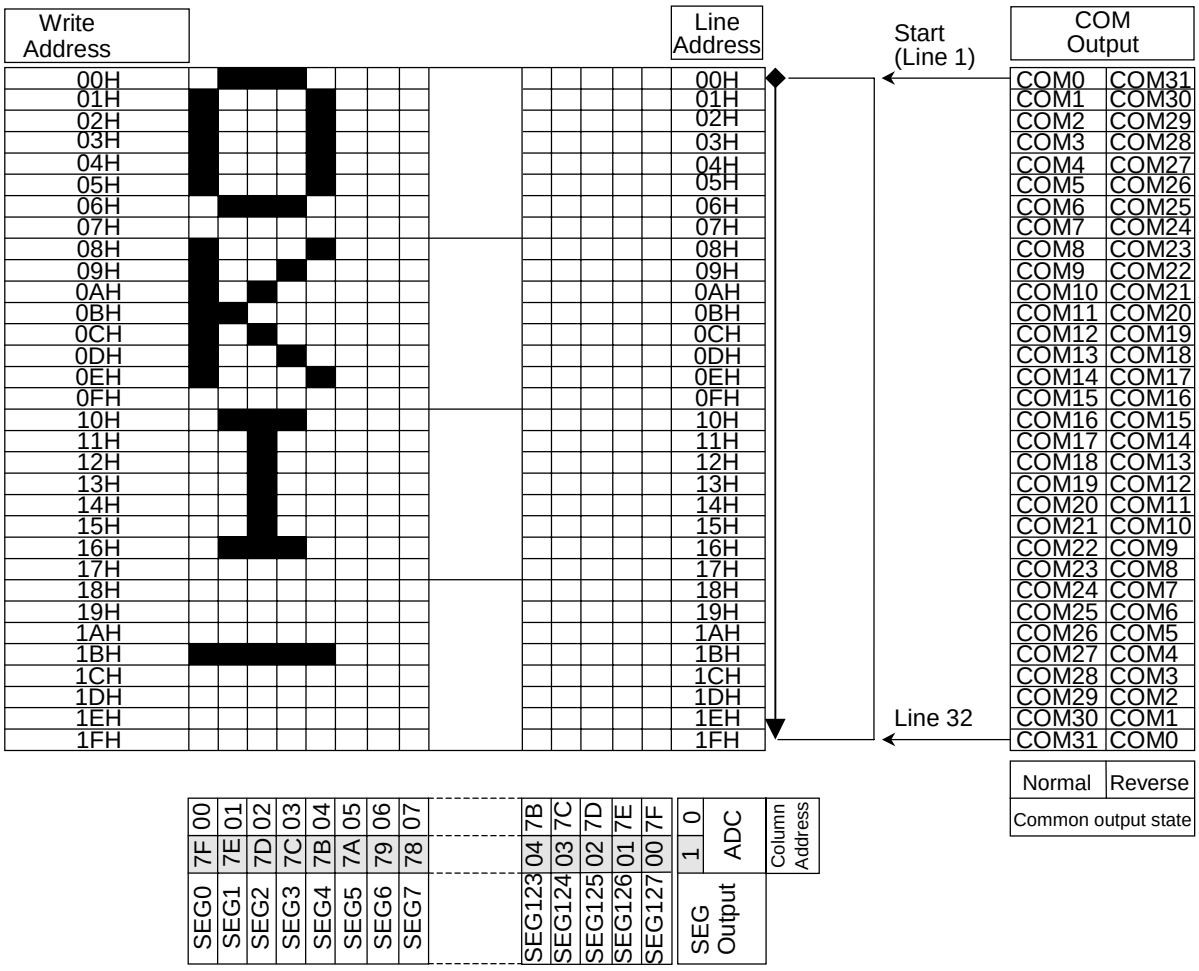
The line address circuit is used for specifying the line address corresponding to the COM output when displaying the contents of the display data RAM as is shown in Figures 4-1 to 4-10. The address line is specified depending on whether or not a fixed display line is set.
The display area when a fixed display line is not set is equivalent to the number of display lines that are specified to the increment direction of the line address from the specified scroll start address.
When the line address exceeds 1FH, it returns to 00H.
It is possible to carry out screen scrolling and page changing by changing the line address using the scroll start line address set command.
The display area when a fixed display line is specified is equivalent to the number of lines which are calculated by subtracting the number of fixed display lines from the number of display lines that are specified to the increment direction of the line address from the scroll start line address.
When the line address exceeds 1FH, it returns to the address next to the fixed display line specified.
It is possible to carry out screen scrolling except the fixed display line by changing the line address using the scroll start line address set command.

- Display data latch circuit

The display data latch circuit is a latch for temporarily storing the data from the display data RAM before being output to the organic EL drive circuits. Since the commands for selecting normal/reverse display and turning the display ON/OFF control the data in this latch, the data in the display data RAM will not be changed.

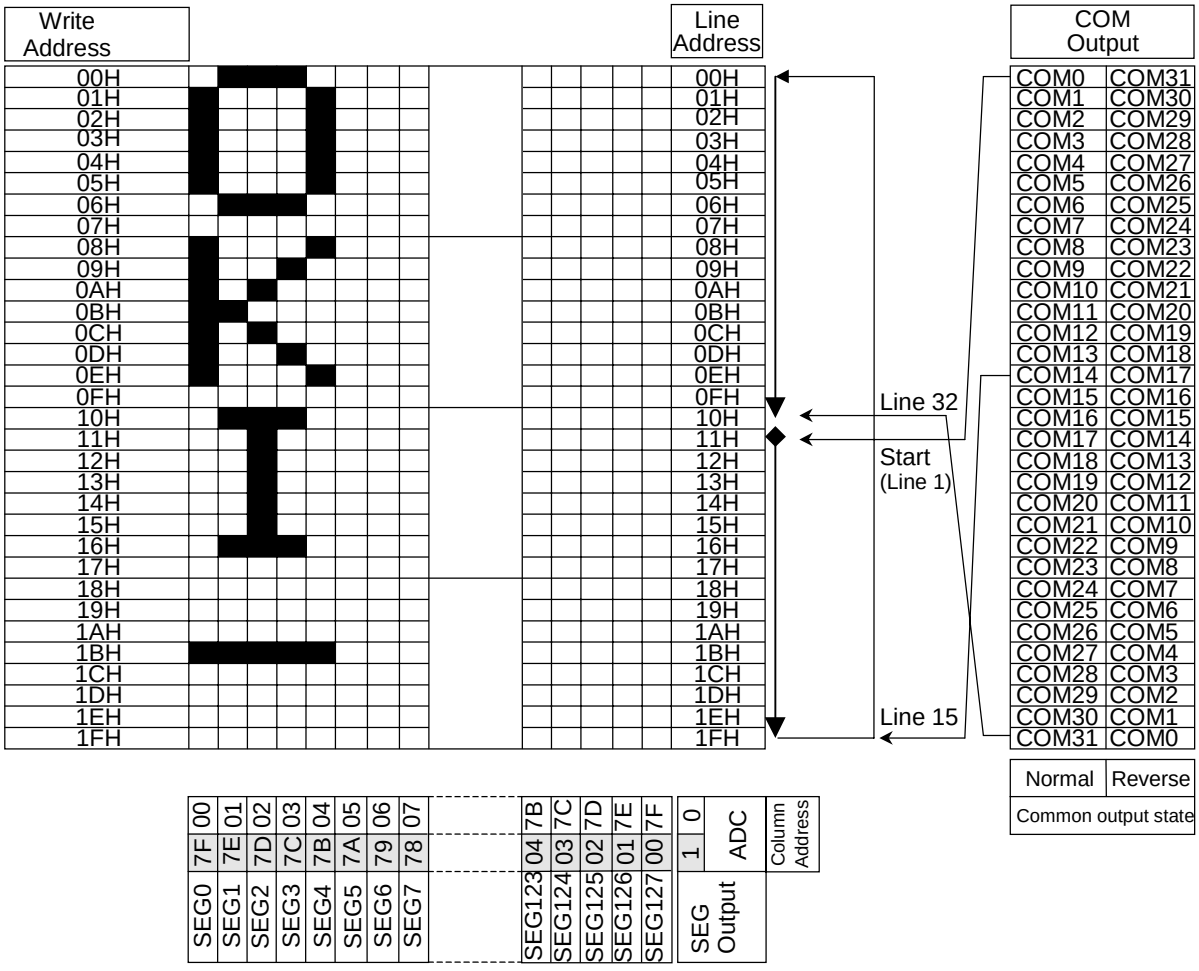
Oscillator circuit

This is an RC oscillator that generates the display clock. The oscillator circuit is effective only when CLS = “L”. The oscillations will be stopped when CLS = “H”, and the display clock has to be input to the CL pin. The oscillations will also be stopped during the power save mode.



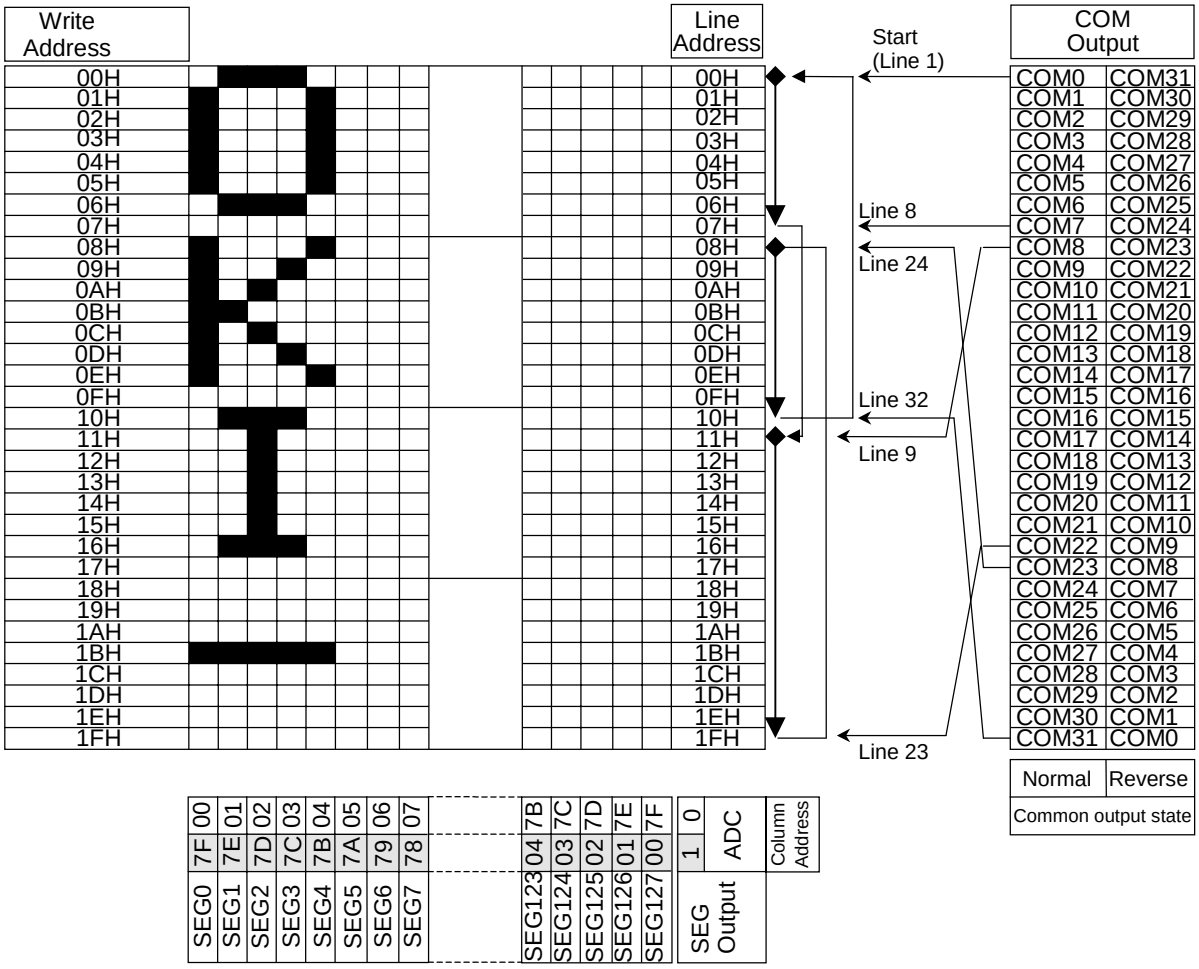
- Number of display lines: 32 lines
- Number of fixed display lines: None
- Scroll start line address: 00H

Figure 4-1



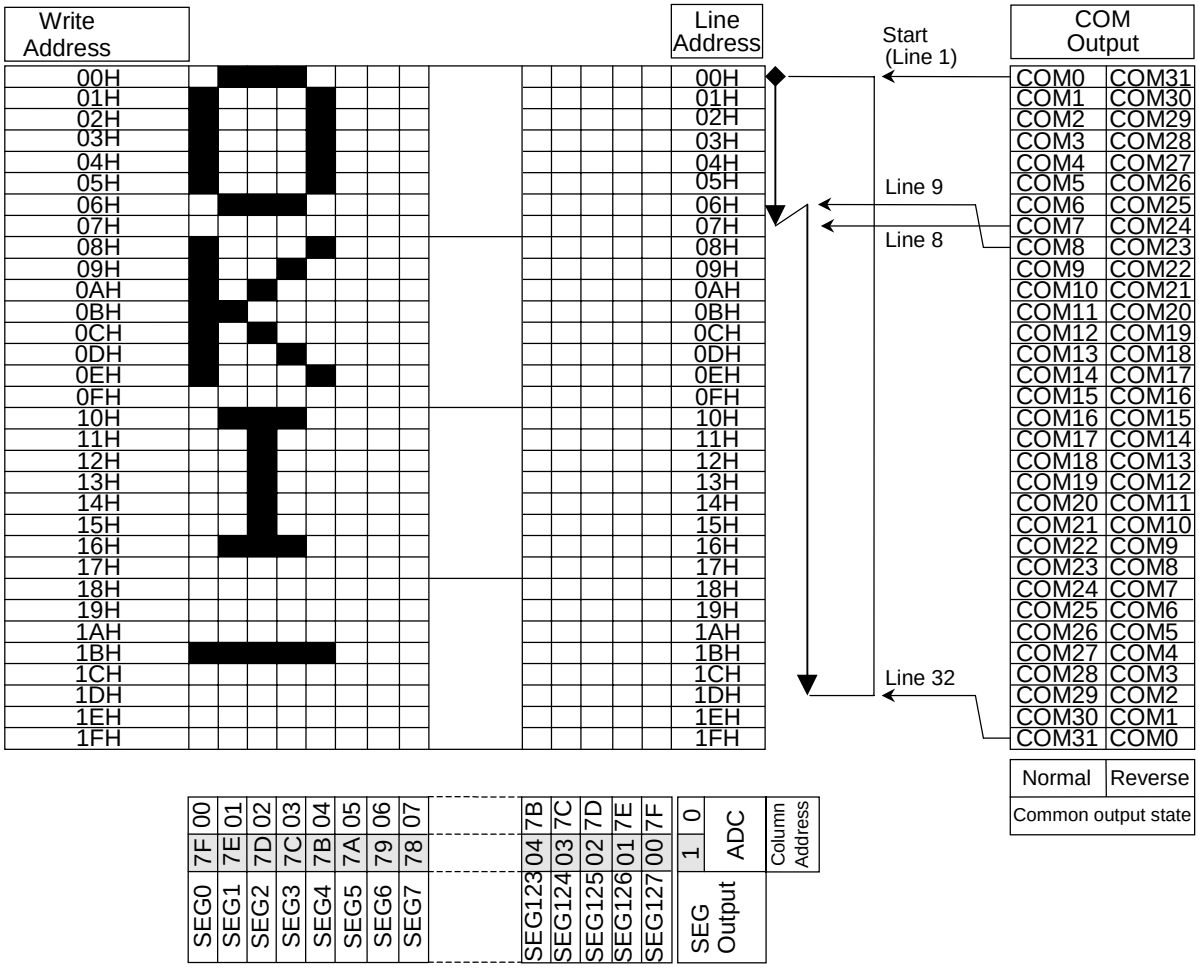
- Number of display lines: 32 lines
- Number of fixed display lines: None
- Scroll start line address: 11H

Figure 4-2



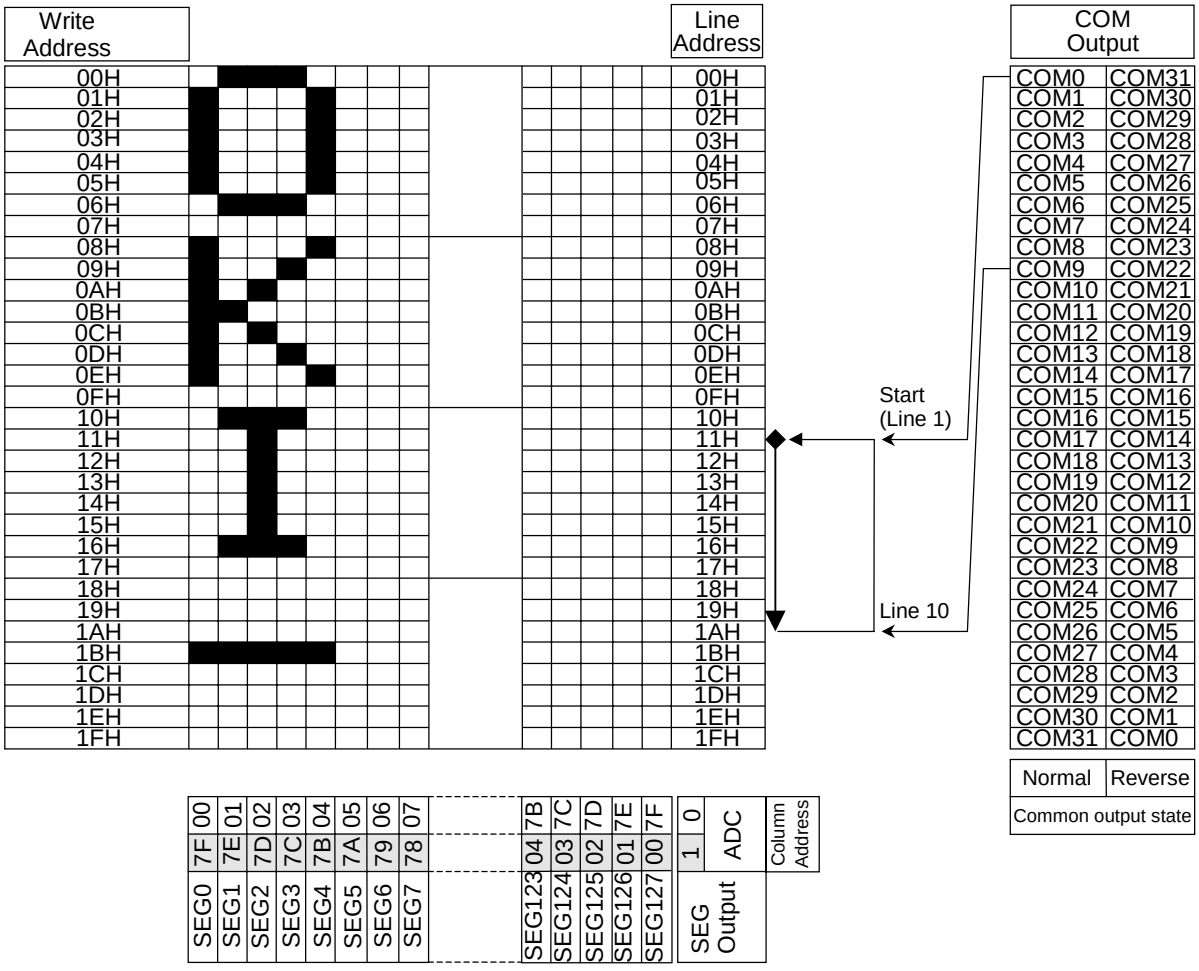
- Number of display lines: 32 lines
- Number of fixed display lines: 00H to 07H
- Scroll start line address: 11H

Figure 4-3



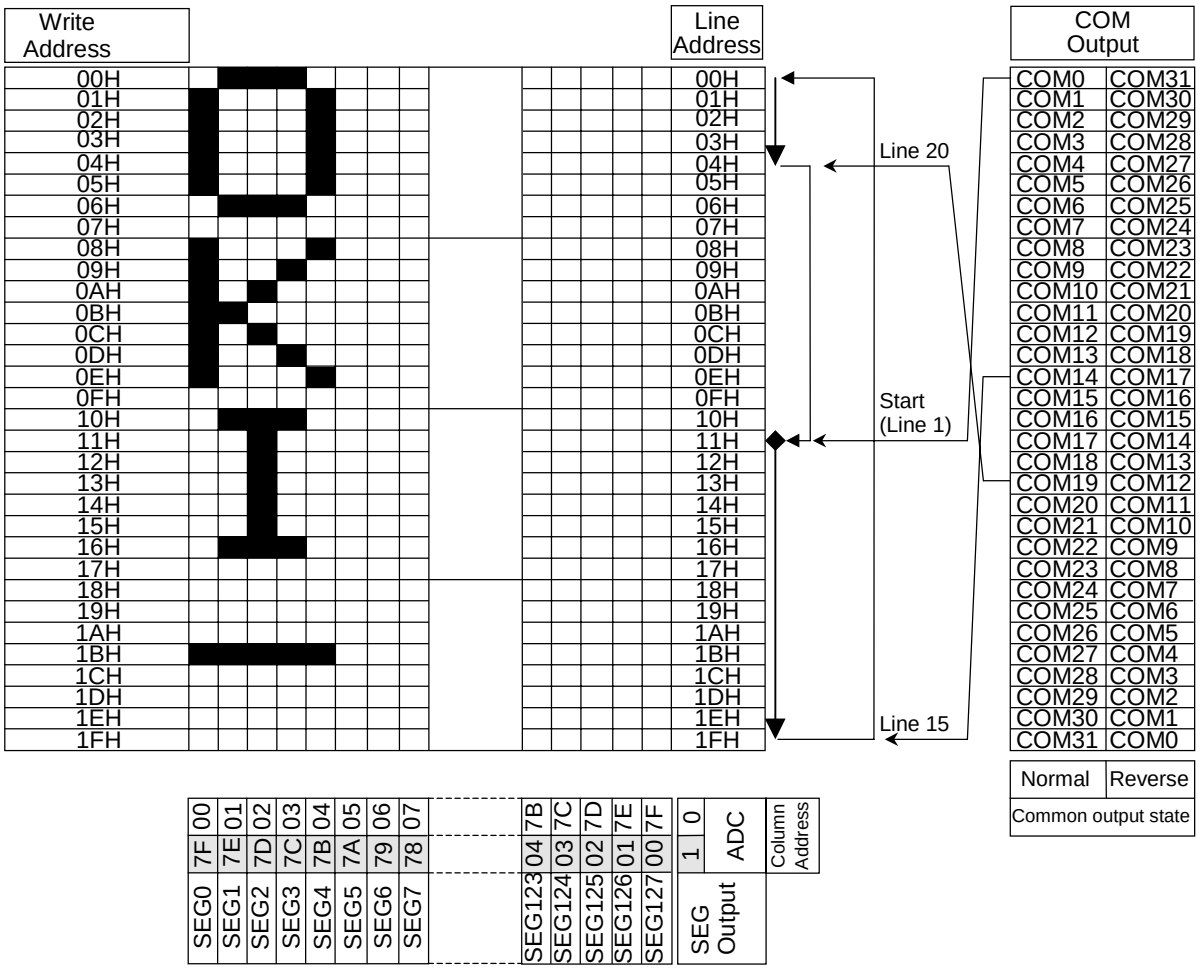
- Number of display lines: 32 lines
- Number of fixed display lines: 00H to 07H
- Scroll start line address: 06H

Figure 4-4



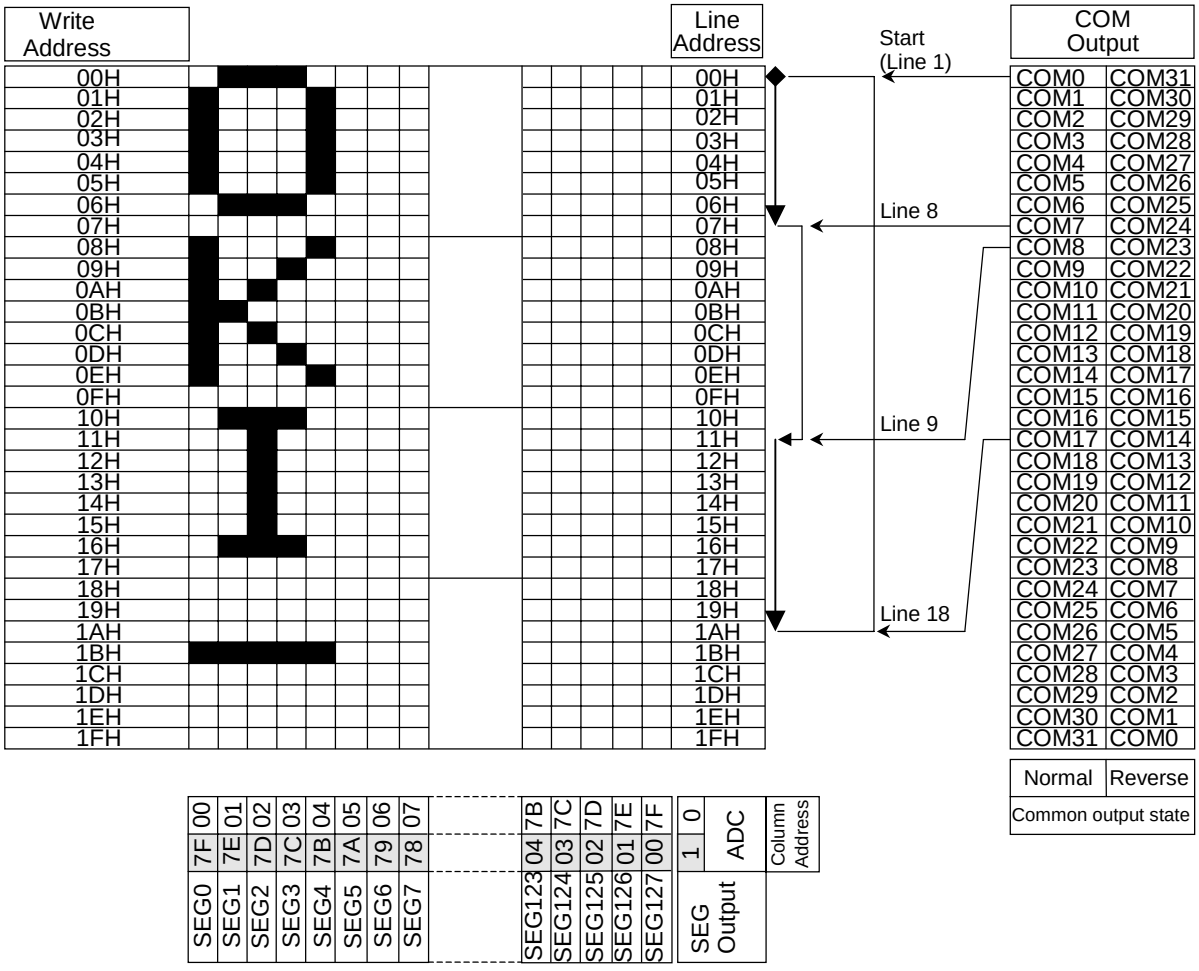
- Number of display lines: 10 lines
- Number of fixed display lines: None
- Scroll start line address: 11H

Figure 4-5



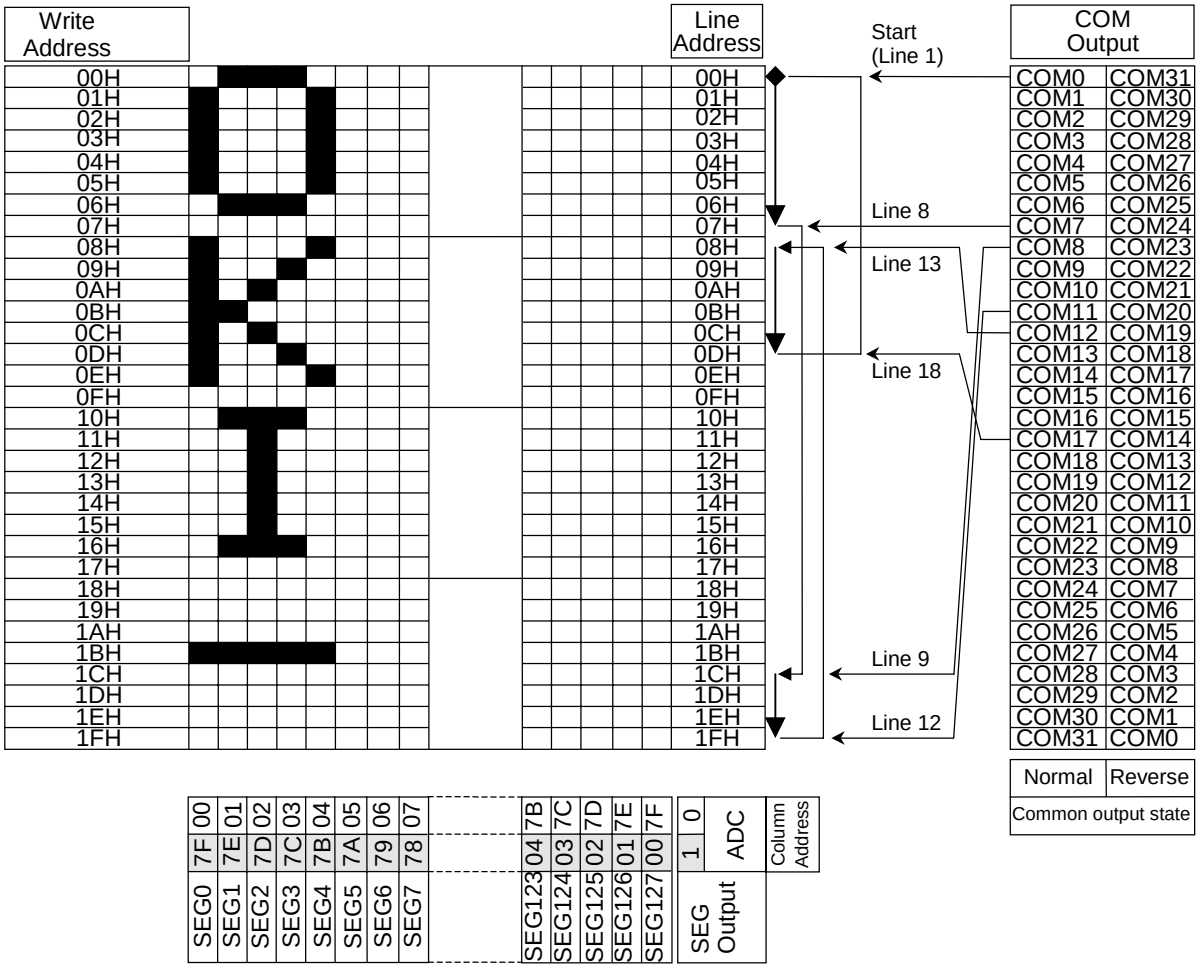
- Number of display lines: 20 lines
- Number of fixed display lines: None
- Scroll start line address: 11H

Figure 4-6



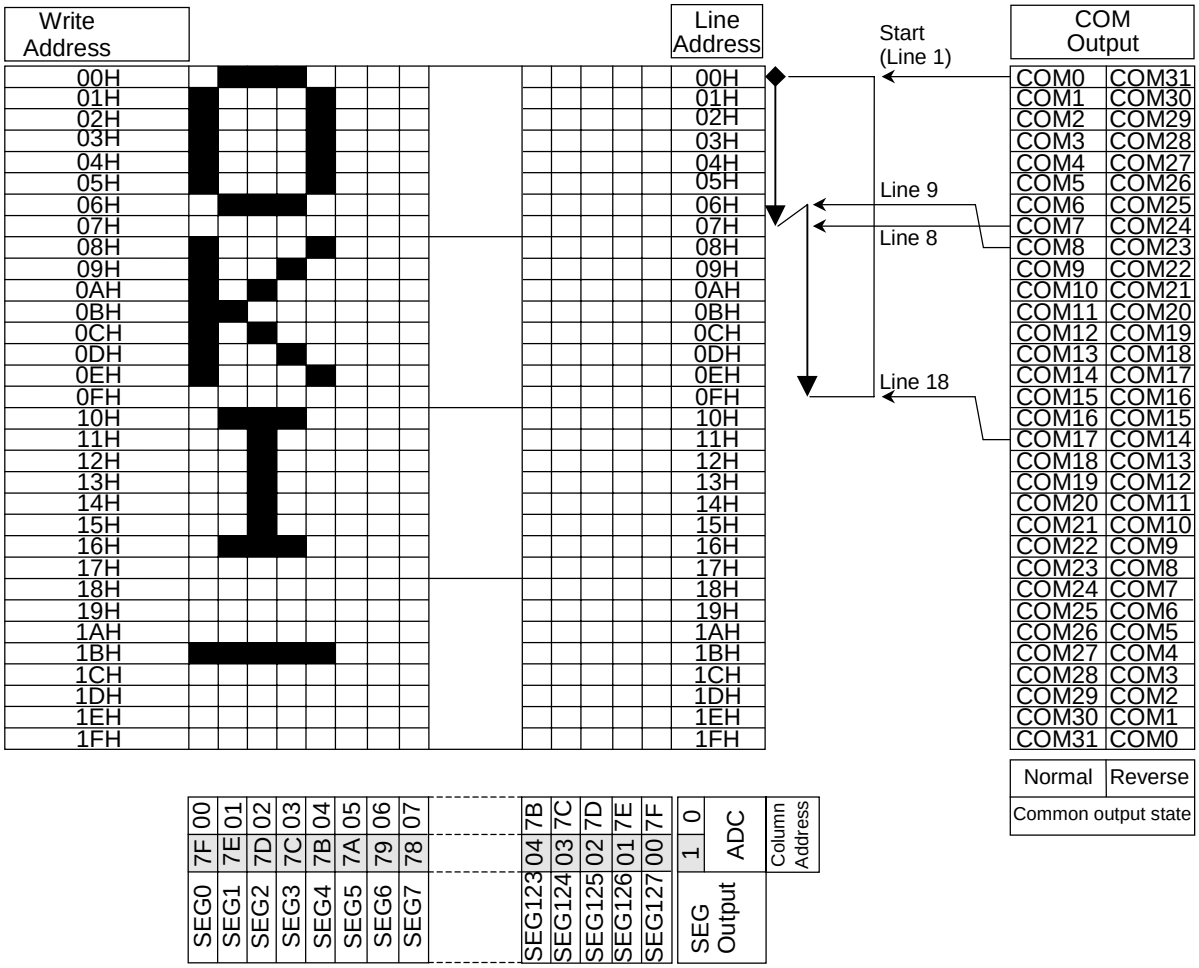
- Number of display lines: 18 lines
- Number of fixed display lines: 00H to 07H
- Scroll start line address: 11H

Figure 4-7



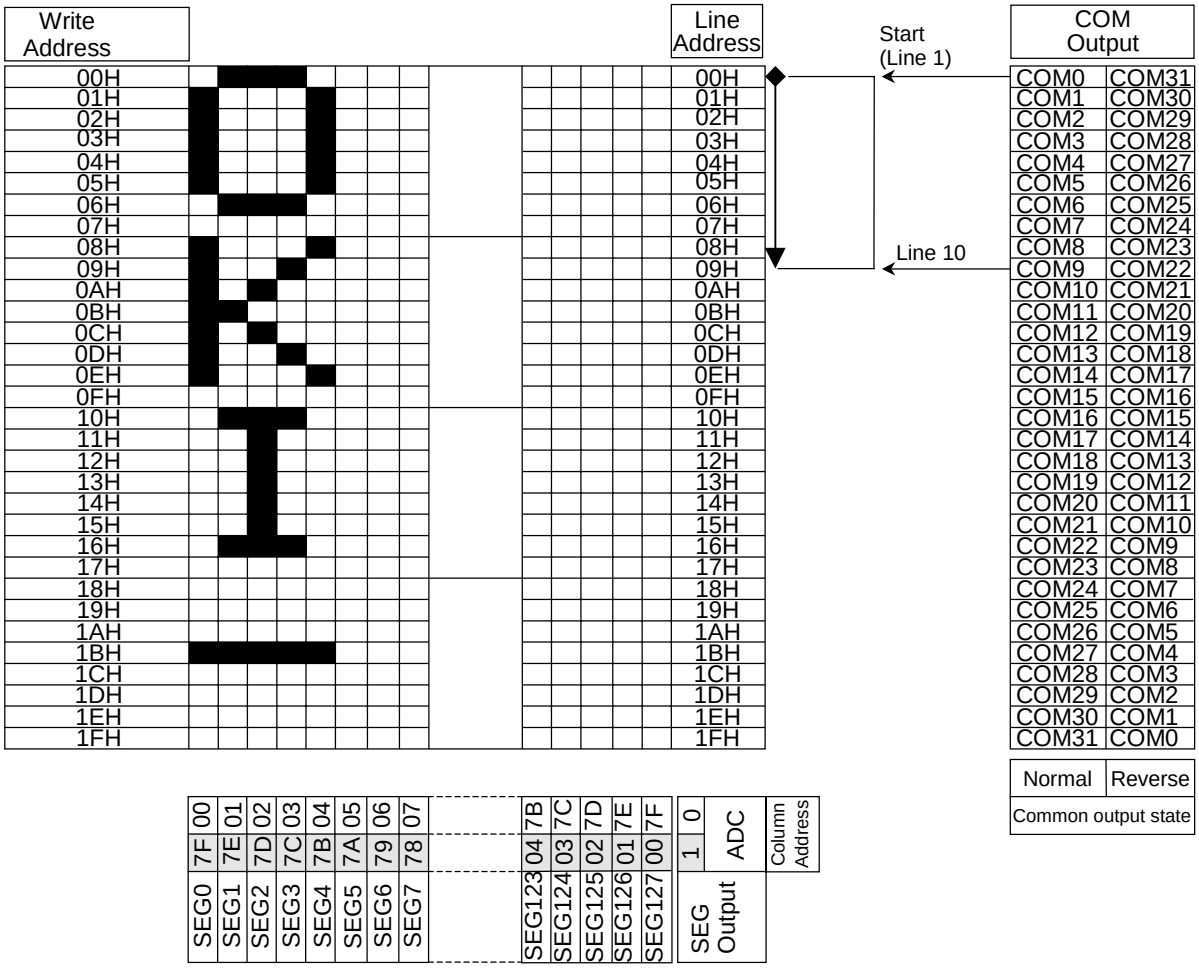
- Number of display lines: 18 lines
- Number of fixed display lines: 00H to 07H
- Scroll start line address: 1CH

Figure 4-8



- Number of display lines: 18 lines
- Number of fixed display lines: 00H to 07H
- Scroll start line address: 06H

Figure 4-9



- Number of display lines: 10 lines
- Number of fixed display lines: 00H to 0FH
- Scroll start line address: 10H

Figure 4-10

Display timing generator circuit

This circuit generates the timing signals for the line address circuit and the display data latch circuit from the display clock. The display data is latched in the display data latch circuit and is output to the anode driver output pin in synchronization with the display clock. The read out of the display data to the organic EL drive circuits is completely independent of the display data RAM access from the MPU. As a result, there is no bad influence such as flickering on the display even when the display data RAM is accessed asynchronously during the organic EL display. Also, the internal cathode timing is generated by this circuit from the display clock.

Common output state selection circuit (see Table 5)

Since the COM output scanning directions can be set using the common output scan direction select command in the ML9352, it is possible to reduce the IC placement restrictions at the time of assembling organic EL modules.

Table 5

State	COM Scanning direction
Normal Display	COM0 → COM31
Reverse Display	COM31 → COM0

* When the number of display lines is 32.

Organic EL Drive circuits

The anode driver circuit employs the constant current system and the cathode driver circuit employs the push-pull system. The anode output current is set by the voltage applied to V_{EL} pin, or output voltage of the built-in voltage regulator, and the external resistors connected to the R_{EL1} and R_{EL2} pins.

$$I_{ELA} = V_{EL}/R_{EL}$$

(Here, I_{ELA}: Anode output current; V_{EL}: Voltage applied to V_{EL} pin or the output voltage of built-in voltage regulator; and R_{EL}: External resistors connected to the R_{EL1} and R_{EL2} pins.)

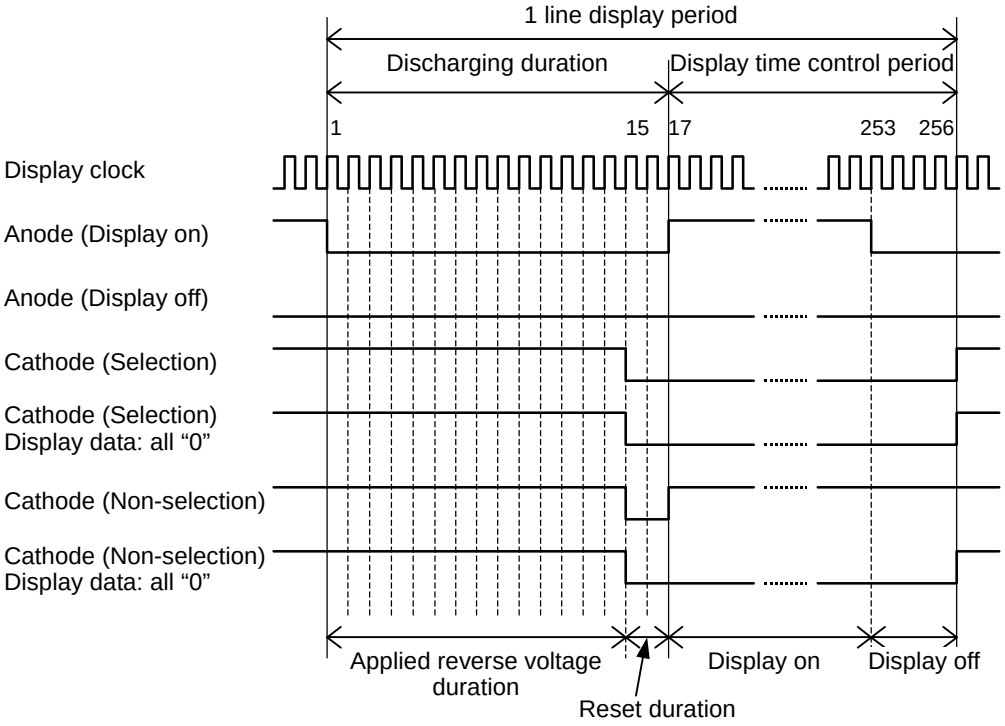
Selection between the voltage applied to the V_{EL} pin and the output voltage of built-in voltage regulator is by the EL_{SEL} pin. Similarly, selection of R_{EL1} pin or R_{EL2} pin is by the external resistor switching command for adjusting anode output current.

When in the power save mode, all operations of the built-in voltage regulator and the organic EL drive circuits are stopped. And the anode and cathode drivers' outputs go to the V_{SS} level.

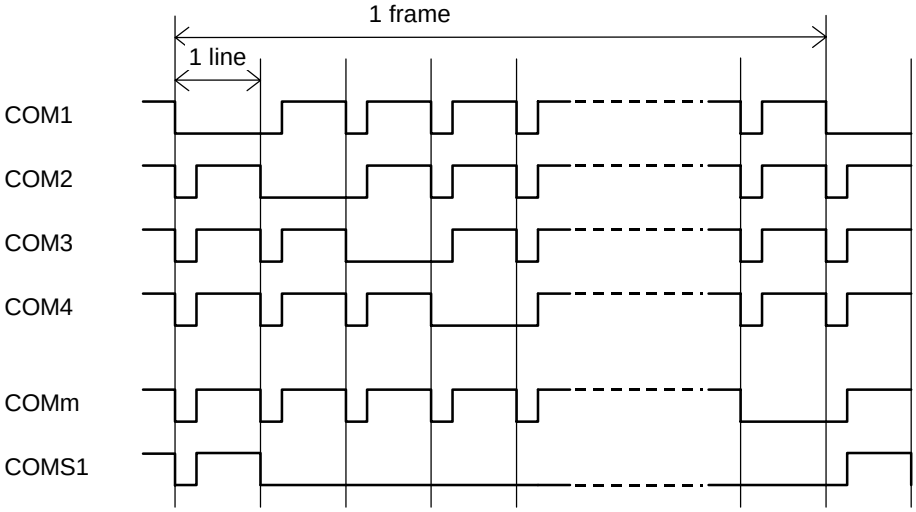
- Organic EL Driver Waveform

[Command Setting Conditions]

Anode driver system set: Set the non-display anode output status to low.
Cathode driver system set 1: Set the cathode output status during discharge period to low.
Cathode driver system set 2: Set the output status, other than during discharge period of non-selected cathode output, to high.
Anode pulse width adjustment: Set to 235/256
Reverse voltage pulse width adjustment: Set to 14/256
Applied reverse voltage setting: Set the reverse voltage to be applied.
Static on/off: Set to static ON



- Cathode Waveform



- Reset circuit

This LSI goes into the initialized condition when the $\overline{RES}$ input goes to the "L" level. The initialized condition consists of the following conditions.

(1) Display OFF
(2) Normal display mode
(3) ADC Select: Forward (ADC command D0 = "L")
(4) The registers and data in the serial interface are cleared.
(5) Read-modify-write: OFF
(6) Scroll start line is set to line 1.
(7) The column address is address 0.
(8) The write address is 00H.
(9) Common output state: Normal
(10) A fixed display line is not set.
(11) The number of display lines is 32.
(12) The anode pulse width adjustment is 0/256.
(13) The reverse voltage pulse width adjustment is 16/256.
(14) Applied reverse voltage setting OFF
(15) The cathode drive system is set to "Low during discharge" and "High during other than discharge in non-selection mode".
(16) The anode drive system is set to "Low during display OFF".
(17) The anode output current adjusting external resistor is R_{EL1}.
(18) Static OFF.

On the other hand, when the reset command is used, only the conditions (5) to (18) above are set.

As is shown in the "MPU Interface (example for reference)", the $\overline{RES}$ pin is connected to the Reset pin of the MPU and the initialization of this LSI is made simultaneously with the resetting of the MPU. This LSI always has to be reset using the $\overline{RES}$ pin at the time the power is switched ON. Also, excessive current can flow through this LSI when the control signal from the MPU is in the Hi-Z state. It is necessary to take measures to ensure that the control signal from the MPU does not go into the Hi-Z state after the power has been switched ON. During the period when $\overline{RES}$ = "L", although the oscillator circuit is operating, the display timing generator would have stopped and the CL pin would have been tied to the "H" level. There is no effect on the pins D0 to D7.

COMMANDS

MPU Interface

MPU	Read mode	Write mode
80-Series	Pin $\overline{RD}$ = "L"	Pin $\overline{WR}$ = "L"
68-Series	Pin R/$\overline{W}$ = "H" Pin E = "H"	Pin R/$\overline{W}$ = "L" Pin E = "H"

In the case of the 80-series MPU interface, a command is started by inputting a Low pulse on the $\overline{RD}$ pin or the $\overline{WR}$ pin.
In the case of the 68-series MPU interface, a command is started by inputting a High pulse on the E pin.

Description of commands

- Display ON/OFF (Write)

This is the command for controlling the turning on or off the organic EL panel. The organic EL display is turned on when a "1" is written in bit D0 and is turned off when a "0" is written in this bit. While the organic EL panel is turned off, the anode and cathode drivers output the V_{SS} level.

	A0	D7	D6	D5	D4	D3	D2	D1	D0
Display ON	0	1	0	1	0	1	1	1	1
Display OFF	0	1	0	1	0	1	1	1	0

- Display line number (2-byte command)

This command specifies the number of lines to be displayed on the organic EL panel. This command is used together with a pair of the display line number set mode command and the display line number register set command. Be sure to use these two paired commands sequentially.

- Display line number set mode (Write)

The display line number register set command is enabled by inputting this command. When the display line number set mode is set, commands other than the display line number register set command cannot be used. This status is released when display line number data is set to the register with the display line number register set command.

No. of display lines	A0	D7	D6	D5	D4	D3	D2	D1	D0
32 lines	0	1	1	0	1	0	*	*	*
Determined by display line register data	0	1	1	0	1	1	*	*	*

Note: When the number of display lines is set to 32 (D3 = 0), the display line number register set command is disabled.

- Display line number register set (Write)

The number of lines to be displayed on the organic EL panel can be selected by setting 6-bit data to the display line number register with this command. The cathode output pins are fixed to a "H" level except for the outputs that correspond to the selected lines.
The display line number set mode is released when the display line number register is set by inputting this command.

No. of display lines	A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	*	*	0	0	0	0	0	0
2	0	*	*	0	0	0	0	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
31	0	*	*	1	1	1	1	1	0
32	0	*	*	1	1	1	1	1	1

- Fixed display line number (2-byte command)

This command is used to specify the number of lines, which are not scrolled on the organic EL panel, on an 8-bit unit basis.
This command is used together with a pair of the fixed display line number set mode command and the fixed display line number register set command.
Be sure to use these two paired commands sequentially.

- Fixed display line number set mode (Write)

The fixed display line number register set command is enabled by inputting this command. When the fixed display line number set mode is set, commands other than the fixed display line number register set command cannot be used.
This status is released when fixed display line number data is set to the register with the fixed display line number register set command.

No. of fixed display lines	A0	D7	D6	D5	D4	D3	D2	D1	D0
None	0	1	0	0	1	0	*	*	*
Determined by fixed display line register data	0	1	0	0	1	1	*	*	*

Note: When the fixed display line is not set (D3 = 0), the fixed display line number register set command is disabled.

- Fixed display line number register set (Write)

The number of lines not to be scrolled on the organic EL panel can be selected on an 8-bit unit basis by setting 3-bit data to the fixed display line number register with this command.
The fixed display line number set mode is released when the fixed display line number register is set by inputting this command.

Fixed display line address	A0	D7	D6	D5	D4	D3	D2	D1	D0
00H to 07H	0	*	*	*	*	*	0	0	0
00H to 0FH	0	*	*	*	*	*	0	0	1
00H to 17H	0	*	*	*	*	*	0	1	0
00H to 1FH	0	*	*	*	*	*	0	1	1

- Scroll start line set (Write)

This command specifies the scroll start line address in the display data RAM.
The scroll start line is specified by using the scroll start line set command. It is possible to scroll the display screen by dynamically changing the address using the scroll start line set command.

Line address	A0	D7	D6	D5	D4	D3	D2	D1	D0
00H	0	0	1	0	0	0	0	0	0
01H	0	0	1	0	0	0	0	0	1
02H	0	0	1	0	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1EH	0	0	1	0	1	1	1	1	0
1FH	0	0	1	0	1	1	1	1	1

- Write Address Set (2-byte command)

This command specifies the write data of the display data RAM. Since this is a 2-byte command used with a pair of the write address set mode command and the write address register set command, be sure to use these two commands sequentially.
The display data RAM allows access to a desired bit by specifying the write address and the column address.

- Write Address Set Mode (Write)

The write address register set command is enabled by inputting this command.
When once set to the write address set command, commands other than the write address register set command cannot be used. This status is released when the write address data is set by the write address register set command.

A0	D7	D6	D5	D4	D3	D2	D1	DO
0	1	0	1	1	*	*	*	*

- Write address register set (Write)

This command specifies the write address of the display data RAM by setting 6-bit data to the write address register.
The write address set mode is released when the write address register is set by inputting this command.

Write address	A0	D7	D6	D5	D4	D3	D2	D1	D0
00H	0	*	*	0	0	0	0	0	0
01H	0	*	*	0	0	0	0	0	1
02H	0	*	*	0	0	0	0	1	0
03H	0	*	*	0	0	0	0	1	1
04H	0	*	*	0	0	0	1	0	0
05H	0	*	*	0	0	0	1	0	1
06H	0	*	*	0	0	0	1	1	0
07H	0	*	*	0	0	0	1	1	1
08H	0	*	*	0	0	1	0	0	0
09H	0	*	*	0	0	1	0	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1EH	0	*	*	0	1	1	1	1	0
1FH	0	*	*	0	1	1	1	1	1

- Column address set (Write)

This command specifies the column address of the display data RAM. The column address is specified by successively writing the upper 4 bits and the lower 4 bits. Since the column address is automatically incremented (by +1) every time the display data RAM is accessed, the MPU can read or write the display data continuously. The incrementing of the column address is stopped at the address 7FH.

	A0	D7	D6	D5	D4	D3	D2	D1	D0
Upper bits	0	0	0	0	1	a7	a6	a5	a4
Lower bits	0	0	0	0	0	a3	a2	a1	a0

Column address	a7	a6	a5	a4	a3	a2	a1	a0
00H	0	0	0	0	0	0	0	0
01H	0	0	0	0	0	0	0	1
02H	0	0	0	0	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
7EH	0	1	1	1	1	1	1	0
7FH	0	1	1	1	1	1	1	1

- Status read (Read)

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	When BUSY is '1', it indicates that the internal operations are being made or the LSI is being reset. Although no command is accepted until BUSY becomes '0', there is no need to check this bit if the cycle time can be satisfied.
ADC	This bit indicates the relationship between the column address and the segment driver. 0: Reverse (SEG127 → SEG0; column address 0H → 7FH) 1: Forward (SEG0 → SEG127; column address 0H → 7FH) (Opposite to the polarity of the ADC command.)
ON/OFF	This bit indicates the ON/OFF state of the display. (Opposite to the polarity of the display ON/OFF command.) 0: Display ON 1: Display OFF
RESET	This bit indicates that the LSI is being reset due to the $\overline{RES}$ signal or the reset command. 0: Operating state 1: Being reset

- Display data write (Write)

This command writes an 8-bit data at the specified address of the display data RAM. Since the column address is automatically incremented (by +1) after writing the data, the MPU can write the display data to the display data RAM continuously.

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	Write data							

- Display data read (Read)

This command read the 8-bit data from the specified address of the display data RAM. Since the column address is automatically incremented (by +1) after reading the data, the MPU can read display data from the display data RAM continuously. Further, one dummy read operation is necessary immediately after setting the column data. The display data cannot be read out when the serial interface is being used.

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	Read data							

- ADC Select (segment driver direction select) (Write)

Using this command it is possible to reverse the relationship of correspondence between the column address of the display data RAM and the segment driver output. It is possible to reverse the sequence of the segment driver output pin by the command.

	A0	D7	D6	D5	D4	D3	D2	D1	D0
Forward	0	1	0	1	0	0	0	0	0
Reverse	0	1	0	1	0	0	0	0	1

- Normal/reverse display mode (Write)

It is possible to toggle the display on and off condition without changing the contents of the display data RAM. In this case, the contents of the display data RAM will be retained.

	A0	D7	D6	D5	D4	D3	D2	D1	D0	RAM Data
Forward	0	1	0	1	0	0	1	1	0	Organic EL ON when “H”
Reverse	0	1	0	1	0	0	1	1	1	Organic EL ON when “L”

- Display all-ON/OFF (Write)

Using this command, it is possible to forcibly turn ON all the dots in the display irrespective of the contents of the display data RAM. In this case, the contents of the display data RAM will be retained.
This command is given priority over the Normal/reverse display mode command.

	A0	D7	D6	D5	D4	D3	D2	D1	D0
Normal display state	0	1	0	1	0	0	1	0	0
All-on display	0	1	0	1	0	0	1	0	1

The power save mode will be entered into when the Display all-ON command is executed in the display OFF condition.

- Read-modify-write (Write)

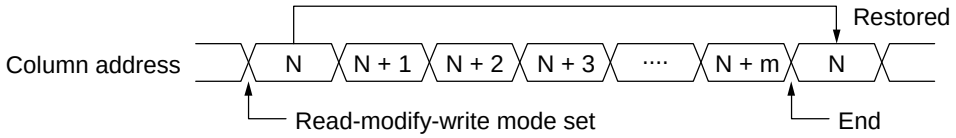
This command is used in combination with the End command. When this command is issued once, the column address is not changed when the Display data read command is issued, but is incremented (by +1) only when the Display data write command is issued. This condition is maintained until the End command is issued. When the End command is issued, the column address is restored to the address that was effective at the time the Read-modify-write command was issued last. Using this function, it is possible to reduce the overhead on the MPU when repeatedly changing the data in special display area such as a blinking cursor.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	0	0	0

- End (Write)

This command releases the read-modify-write mode and restores the column address to the value at the beginning of the read-modify-write mode.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	1	1	1	0



- Reset (Write)

This command initializes the scroll start line number, column address, page address, common output state, fixed display line, number of display lines, anode pulse width adjustment, cathode driving, and anode driving, and also releases the read-modify-write mode and the test mode. This command does not affect the contents of the display data RAM.

The reset operation is made after issuing the reset command.

The initialization after switching on the power is carried out by the reset signal input to the $\overline{RES}$ pin.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	0	1	0

- Common output scan direction select (Write)

This command is used for selecting the scanning direction of the COM output pins.

	ML9352	A0	D7	D6	D5	D4	D3	D2	D1	D0
Forward	COM0 → COM31	0	1	1	0	0	0	*	*	*
Reverse	COM31 → COM0	0	1	1	0	0	1	*	*	*

*: Invalid bits

- Cathode drive set 1 (Write)

This command is used to select an output state of the cathode drive circuit during discharging.

Cathode output state	A0	D7	D6	D5	D4	D3	D2	D1	D0
Low	0	1	0	1	0	0	0	1	0
High	0	1	0	1	0	0	0	1	1

- Cathode drive set 2 (Write)

This command is used to select an output state of the unselected cathode drive circuit during other than discharging.

Cathode output state	A0	D7	D6	D5	D4	D3	D2	D1	D0
High	0	1	0	1	0	1	0	1	0
High impedance	0	1	0	1	0	1	0	1	1

- Anode drive set (Write)

This command is used to select an output state of the anode drive circuit during display-OFF condition.

Anode output state	A0	D7	D6	D5	D4	D3	D2	D1	D0
Low	0	1	0	1	0	1	0	0	0
High impedance	0	1	0	1	0	1	0	0	1

- Anode pulse width adjustment (Write)

This command specifies the output pulse width of the anode driver outputs (SEG0 to SEG127). This allows a luminance of the organic EL panel to be set.
This command is used together with a pair of the anode pulse width adjustment set mode command and the anode pulse width adjustment register set command. Be sure to use these paired commands sequentially.

- Anode pulse width adjustment set mode (Write)

The anode pulse width adjustment register set command is enabled by setting this command. When the anode pulse width adjustment set mode is set, commands other than the anode pulse width adjustment register set command cannot be used. This state is released by setting anode pulse width adjustment data to the register.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	1

- Anode pulse width adjustment register set (Write)

The duty of anode driver output pulse width is set between 0/256 and 240/256 by setting 8-bit data to the anode pulse width adjustment register using this command.
If 8-bit data (D7 to D0) is set with F0h to FFh, the output pulse width (duty) becomes 240/256.
When the anode pulse width adjustment register is set by inputting this command, the anode pulse width adjustment set mode is released.

Output pulse width (Duty)	A0	D7	D6	D5	D4	D3	D2	D1	D0
0/256	0	0	0	0	0	0	0	0	0
1/256	0	0	0	0	0	0	0	0	1
2/256	0	0	0	0	0	0	0	1	0
•	•	•	•	•	•	•	•	•	•
239/256	0	1	1	1	0	1	1	1	1
240/256	0	1	1	1	1	0	0	0	0
•	•	•	•	•	•	•	•	•	•
240/256	0	1	1	1	1	1	1	1	1

- Reverse voltage pulse width adjustment (Write)

This command specifies the pulse width for the reverse voltage applying duration (applying reverse voltage makes all anode outputs low and all cathode outputs high). This command is used together with a pair of the reverse voltage pulse width adjustment set mode command and the reverse voltage pulse width adjustment register set command. Be sure to use these paired commands sequentially.

- Reverse voltage pulse width adjustment set mode (Write)

The reverse voltage pulse width adjustment register set command is enabled by setting this command. When the reverse voltage pulse width adjustment set mode is set, commands other than the reverse voltage pulse width adjustment register set command cannot be used. This state is released by setting reverse voltage pulse width adjustment data to the register.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	1	0

- Reverse voltage pulse width adjustment register set (Write)

The pulse width for the reverse voltage applying duration (applying reverse voltage makes all anode outputs low and all cathode outputs high) is set between 0/256 and 16/256 by setting 4-bit data to the reverse voltage pulse width adjustment register using this command.
When the reverse voltage pulse width adjustment register is set by inputting this command, the reverse voltage pulse width adjustment set mode is released.

Reverse voltage pulse width	A0	D7	D6	D5	D4	D3	D2	D1	D0
16/256	0	*	*	*	*	0	0	0	0
14/256	0	*	*	*	*	0	0	0	1
12/256	0	*	*	*	*	0	0	1	0
10/256	0	*	*	*	*	0	0	1	1
8/256	0	*	*	*	*	0	1	0	0
6/256	0	*	*	*	*	0	1	0	1
4/256	0	*	*	*	*	0	1	1	0
2/256	0	*	*	*	*	0	1	1	1
0/256	0	*	*	*	*	1	0	0	0

- Applied reverse voltage setting (Write)

Selects whether to apply the reverse voltage during the discharge interval.
Valid only when, in the cathode drive set 1, the cathode output status during the discharge interval has been set to low.

Cathode output state	A0	D7	D6	D5	D4	D3	D2	D1	D0
Applied reverse voltage setting off	0	1	0	0	0	0	1	0	0
Applied reverse voltage setting on	0	1	0	0	0	0	1	0	1

- Switching of anode output current adjusting external resistor (Write)

This command selects connection pin R_{EL1} or R_{EL2} of the external resistor for adjusting anode output current.

Select pin	A0	D7	D6	D5	D4	D3	D2	D1	D0
R_{EL1}	0	1	0	0	0	1	0	1	0
R_{EL2}	0	1	0	0	0	1	0	1	1

- Static ON/OFF (Write)

This is an operation control command of the cathode driver output (COMS1) for static display. When a "1" is written in bit D0, COMS1 operates and it is possible to carry out the static display. On the other hand, when a "0" is written in bit D0, COMS1 goes high and the static display is turned off.

Select pin	A0	D7	D6	D5	D4	D3	D2	D1	D0
Static ON	0	1	0	1	0	1	1	0	1
Static OFF	0	1	0	1	0	1	1	0	0

- Power save (Compound command)

The power save mode is entered when the display all-ON command is executed in the display OFF condition. This mode can greatly reduce the current consumption.
When in the power save mode, the display data and operating mode remain unchanged, and also it is possible to access the display data RAM from the MPU. The power save mode is released by using the display all-OFF command.

- Power save mode

When in the power save mode, all operations of the organic EL driving circuit are stopped. When there is no access from the MPU, the current consumption can be reduced to nearly the static current. The internal circuit conditions in the power save mode are described below.

(1) The oscillation circuit stops.
(2) The voltage regulator stops.
(3) All the organic EL driving circuits stop and the anode and cathode drivers output the V_{SS} level.

- NOP (Write)

This is a No Operation command.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	0	1	1

- Test (Write)

This is a command for testing the IC chip. Do not use this command. When the test command is issued by mistake, this state can be released by issuing a NOP command. This command will be ineffective if the TEST0 pin is open or at the "L" level.

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	*	*	*	*

*: Invalid bits

LIST OF COMMANDS

No	Operation (ML9352)	Dn								A0	$\overline{RD}$	$\overline{WR}$	Comment
		7	6	5	4	3	2	1	0				
1	Display OFF	1	0	1	0	1	1	1	0	0	1	0	EL display OFF
	Display ON	1	0	1	0	1	1	1	1	0	1	0	EL display ON
2	Display line number set	1	1	0	1	0	*	*	*	0	1	0	32-line display
		1	1	0	1	1	*	*	*	0	1	0	Sets the number of display lines to the display line number register.
	Display line number register set	*	*	No. of display lines						0	1	0	
3	Fixed display line number set	1	0	0	1	0	*	*	*	0	1	0	Without a fixed display line
		1	0	0	1	1	*	*	*	0	1	0	Sets the number of fixed display lines to the fixed display line number register.
	Fixed display line number register set	*	*	*	*	*	No. of fixed display lines			0	1	0	
4	Scroll start line set	0	1	Display start line address						0	1	0	Sets the scroll start line address of the display data RAM.
5	Write address set mode	1	0	1	1	*	*	*	*	0	1	0	Sets the write address of the display data RAM.
	Write address register set	*	*	Write address						0	1	0	
6	Column address set (upper)	0	0	0	1	Column address (Upper)				0	1	0	Sets the upper 4 bits of column address of the display data RAM.
	Column address set (lower)	0	0	0	0	Column address (Lower)				0	1	0	Sets the lower 4 bits of column address of the display data RAM.
7	Status read	Status				0	0	0	0	0	0	1	Reads the status information using the upper 4 bits.
8	Display data write	Write data								1	1	0	Writes data to the display data RAM.
9	Display data read	Read data								1	0	1	Reads data from the display data RAM.
10	ADC select forward	1	0	1	0	0	0	0	0	0	1	0	Correspondence between the display data RAM address and SEG output (Forward)
	ADC select reverse	1	0	1	0	0	0	0	1	0	1	0	Correspondence between the display data RAM address and SEG output (Reverse)
11	Normal display	1	0	1	0	0	1	1	0	0	1	0	EL display normal
	Reverse display	1	0	1	0	0	1	1	1	0	1	0	EL display reverse
12	Normal display	1	0	1	0	0	1	0	0	0	1	0	Normal EL display
	Display all-ON	1	0	1	0	0	1	0	1	0	1	0	EL display all ON
13	Read-modify-write	1	1	1	0	0	0	0	0	0	1	0	Increments the column address (by +1) during a write only.
14	End	1	1	1	0	1	1	1	0	0	1	0	Releases the read-modify-write state.
15	Reset	1	1	1	0	0	0	1	0	0	1	0	Internal reset
16	Scanning COM outputs in forward direction	1	1	0	0	0	*	*	*	0	1	0	COM output scanning direction forward
	Scanning COM outputs in reverse direction	1	1	0	0	1	*	*	*	0	1	0	COM output scanning direction reverse
17	Cathode drive set 1	1	0	1	0	0	0	1	0	0	1	0	Cathode driver output “L” level during discharging
		1	0	1	0	0	0	1	1	0	1	0	Cathode driver output “H” level during discharging

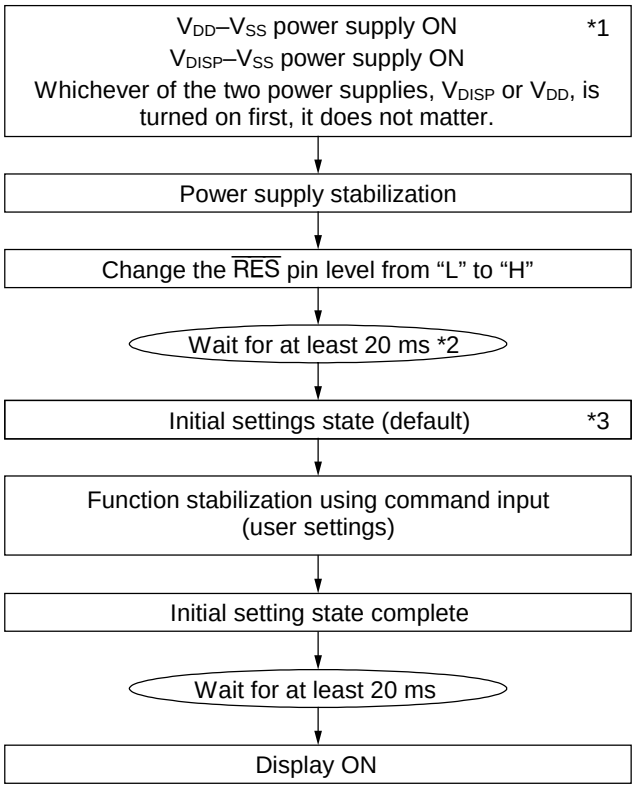
No	Operation (ML9352)	Dn								A0	$\overline{RD}$	$\overline{WR}$	Comment
		7	6	5	4	3	2	1	0				
18	Cathode drive set 2	1	0	1	0	1	0	1	0	0	1	0	Unselected Cathode driver output “H” level during other than discharging
		1	0	1	0	1	0	1	1	0	1	0	Unselected Cathode driver is high impedance during other than discharging
19	Anode drive set	1	0	1	0	1	0	0	0	0	1	0	Anode driver output “L” level during display OFF
		1	0	1	0	1	0	0	1	0	1	0	Anode driver output high impedance during display OFF
20	Anode pulse width adjustment set	1	0	0	0	0	0	0	1	0	1	0	Sets the anode pulse width data to the anode pulse width adjustment register.
	Anode pulse width adjustment register set	Pulse width data								0	1	0	
21	Reverse voltage pulse width adjustment set mode	1	0	0	0	0	0	1	0	0	1	0	Sets the data of the pulse width of the reverse voltage applying duration to the reverse voltage pulse width adjustment register.
	Reverse voltage pulse width adjustment register set	*	*	*	*	Pulse width data				0	1	0	
22	Applied reverse voltage setting	1	0	0	0	0	1	0	0	0	1	0	Applied reverse voltage setting OFF
		1	0	0	0	0	1	0	1	0	1	0	Applied reverse voltage setting ON
23	Switching of the anode output current adjusting external resistor	1	0	0	0	1	0	1	0	0	1	0	Selects the R_{EL1} pin.
		1	0	0	0	1	0	1	1	0	1	0	Selects the R_{EL2} pin.
24	Static ON	1	0	1	0	1	1	0	1	0	1	0	Cathode driver for static display (COMS1) operates.
	Static OFF	1	0	1	0	1	1	0	0	0	1	0	COMS1 always “H”.
25	Power save												Compound command of display OFF and display all ON
26	NOP	1	1	1	0	0	0	1	1	0	1	0	The “No Operation” command
27	Test	1	1	1	1	*	*	*	*	0	1	0	The command for factory testing of the IC chip

*: Invalid data

DESCRIPTION OF COMMANDS

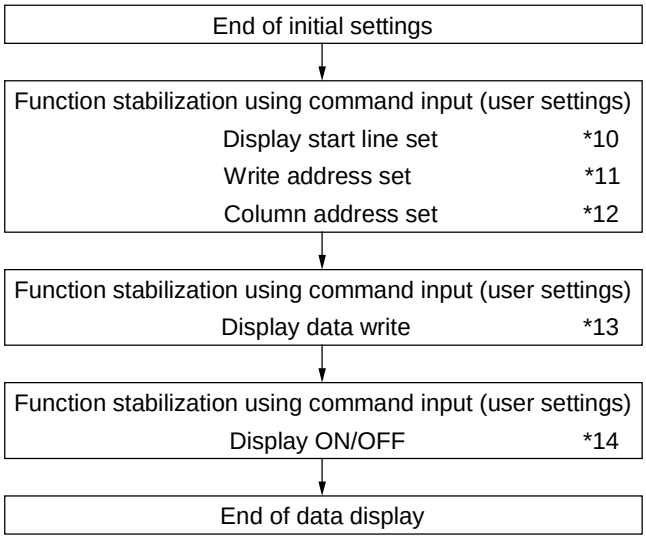
Examples of settings for the instructions (reference examples)

- Initial setting



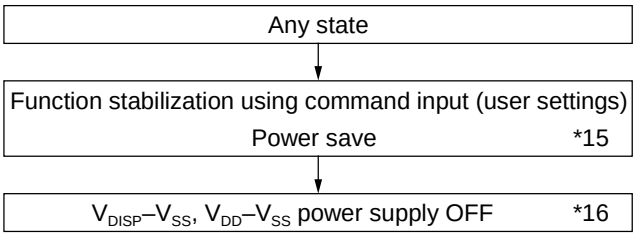
Notes: Sections to be referred to
*1: V_{DD}: V_{DDA} and V_{DDL}
V_{DISP}: V_{DISPS} and V_{DISPC}
V_{SS}: V_{SSA}, V_{SSL}, V_{SSS}, and V_{SSC}
*2: Stabilization time of the internal oscillator
*3: Function description “Reset circuit”

- Data display



Notes: Sections to be referred to
*10: Command description “Display start line set”
*11: Command description “Write address set”
*12: Command description “Column address set”
*13: Command description “Display data write”
*14: Command description “Display ON/OFF”

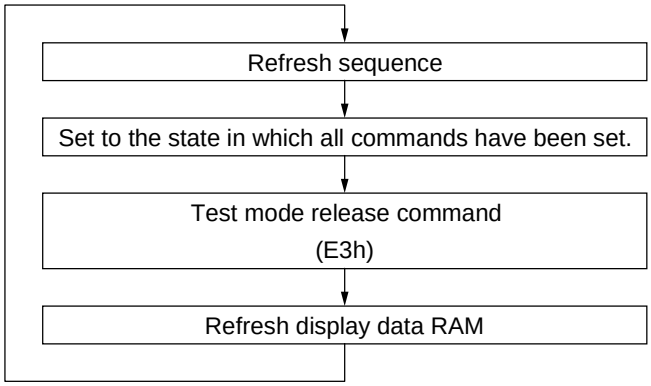
- Power supply OFF



Notes: Sections to be referred to
*15: Command description “Power save”
*16: Do not enter Reset when switching the power supply OFF.
V_{DD}: V_{DDA} and V_{DDL}
V_{DISP}: V_{DISPS} and V_{DISPC}
V_{SS}: V_{SSA}, V_{SSL}, V_{SSS}, and V_{SSC}

- Refresh

To avoid malfunction or erroneous display, it is recommended to use the refresh sequence at regular intervals.



ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit	Applicable pins
Power supply voltage	V_{DD}	Ta = 25°C	–0.3 to +6.5	V	V_{DD}, V_{SS}
EL drive voltage	V_{DISP}	Ta = 25°C	–0.3 to +35	V	V_{DISP}, V_{SS}
EL reference voltage	V_{EL}	—	–0.3 to V_{DISPS}	V	V_{EL}, V_{SS}
Logic input voltage	V_I	Ta = 25°C	–0.3 to V_{DD}+0.3	V	All logic inputs
Anode output voltage	V_{ELA}	Ta = 25°C	–0.3 to V_{DISPS}+0.3	V	SEG0 to 127
Cathode output voltage	V_{ELK}	Ta = 25°C	–0.3 to V_{DISPC}+0.3	V	COM0 to 31, COMS1
Anode output current	I_{ELA}	during “L” level output	0.0 to 30	mA	SEG0 to 127
		during “H” level output	–1.0 to 0.0		
Cathode output current	I_{ELK}	during “L” level output	0.0 to 150	mA	COM0 to 31, COMS1
		during “H” level output	–70 to 0.0		
Storage temperature range	T_{stg}	Chip	–55 to +125	°C	—

Ta: Ambient temperature
V_{DD}: V_{DDA} and V_{DDL}
V_{DISP}: V_{DISPS} and V_{DISPC}
V_{SS}: V_{SSA}, V_{SSL}, V_{SSS}, and V_{SSC}

RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0 V

Parameter	Symbol	Condition	Range	Unit	Applicable pins
Power supply voltage	V_{DD}	—	2.7 to 5.5	V	V_{DD}, V_{SS}
EL drive voltage	V_{DISP}	—	18 to 30	V	V_{DISP}, V_{SS}
EL reference voltage	V_{EL}	—	4 to V_{DISPS}/3	V	V_{EL}, V_{SS}
Anode output voltage	V_{ELA}	—	–0.3 to V_{DISPS}–5	V	SEG0 to 127
Cathode output voltage	V_{ELC}	—	–0.3 to V_{DISPC}	V	COM0 to 31, COMS1
“H” anode output current	I_{ELA}	—	–0.8 to –0.1	mA	SEG0 to 127
“L” anode output current (during charging or discharging of the panel capacitance)	I_{ELA}	—	0 to 20	mA	
“H” cathode output current (during charging or discharging of the panel capacitance)	I_{ELK}	—	–50 to 0	mA	COM0 to 31, COMS1
“L” cathode output current	I_{ELK}	—	0 to 100	mA	
Operating temperature range	Tjop	—	–40 to +125	°C	—

V_{DD}: V_{DDA} and V_{DDL}
V_{DISP}: V_{DISPS} and V_{DISPC}
V_{SS}: V_{SSA}, V_{SSL}, V_{SSS}, and V_{SSC}

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{DISP} = 18 to 30 V, V_{SS} = 0 V, Tjop = –40 to +125°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pins
"H" input voltage "L" input voltage	V_{IH} V_{IL}	—	0.8 × V_{DD} V_{SS}	—	V_{DD} 0.2 × V_{DD}	V	*1
"H" output voltage "L" output voltage	V_{OH} V_{OL}	I_{OH} = –0.5 mA I_{OL} = 0.5 mA	0.8 × V_{DD} V_{SS}	—	V_{DD} 0.2 × V_{DD}	V	*2
"H" input current "L" input current	I_{IH1} I_{IL}	V_I = V_{DD} V_I = 0 V	–10	—	+10	µA	*3 *4
"H" input current	I_{IH2}	V_I = V_{DD}	5	—	200	µA	*5
Anode driver average output current 1 *6	$-I_{ELA1}$	ELSEL = "H" V_{EL} = 5 V R_{EL2} = 7.2 kΩ V_{OH} = V_{DISPS} – 8 V	–724	–694	–664	µA	SEG0 to 127
Anode driver output current dispersion within the LSI chip 1 *7	ΔI_{ELA11}	ELSEL= "H" V_{EL} = 5 V R_{EL2} = 7.2 kΩ V_{OH} = V_{DISPS} – 8 V	–5	0	+5	%	SEG0 to 127
Anode driver output current dispersion within 8 contiguous bits 1 *8	ΔI_{ELA21}	ELSEL = "H" V_{EL} = 5 V R_{EL2} = 7.2 kΩ V_{OH} = V_{DISPS} –8 V	–4	0	+4	%	SEG0 to 127
Anode driver average output current 2 *6	$-I_{ELA2}$	ELSEL = "L" R_{EL2} = 7.2 kΩ V_{OH} = V_{DISPS} – 8 V	–770	–694	–617	µA	SEG0 to 127
Anode driver output current dispersion within the LSI chip 2 *7	ΔI_{ELA12}	ELSEL = "L" R_{EL2} = 7.2 kΩ V_{OH} = V_{DISPS} – 8 V	–5	0	+5	%	SEG0 to 127
Anode driver output current dispersion within 8 contiguous bits 2 *8	ΔI_{ELA22}	ELSEL = "L" R_{EL2} = 7.2 kΩ V_{OH} = V_{DISPS} – 8 V	–4	0	+4	%	SEG0 to 127
Anode driver average output current 3 *6	$-I_{ELA3}$	ELSEL = "H" V_{EL} = 5 V R_{EL1} = 24.7 kΩ V_{OH} = V_{DISPS} – 8 V	–212	–202	–192	µA	SEG0 to 127
Anode driver output current dispersion within the LSI chip 3 *7	ΔI_{ELA13}	ELSEL = "H" V_{EL} = 5 V R_{EL1} = 24.7 kΩ V_{OH} = V_{DISPS} – 8 V	–5	0	+5	%	SEG0 to 127
Anode driver output current dispersion within 8 contiguous bits 3 *8	ΔI_{ELA23}	ELSEL = "H" V_{EL} = 5 V R_{EL1} = 24.7 kΩ V_{OH} = V_{DISPS} – 8 V	–4	0	+4	%	SEG0 to 127

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pins
Anode driver average output current 4 *6	$-I_{ELA4}$	ELSEL = "L" R_{EL1} = 24.7 kΩ $V_{OH} = V_{DISPS} - 8$ V	–224	–202	-180	μA	SEG0 to 127
Anode driver output current dispersion within the LSI chip 4 *7	ΔI_{ELA14}	ELSEL = "L" R_{EL1} = 24.7 kΩ $V_{OH} = V_{DISPS} - 8$ V	–5	0	+5	%	SEG0 to 127
Anode driver output current dispersion within 8 contiguous bits 4 *8	ΔI_{ELA24}	ELSEL = "L" R_{EL1} = 24.7 kΩ $V_{OH} = V_{DISPS} - 8$ V	–4	0	+4	%	SEG0 to 127
Output voltage fluctuation to anode driver output current 1 *9	ΔI_{ELA31}	ELSEL = "H" V_{EL} = 5 V R_{EL2} = 7.2 kΩ $V_{OH} \leq V_{DISPS} - 3$ V	–2.5	—	—	%/V	SEG0 to 127
Output voltage fluctuation to anode driver output current 2 *9	ΔI_{ELA32}	ELSEL = "H" V_{EL} = 5 V R_{EL1} = 24.7 kΩ $V_{OH} \leq V_{DISPS} - 3$ V	–2.0	—	—	%/V	SEG0 to 127
V_{DISP} voltage fluctuation to anode driver output current 1 *10	ΔI_{ELA41}	ELSEL = "H" V_{EL} = 5 V V_{OH} = 10 V R_{EL2} = 7.2 kΩ V_{DISPS} = 18 to 30 V	—	—	+2.0	%/V	SEG0 to 127
V_{DISP} voltage fluctuation to anode driver output current 2 *10	ΔI_{ELA42}	ELSEL = "H" V_{EL} = 5 V V_{OH} = 10 V R_{EL1} = 24.7 kΩ V_{DISPS} = 18 to 30 V	—	—	+2.0	%/V	SEG0 to 127
Anode driver "L" output current	I_{ELAL}	V_{DISPS} = 18 V V_O = 18 V	20	—	—	mA	SEG0 to 127
Cathode driver "L" output current	I_{ELCL}	V_{DISPC} = 18 V V_O = 1 V Only one output is "L".	100	—	—	mA	COM0 to 31, COMS1
Cathode driver "H" output current	I_{ELC1H}	V_{DISPC} = 18 V V_O = 0 V	–50	—	—	mA	COM0 to 31, COMS1
Voltage regulator output	V_{REG}	—	4.7	5	5.3	V	TEST5
Input pin capacitance	C_{IN}	Ta = 25°C, f = 1 MHz	—	5	8	pF	
Oscillator frequency — Internal oscillation	f_{OSC}	—	3.07	4.05	5.33	MHz	*11
Oscillator frequency — External input	f_{CL}	—	32	—	1000	kHz	CL*5
Internal oscillator frequency adjustment	f_{OSCADJ}	Connect R_{OSC} to V_{SSL}	–20	–16	–12	%	

*1: A0, D0 to D5, D6 (SCL), D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, CL, C86, $\overline{P}$/S, $\overline{RES}$, EL_{SEL}
*2: D0 to D7, CL
*3: A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, $\overline{RES}$
*4: Applicable to the pins D0 to D5, D6 (SCL), D7 (SI), and CL in the high impedance state.
*5: CLS, C86, $\overline{P}$/S, EL_{SEL}
*6: The average of output currents of SEG0 to SEG127
*7: Each output current from SEG0 to SEG127 divided by the average of output currents of SEG0 to SEG127
*8: Each output current from SEG_{8n} to SEG_{8n+7} divided by the average of output currents of SEG_{8n} to SEG_{8n+7}: n = 0 to 15
*9: $\{[I(V_O = V_{DISPS} - 8\ V) - I(V_O = V_{DISP} - n\ V)]/[(V_{DISPS} - 8\ V) - (V_{DISP} - n\ V)]\}/I(V_O = V_{DISPS} - 8\ V) \times 100$
*10: $\{[I(V_{DISP} = n\ V) - I(V_{DISPS} = 18\ V)]/(n\ V - 18\ V)\}/I(V_{DISPS} = 18\ V) \times 100$
*11: See Table 24 for the relationship between the oscillator frequency and the frame frequency.

V_{DD}: V_{DDA} and V_{DDL}
V_{DISP}: V_{DISPS} and V_{DISPC}
V_{SS}: V_{SSA}, V_{SSL}, V_{SSS}, and V_{SSC}

Table 24 Relationship among the oscillator frequency (f_{OSC}), display clock frequency (f_{CL}), and Organic EL frame frequency (f_{FR})

When the internal oscillator is used	No. of display lines	Frame frequency (Hz)	Error (Hz)
	1	124.92	0.0
	2	124.92	0.0
	3	124.92	0.0
	4	124.92	0.0
	5	119.92	–5.08
	6	124.92	0.0
	7	142.76	17.76
	8	124.92	0.0
	9	133.25	8.25
	10	119.92	–5.08
	11	136.27	11.27
	12	124.92	0.0
	13	115.31	–9.69
	14	142.76	17.76
	15	133.25	8.25
	16	124.92	0.0
	17	117.57	–7.43
	18	133.25	8.25
	19	126.23	1.23
	20	119.92	–5.08
	21	114.21	–10.79
	22	136.27	11.27
	23	130.35	5.35
	24	124.92	0.0
	25	119.92	–5.08
	26	115.31	–9.69
	27	111.04	–13.96
	28	142.76	17.76
	29	137.84	12.84
	30	133.25	8.25
	31	128.95	3.95
	32	124.92	0.0

Note: The above values apply when f_{OSC} = 3.07 MHz.

Parameter	Display clock frequency (f_{CL})	Organic EL frame frequency (f_{FR})
When the internal oscillator is not used	External input	$f_{CL}/(256 \times$ No. of display lines)

- Operating current consumption value (V_{DD} = 2.7 to 5.5 V, V_{DISP} = 18 to 30 V, V_{SS} = 0 V, Tjop = –40 to +125°C)

(1) During display operation
Display mode: All-white (When an organic EL panel is not connected)

Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
I_{DDA}	V_{DD} = 3 V, V_{DISP} = 30 V	—	—	1.0	mA	
	V_{DD} = 5 V, V_{DISP} = 30 V	—	—	1.5		
I_{DDL}	V_{DD} = 3 V, V_{DISP} = 30 V	—	—	1.5		
	V_{DD} = 5 V, V_{DISP} = 30 V	—	—	2.5		
I_{DISPS}	V_{DISPS} = 30 V	—	—	3.0		
I_{DISPC}	V_{DISPC} = 30 V	—	—	1.0		

Display mode: Checker pattern (When an organic EL panel is not connected)

Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
I_{DDA}	V_{DD} = 3 V, V_{DISP} = 30 V	—	—	1.0	mA	
	V_{DD} = 5 V, V_{DISP} = 30 V	—	—	1.5		
I_{DDL}	V_{DD} = 3 V, V_{DISP} = 30 V	—	—	1.5		
	V_{DD} = 5 V, V_{DISP} = 30 V	—	—	2.5		
I_{DISPS}	V_{DISPS} = 30 V	—	—	3.0		
I_{DISPC}	V_{DISPC} = 30 V	—	—	1.0		

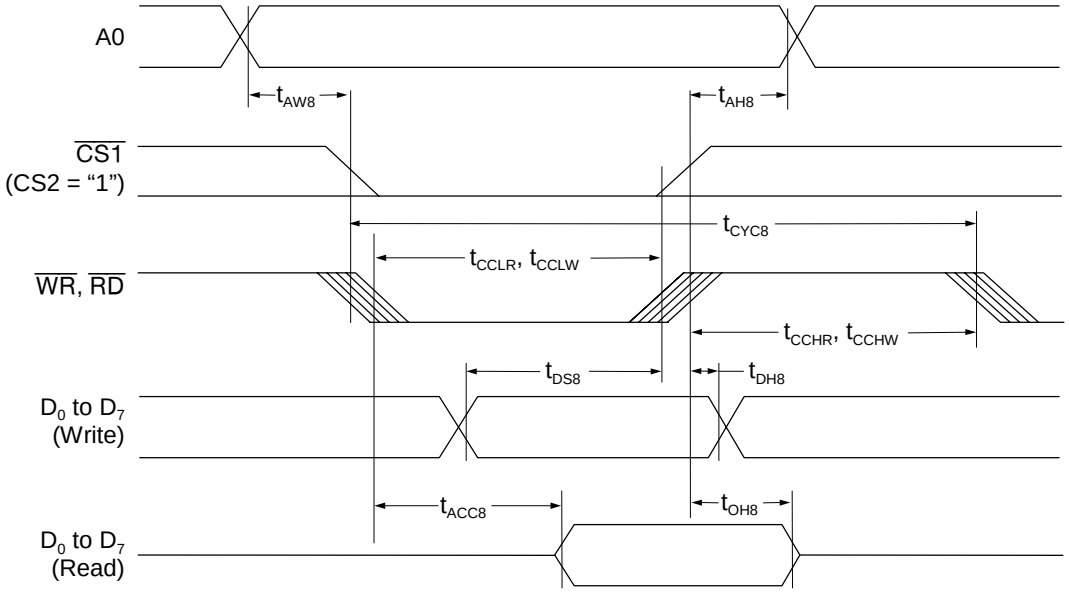
- Power save current consumption (V_{DD} = 2.7 to 5.5 V, V_{DISP} = 18 to 30 V, V_{SS} = 0 V, Tjop = –40 to +125°C)

Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
I_{DDAS}	During the power save mode	—	—	10.0	μA	
I_{DDLS}	During the power save mode	—	—	50.0		
I_{DISPSS}	During the power save mode	—	—	20.0		
I_{DISPCS}	During the power save mode	—	—	50.0		

V_{DD}: V_{DDA} and V_{DDL}
V_{DISP}: V_{DISPS} and V_{DISPC}
V_{SS}: V_{SSA}, V_{SSL}, V_{SSS}, and V_{SSC}

Timing Characteristics

- System bus read/write characteristics 1 (80-series MPU)



(V_{DDA} = V_{DDL} = 4.5 to 5.5 V, V_{SSA} = V_{SSL} = 0 V, Tjop = –40 to +125°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address hold time	t_{AH8}		0	—	ns
Address setup time	t_{AW8}		0	—	
System cycle time	t_{CYC8}		166	—	
Control "L" pulse width ($\overline{WR}$)	t_{CCLW}		30	—	
Control "L" pulse width ($\overline{RD}$)	t_{CCLR}		30	—	
Control "H" pulse width ($\overline{WR}$)	t_{CCHW}		30	—	
Control "H" pulse width ($\overline{RD}$)	t_{CCHR}		30	—	
Data setup time	t_{DS8}		30	—	
Data hold time	t_{DH8}		10	—	
$\overline{RD}$ access time	t_{ACC8}	CL = 100 pF	—	30	
Output disable time	t_{OH8}		5	50	

(V_{DDA} = V_{DDL} = 2.7 to 4.5 V, V_{SSA} = V_{SSL} = 0 V, Tjop = –40 to +125°C)

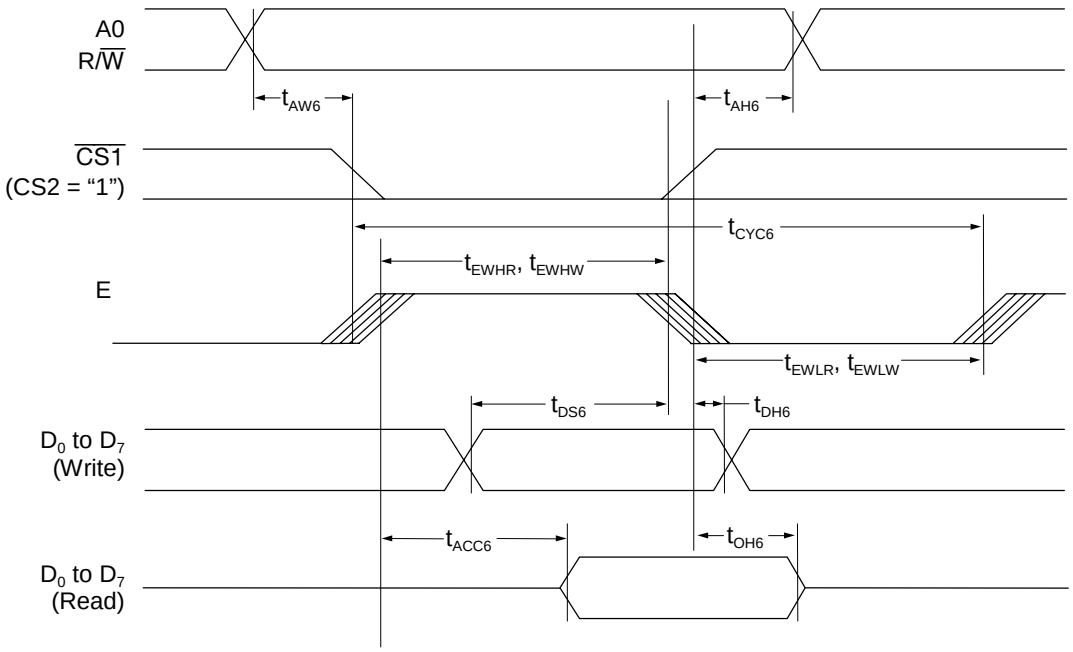
Parameter	Symbol	Condition	Min.	Max.	Unit
Address hold time	t_{AH8}		0	—	ns
Address setup time	t_{AW8}		0	—	
System cycle time	t_{CYC8}		400	—	
Control “L” pulse width ($\overline{WR}$)	t_{CCLW}		60	—	
Control “L” pulse width ($\overline{RD}$)	t_{CCLR}		120	—	
Control “H” pulse width ($\overline{WR}$)	t_{CCHW}		60	—	
Control “H” pulse width ($\overline{RD}$)	t_{CCHR}		60	—	
Data setup time	t_{DS8}		40	—	
Data hold time	t_{DH8}		15	—	
$\overline{RD}$ access time	t_{ACC8}	CL = 100 pF	—	140	
Output disable time	t_{OH8}		10	100	

Note 1: The input signal rise and fall times are specified as 15 ns or less.
When using the system cycle time for fast speed, the specified values are (tr + tf) ≤ (t_{CYC8} – t_{CCLW} – t_{CCHW}) or (tr + tf) ≤ (t_{CYC8} – t_{CCLR} – t_{CCHR}).

Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

Note 3: The values of t_{CCLW} and t_{CCLR} are specified during the overlapping period of $\overline{CS1}$ at “L” (CS2 = “H”) and the “L” levels of $\overline{WR}$ and $\overline{RD}$, respectively.

- System bus read/write characteristics 2 (68-series MPU)



(V_{DDA} = V_{DDL} = 4.5 to 5.5 V, V_{SSA} = V_{SSL} = 0 V, Tjop = –40 to +125°C)

Parameter		Symbol	Condition	Min.	Max.	Unit
Address hold time		t_{AH6}	—	10	—	ns
Address setup time		t_{AW6}		10	—	
System cycle time		t_{CYC6}	—	166	—	
Data setup time		t_{DS6}	—	30	—	
Data hold time		t_{DH6}		10	—	
Access time		t_{ACC6}	CL = 100 pF	—	30	
Output disable time		t_{OH6}		5	50	
Enable "H" pulse width	Read	t_{EWHR}	—	30	—	
	Write	t_{EWHW}		30	—	
Enable "L" pulse width	Read	t_{EWLR}	—	40	—	
	Write	t_{EWLW}		40	—	

(V_{DDA} = V_{DDL} = 2.7 to 4.5 V, V_{SSA} = V_{SSL} = 0 V, Tjop = –40 to +125°C)

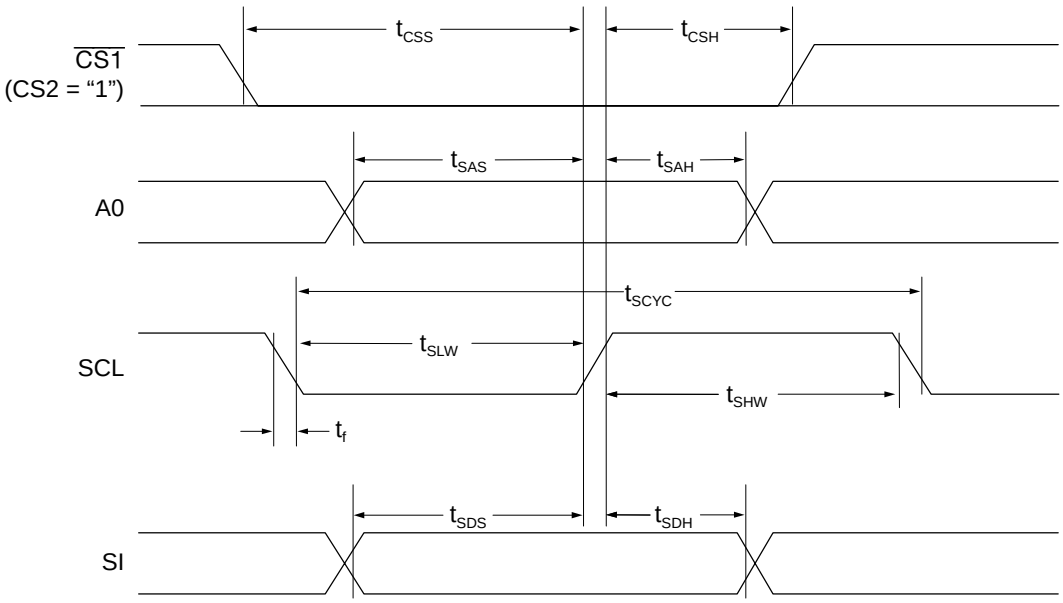
Parameter		Symbol	Condition	Min.	Max.	Unit
Address hold time		t_{AH6}	—	10	—	ns
Address setup time		t_{AW6}		10	—	
System cycle time		t_{CYC6}	—	400	—	
Data setup time		t_{DS6}	—	40	—	
Data hold time		t_{DH6}		15	—	
Access time		t_{ACC6}	CL = 100 pF	—	140	
Output disable time		t_{OH6}		10	100	
Enable “H” pulse width	Read	t_{EWHR}	—	120	—	
	Write	t_{EWHW}		60	—	
Enable “L” pulse width	Read	t_{EWLR}	—	60	—	
	Write	t_{EWLW}		60	—	

Note 1: The input signal rise and fall times are specified as 15 ns or less.
When using the system cycle time for fast speed, the specified values are (tr + tf) ≤ (t_{CYC6} – t_{EWLW} – t_{EWHW}) or (tr + tf) ≤ (t_{CYC6} – t_{EWLR} – t_{EWHR}).

Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

Note 3: The values of t_{EWLW} and t_{EWLR} are specified during the overlapping period of $\overline{CS1}$ at “L” (CS2 = “H”) and the “H” level of E.

- Serial interface



(V_{DDA} = V_{DDL} = 4.5 to 5.5 V, V_{SSA} = V_{SSL} = 0 V, Tjop = –40 to +125°C)

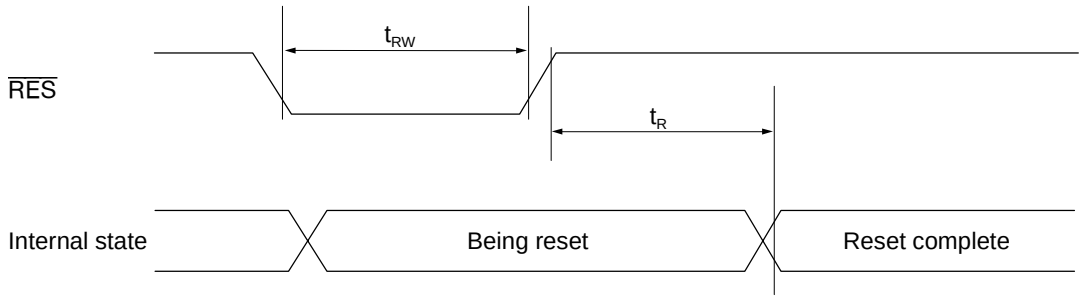
Parameter	Symbol	Condition	Min.	Max.	Unit
Serial clock period	t_{SCYC}		200	—	ns
SCL "H" pulse width	t_{SHW}		75	—	
SCL "L" pulse width	t_{SLW}		75	—	
Address setup time	t_{SAS}		50	—	
Address hold time	t_{SAH}		100	—	
Data setup time	t_{SDS}		50	—	
Data hold time	t_{SDH}		50	—	
CS–SCL Time	t_{CSS}		100	—	
	t_{CSH}		100	—	

(V_{DDA} = V_{DDL} = 2.7 to 4.5 V, V_{SSA} = V_{SSL} = 0 V, Tjop = –40 to +125°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Serial clock period	t_{SCYC}		250	—	ns
SCL “H” pulse width	t_{SHW}		100	—	
SCL “L” pulse width	t_{SLW}		100	—	
Address setup time	t_{SAS}		150	—	
Address hold time	t_{SAH}		150	—	
Data setup time	t_{SDS}		100	—	
Data hold time	t_{SDH}		100	—	
CS–SCL Time	t_{CSS}		150	—	
	t_{CSH}		150	—	

Note 1: The input signal rise and fall times are specified as 15 ns or less.
Note 2: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

- Reset input timing



(V_{DDA} = V_{DDL} = 4.5 to 5.5 V, V_{SSA} = V_{SSL} = 0 V, Tjop = –40 to +125°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time	t_R		—	—	0.5	ms
Reset “L” pulse width	t_{RW}		0.5	—	—	

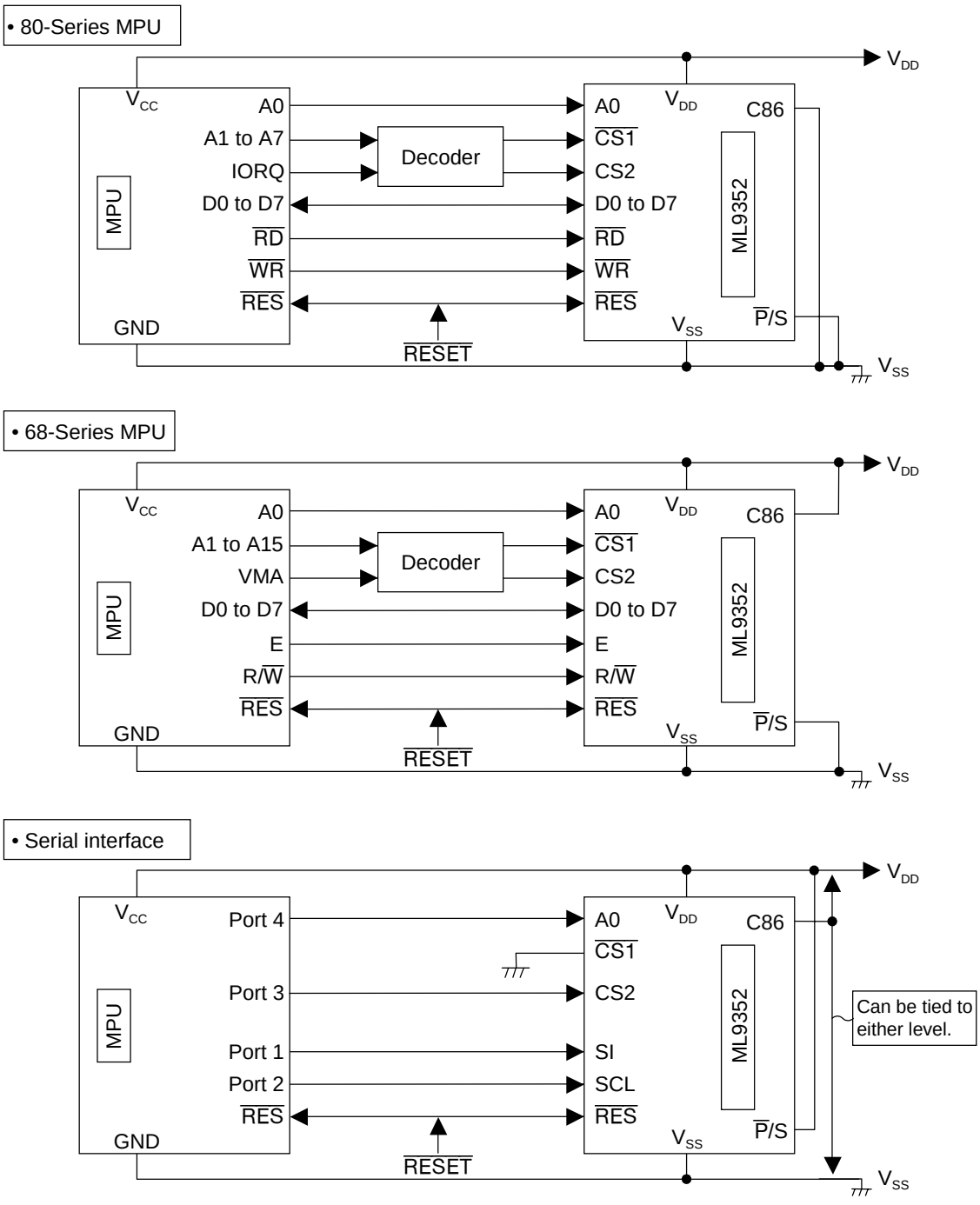
(V_{DDA} = V_{DDL} = 2.7 to 4.5 V, V_{SSA} = V_{SSL} = 0 V, Tjop = –40 to +125°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time	t_R		—	—	1	ms
Reset “L” pulse width	t_{RW}		1	—	—	

Note 1: All timings are specified taking the levels of 20% and 80% of V_{DD} as the reference.

MPU INTERFACE (Reference)

The ML9352 can be connected directly to the 80-series and 68-series MPUs.
Further, by using the serial interface, it is possible to operate the LSI with a minimum number of signal lines.



REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL9352-01	Dec. 27, 2002	–	–	Preliminary edition 1

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

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