OKI Semiconductor

FEDL9226-01
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ML9226

32-Bit Duplex/Triplex VFD Controller/Driver with Digital Dimming, ADC and Keyscan

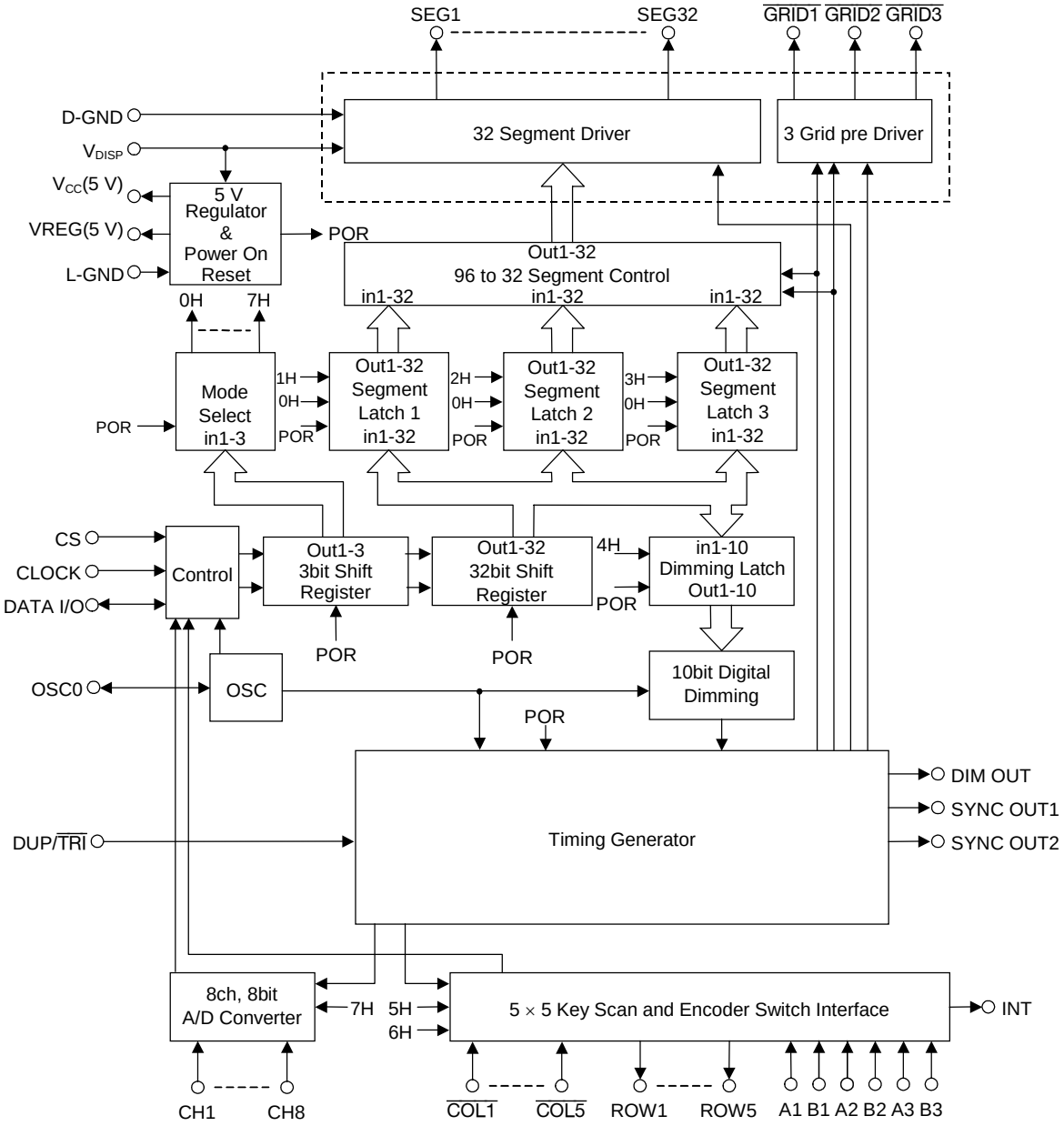
GENERAL DESCRIPTION

The ML9226 is a full CMOS controller/driver for Duplex or Triplex vacuum fluorescent display tube. It consttsts of 32-segment driver outputs and 3-grid pre-driver outputs, so that it can drive directly up to 96-segment VFD. ML9226 features a digital dimming function, a 8-ch ADC, a 5 × 5 keyscan circuit and an encoder type switch interface.
ML9226 provides an interface with a microcontroller only by four signal lines: DATA I/O, CLOCK, CS.

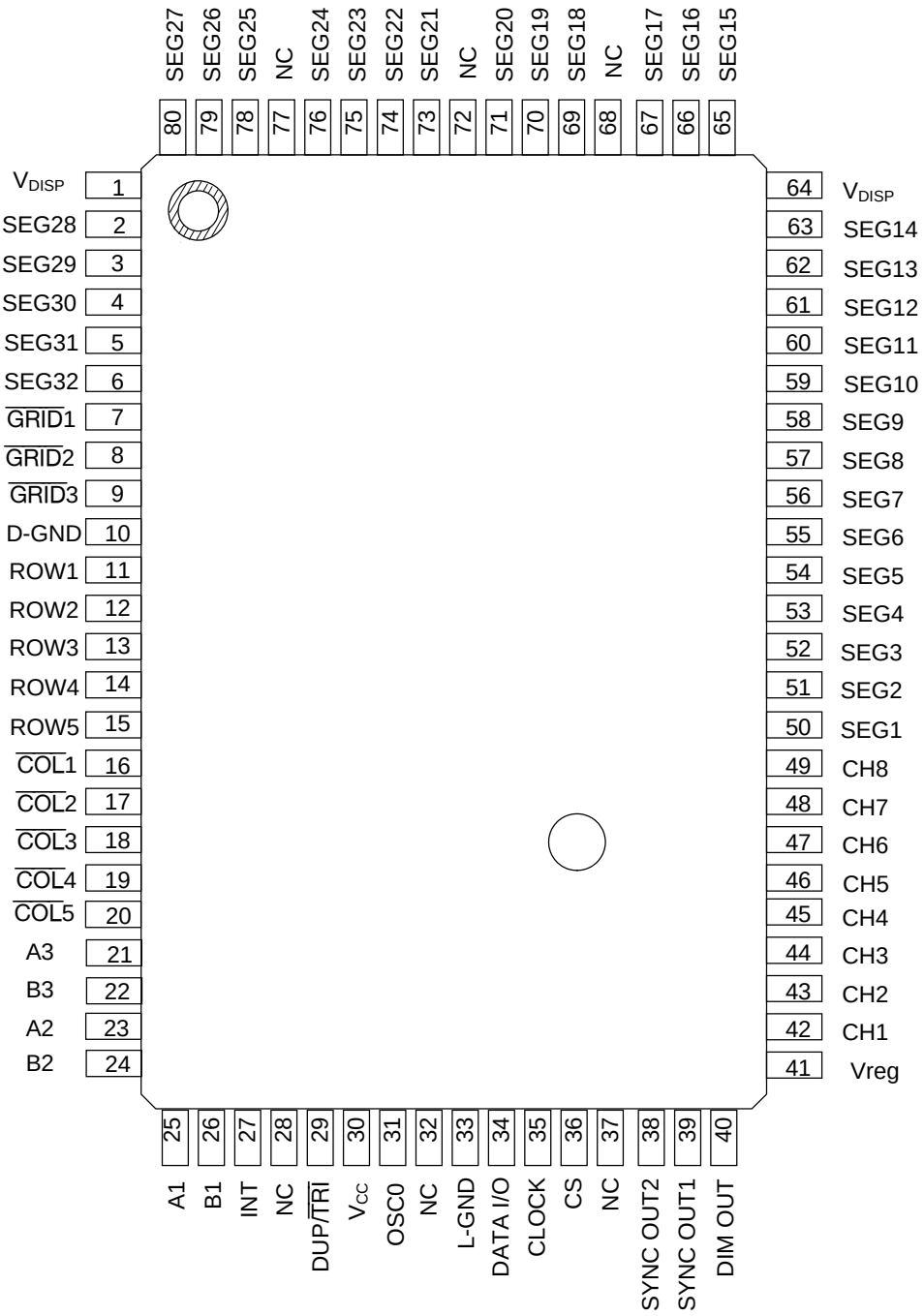
FEATURES

- Supply voltage (V_{DISP}) : 8 to 18.5V (Built-in 5V regulator for logic)
- Duplex/Triplex selectable
- Applicable VFD tube : 2 Grids × 32 Anodes VFD tube
  : 3 Grids × 32 Anodes VFD tube
- 32-segment driver outputs : I_{OH} = –5 mA at V_{OH} = V_{DISP} – 0.8 V (SEG1 to 22)
  I_{OH} = –10 mA at V_{OH} = V_{DISP} – 0.8 V (SEG23 to 32)
  I_{OL} = 500 uA at V_{OL} = 2.0 V (SEG1 to 32)
- 3-grid pre-driver outputs : I_{OH} = – 5.0 mA at V_{OH} = V_{DISP} – 0.8V
  I_{OL} = 10 mA at V_{OL} = 2.0V
- Built-in digital dimming circuit (10-bit resolution)
- Built-in 8-ch A/D converter
- Built-in 5 × 5 keyscan circuit
- 3 interface circuits for an encoder type rotary switch
- Built-in oscillation circuit (external R and C)
- Built-in Power-On-Reset circuit
- Package:
  80-pin plastic QFP (QFP80-P-1420-0.80-BK) (ML9226GA)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

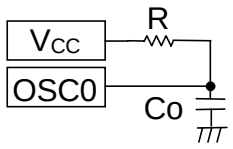


NC: No connection
(OPEN)

80-pin Plastic QFP

PIN DESCRIPTIONS

Pin	Symbol	Type	Description
1, 64	V_{DISP}	—	Power supply pins. Pin1 and pin64 should be connected externally.
10	D-GND	—	D-GND is ground pin for the VFD driver circuit. L-GND is ground pin for the logic circuit. Pins 10 and 33 should be connected externally.
33	L-GND	—	
30	V_{CC}	O	5 V output pin for internal logic portion and external logic circuit.
41	V_{REG}	O	Reference voltage (5 V) output pin for A/D converter.
50 to 63, 65 to 67, 69 to 71, 73, 74	SEG1 to 22	O	Segment (anode) signal output pins for a VFD tube. These pins can be directly connected to the VFD tube. External circuit is not required. $I_{OH} \leq -5$ mA
75, 76, 78 to 80, 2 to 6	SEG23 to 32	O	Segment (anode) signal output pins for a VFD tube. These pins can be directly connected to the VFD tube. External circuit is not required. $I_{OH} \leq -10$ mA
7, 8, 9	$\overline{GRID1}$ to $\overline{3}$	O	Inverted Grid signal output pins. For pre-driver, the external circuit is requiend. $I_{OL} \leq 10$ mA
36	CS	I	Chip Select input pin. Data input/output operation is valid when this pin is set at a High level.
35	CLOCK	I	Serial clock input pin. Data is input and/or output through the DATA I/O pin at the rising edge of the serial clock.
34	DATA I/O	I/O	Serial data input/output pin. Data is input to/comes out from the shift register at the rising edge of the serial clock.
27	INT	O	Interrupt signal output to microcontroller. When any key of key matrix is pressed or released, key scanning is started. After the completion of the one cycle, this pin goes to high level and keeps the high level until keyscan stop mode is selected.
29	DUP/$\overline{TRI}$	I	Duplex/Triplex operation select input pin. Duplex (1/2 duty) operation is selected when this pin is set at a V_{CC} level. Triplex (1/3 duty) operation is selected when this pin is set at a GND level.
42 to 49	CH1 to 8	I	Analog voltage input pin for the 8-bit A/D converter.
21 to 26	A1 to A3 B1 to B3	I	Input pin for the encoder type rotary switch. The phase of an An/Bn input is detected.
16 to 20	$\overline{COL1}$ to $\overline{5}$	I	Return inputs from the key matrix. These pins are active low. When key matrix are in the inactive sate, these pins are at high level through the internal pull-up resistors. All the inputs do not have the cahttering absorption function for the keyscans.
11 to 15	ROW1 to 5	O	Key switch scanning outputs. Normally low level is output through these pin. When any switch of key matrix is depressed or released, key scanning is started and is continued until keyscan stop mode is selected. When keyscan stop mode is selected, all outputs of ROW1 to 5 go back to low level.

Pin	Symbol	Type	Description
40	DIM OUT	O	Dimming pulse output. Connect this pin to the slave side DIM IN pin.
38, 39	SYNC OUT 1, 2	O	Synchronous signal input. Connect these pins to the SYNC IN1 and SYNC IN2 pins of a slave side.
31	OSC0	I/O	RC oscillator connecting pins. Oscillation frequency depends on display tubes to be used. For details refer to ELECTRICAL CHARACTERISTICS. 
28,32, 37,68, 72,77	NC	-	OPEN pins.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition		Rating	Unit
Supply Voltage	V_{DISP}	—		–0.3 to +20	V
Input Voltage	V_{IN}	—		–0.3 to +6.0	V
Power Dissipation	P_D	Ta = 85°C	QFP80-P-1420-0.80-BK	263	mW
Storage Temperature	T_{STG}	—		–55 to +150	°C
Output Current	I_{O1}	SEG1 to 22		–10.0 to +2.0	mA
	I_{O2}	SEG23 to 32		–20.0 to +2.0	mA
	I_{O3}	$\overline{GRID1}$ to $\overline{3}$		–10.0 to +20.0	mA
	I_{O4}	DIM OUT, SYNC OUT1, SYNC OUT2		–2.0 to +2.0	mA

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Driver Supply Voltage	V_{DISP}	—		8.0	13.0	18.5	V
High Level Input Voltage	V_{IH}	All inputs except OSC0		3.8	—	—	V
Low Level Input Voltage	V_{IL}	All inputs except OSC0		—	—	0.8	V
Clock Frequency	f_C	—		—	—	2.0	MHz
Oscillation Frequency	f_{OSC}	R = 10 kΩ ±5%, Co = 27 pF ±5%		2.2	3.3	4.4	MHz
Frame Frequency	f_{FR}	R = 10 kΩ ±5% Co = 27 pF ±5%	1/3 Duty	179	269	358	Hz
			1/2 Duty	268	403	538	Hz
Operating Temperature	T_{OP}	—		–40	—	+85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = –40 to +85°C, V_{DISP} = 8.0 to 18.5 V)

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	*1)	—		3.8	—	V
Low Level Input Voltage	V_{IL}	*1)	—		—	0.8	V
High Level Input Current	I_{IH1}	*2)	V_{IH} = 3.8 V		–5.0	+5.0	µA
	I_{IH2}	*3)	V_{IH} = 3.8 V		–70	–5.0	µA
Low Level Input Current	I_{IL1}	*2)	V_{IL} = 0.0 V		–5.0	+5.0	µA
	I_{IL2}	*3)	V_{IL} = 0.0 V		–160	–10	µA
High Level Output Voltage	V_{OH1}	SEG1 to 22	V_{DISP} = 9.5 V	I_{OH1} = –5 mA	V_{DISP} – 0.8	—	V
	V_{OH2}	SEG23 to 32		I_{OH2} = –10 mA	V_{DISP} – 0.8	—	V
	V_{OH3}	$\overline{GRID1}$ to $\overline{3}$		I_{OH3} = –5 mA	V_{DISP} – 0.8	—	V
	V_{OH4}	*4)		I_{OH4} = –200 µA	4.0	—	V
				Output Open	4.5	—	V
Low Level Output Voltage	V_{OL1}	SEG1 to 22	V_{DISP} = 9.5 V	I_{OL1} = 500 µA	—	2.0	V
	V_{OL2}	SEG23 to 32		I_{OL2} = 500 µA	—	2.0	V
	V_{OL3}	$\overline{GRID1}$ to $\overline{3}$		I_{OL3} = 10 mA	—	2.0	V
	V_{OL4}	*5)		I_{OL4} = 300 µA	—	0.4	V
Supply Current	I_{DISP}	V_{DISP}	R = 10 kΩ ±5%, Co = 27 pF ±5% no load		—	10	mA
Supply Voltage for Logic	V_L	V_{CC}	C = 0.01 µF ± 10%, I_O = 0 to –10 mA		4.5	5.5	V

*1) CS, CLOCK, DATA I/O DUP/$\overline{TRI}$, A1 to A3, B1 to B3, $\overline{COL1}$ to $\overline{5}$
*2) CS, CLOCK, DATA I/O DUP/$\overline{TRI}$, A1 to A3, B1 to B3
*3) $\overline{COL1}$ to $\overline{5}$
*4) DATA I/O, INT, DIM OUT, SYNC OUT1, SYNC OUT2
*5) DATA I/O, INT, DIM OUT, SYNC OUT1, SYNC OUT2, ROW1 to 5

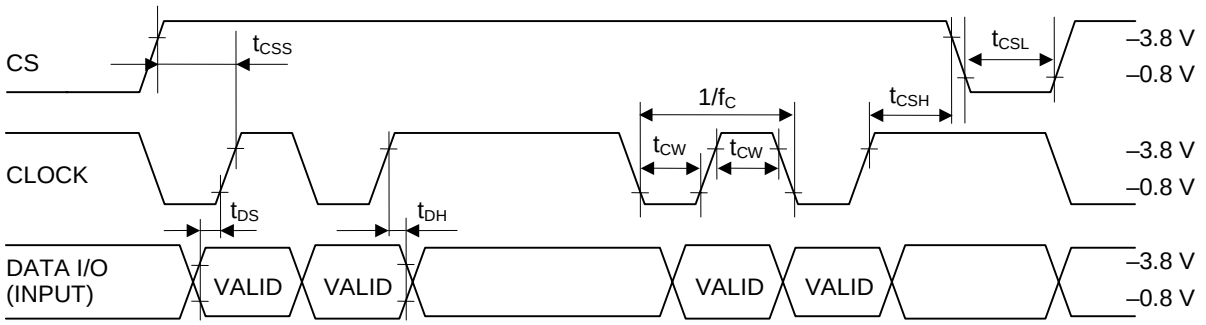
AC Characteristics

(Ta = –40 to +85°C, V_{DISP} = 8.0 to 18.5 V)

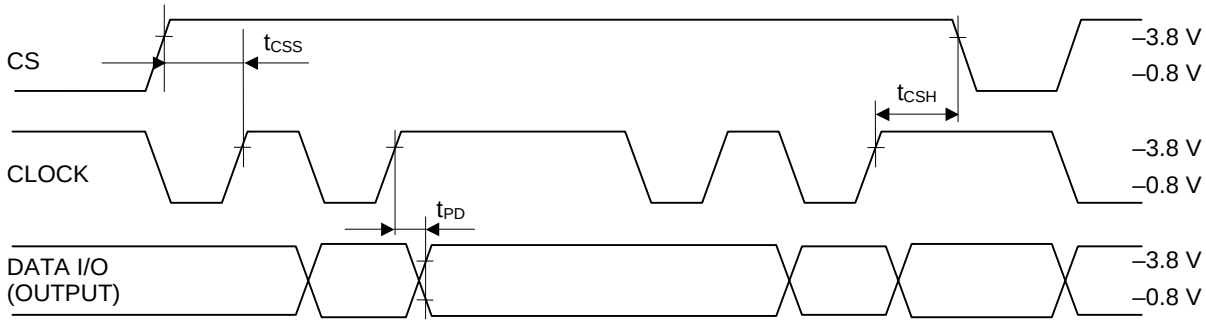
Parameter	Symbol	Condition		Min.	Max.	Unit
Clock Frequency	f_C	—		—	2.0	MHz
Clock Pulse Width	t_{CW}	—		200	—	ns
Data Setup Time	t_{DS}	—		200	—	ns
Data Hold Time	t_{DH}	—		200	—	ns
CS Off Time	t_{CSL}	R = 10 kΩ ±5%, Co = 27 pF ±5%		20	—	μs
CS Setup Time (CS-Clock)	t_{CSS}	—		200	—	ns
CS Hold Time (Clock-CS)	t_{CSH}	—		200	—	ns
DATA Output Delay Time (Clock-DATA I/O)	t_{PD}	—		—	1.0	μs
Output Slew Rate Time	t_R	C_L= 100 pF	t_R = 20% to 80%	—	2.0	μs
	t_F		t_F = 80% to 20%	—	2.0	μs
V_{DISP} Rise Time	t_{PRZ}	Mounted in a unit		—	100	μs
V_{DISP} Off Time	t_{POF}	Mounted in a unit, V_{DISP} = 0.0 V		5.0	—	ms
CS Wait Time	t_{RSOFF}	—		400	—	μs

TIMING DIAGRAM

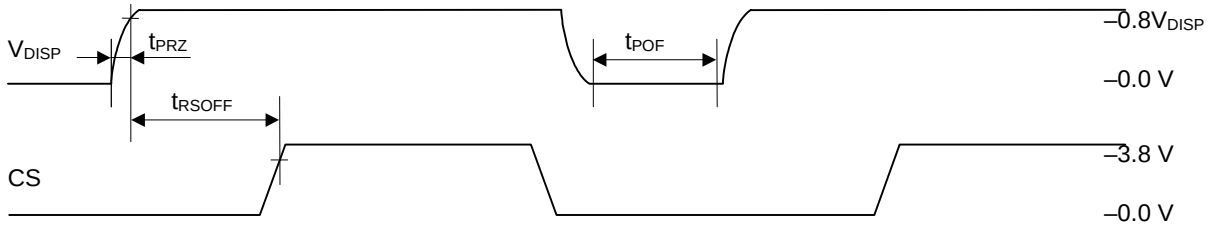
Data Input Timing



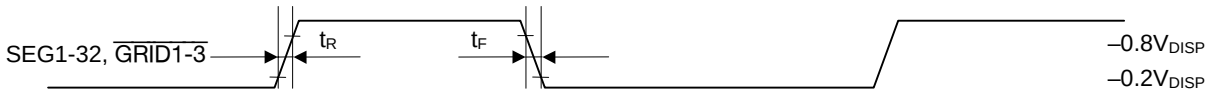
Data Output Timing



Reset Timing



Driver Output Timing



A/D Converter Characteristics

(Ta = –40 to +85°C, V_{DISP} = 8.0 to 18.5 V)

Parameter	Condition	Min.	Typ.	Max.	Unit
Reference Voltage (V_{REG})	—	4.5	5.0	5.5	V
Output Current	—	—	—	–10	mA
Input Voltage Range	—	GND	—	V_{REG}	V
Conversion Time/Channel	R = 10 kΩ ±5%, C2 = 27 pF ±5%	256	310	394	µs
Resolution		—	—	8	bit
Linearity error		—	—	±2.0	LSB
Differentiation linearity error		—	—	±2.0	LSB
Zero scale error		—	—	+2.0	LSB
Full-scale error		—	—	-2.0	LSB

Terminological definition

Resolution → The minimum input analog value which can be recognized. It can decompose into 2^8= 256,(V_{RH}-V_{RL})/256,in 8 bits.

Linearity error → The deviation between the ideal conversion characteristic as a 8-bit A/D converter and the actual conversion characteristic is said. (Therefore, a quantization error is not included.) The ideal conversion characteristic means the step which divided the voltage between V_{RH} to V_{RL} into 256 division into equal parts.

Differentiation linearity error → The smoothness of the conversion characteristic is shown, and ideally, the width of the analog input voltage corresponding to change for 1 bit of digital outputs is 1LSB= (V_{RH}-V_{RL})/256, and says the deviation of this ideal bit size and the bit size in the arbitrary points of the conversion range.

Zero scale error → Digital output "000H" to "001H" changes, and the deviation of the ideal conversion characteristic of a point and the actual conversion characteristic is said.

Full scale error → Digital output "0FEH" to "0FFH" changes, and the deviation of the ideal conversion characteristic of a point and the actual conversion characteristic is said.

Keyscan Characteristics

(Ta = –40 to +85°C, V_{DISP} = 8.0 to 18.5 V)

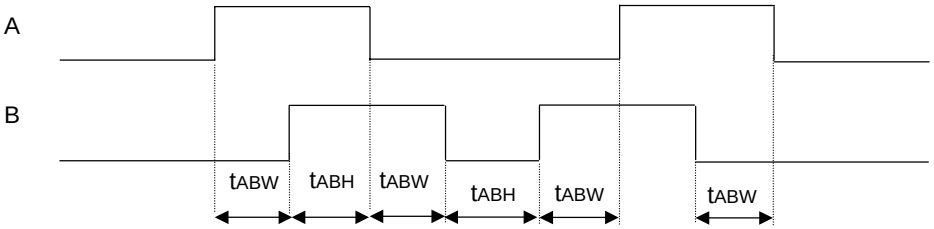
Parameter	Condition	Min.	Typ.	Max.	Unit
Keyscan Cycle Time	R = 10 kΩ ±5%, Co = 27 pF ±5%	160	194	246	µs
Keyscan Pulse Width	R = 10 kΩ ±5%, Co = 27 pF ±5%	32	39	49	µs

Rotary switch characteristic

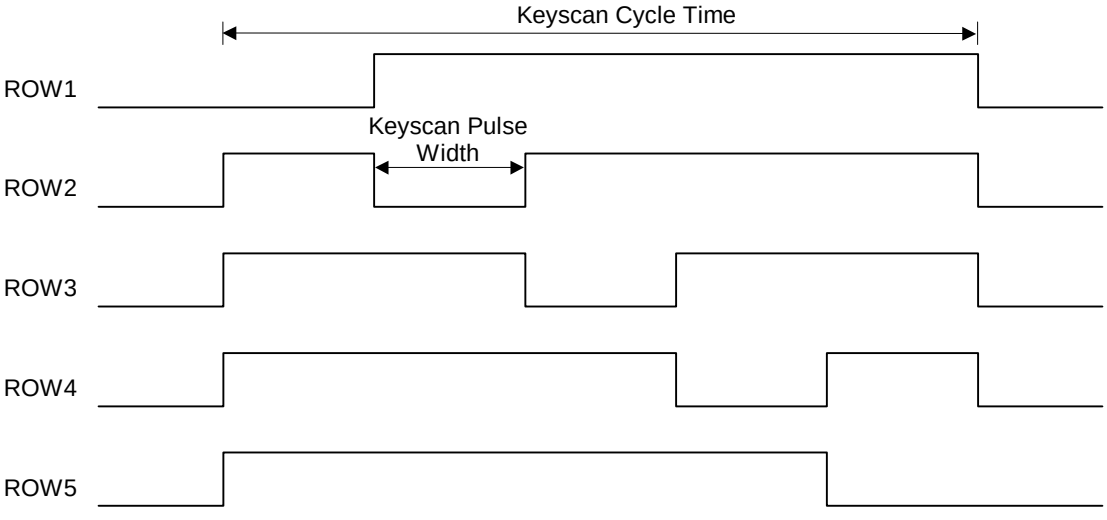
(Ta = –40 to +85°C, V_{DISP} = 8.0 to 18.5 V)

Parameter	Sign	Condition	Min.	Typ.	Max.	Unit
Phase input time	t_{ABW}	R = 10 kΩ ±5%, C_O = 27 pF ±5%	950	—	—	µs
Phase input fixed time	t_{ABH}					

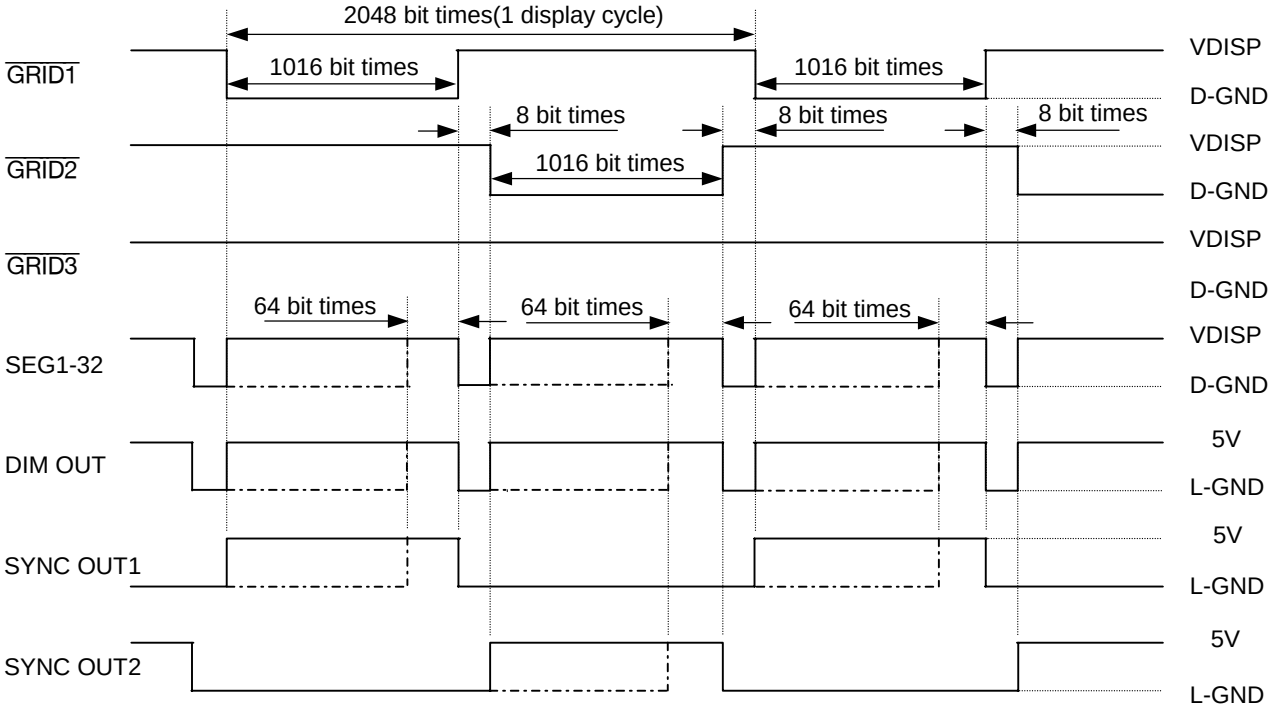
Rotary switch input timing



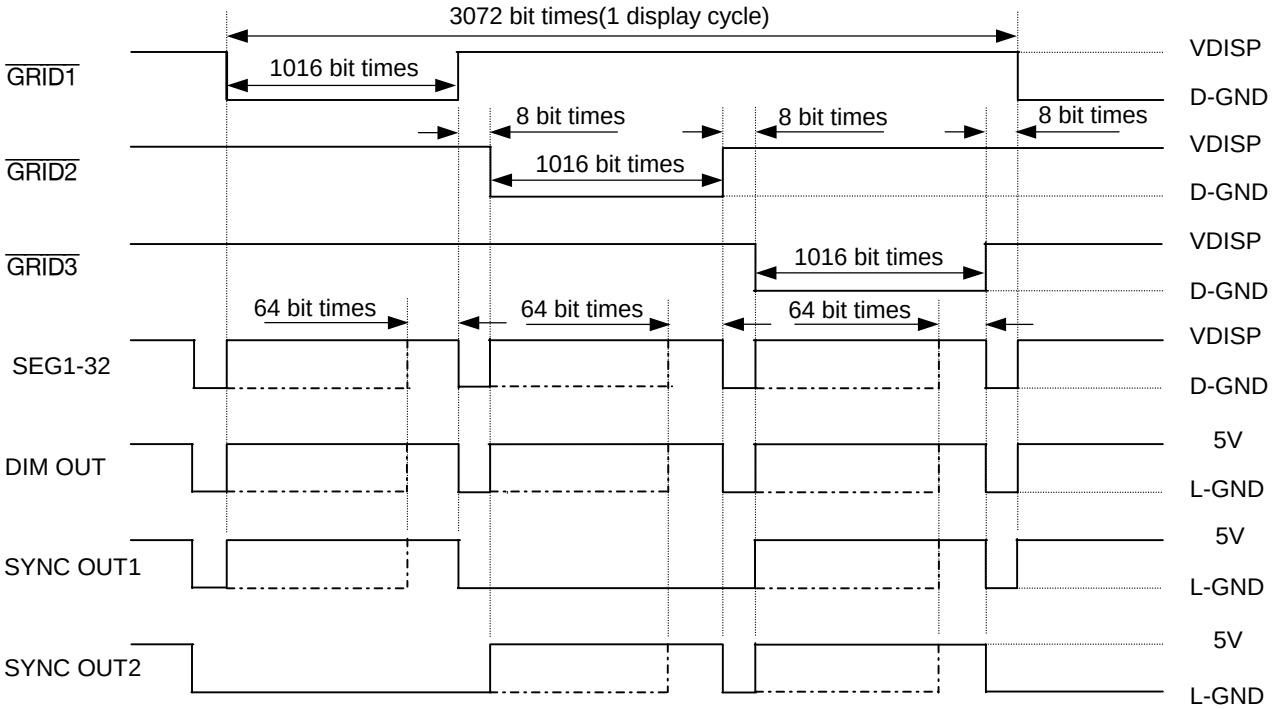
Keyscan Timing



Output Timing (Duplex Operation) *1 bit time = $4/f_{OSC}$
Solid line : The dimming data is 1016/1024
Dotted line : The dimming data is 64/1024



Output Timing (Triplex Operation) *1 bit time = $4/f_{OSC}$
Solid line : The dimming data is 1016/1024
Dotted line : The dimming data is 64/1024



FUNCTIONAL DESCRIPTION

Power-on Reset

When power is turned on, ML9226 is initialized by the internal power-on reset circuit.
The status of the internal circuit after initialization is as follows:

- The contents of the shift registers and latches are set to "0".
- The digital dimming duty cycle is set to "0".
- All segment outputs are set to Low level.
- $\overline{\text{GRID1}}$ outputs are set to Low level.
- $\overline{\text{GRID2}}$ to $\overline{3}$ outputs are set to High level.
- All the ROW outputs are set to Low level.
- INT output is set to Low level.

Mode Data

ML9226 has the seven function modes. The function mode is selected by the mode data (M0 to M2). The relation between function mode and mode data (M0 to M2) is as follows:

FUNCTION MODE	OPERATING MODE	FUNCTION DATA		
		M0	M1	M2
0	Segment Data for $\overline{\text{GRID1-3}}$ Input	0	0	0
1	Segment Data for $\overline{\text{GRID1}}$ Input	1	0	0
2	Segment Data for $\overline{\text{GRID2}}$ Input	0	1	0
3	Segment Data for $\overline{\text{GRID3}}$ Input	1	1	0
4	Digital Dimming Data Input	0	0	1
5	Keyscan Stop	1	0	1
6	Switch Data Output	0	1	1
7	A/D Data Output	1	1	1

Data Input and Output

Data input and output through the DATA I/O pin is valid only when the CS pin is set at a High level.
The input data to DATA I/O pin is shifted into the shift register at the rising edge of the serial clock. The data is automatically loaded to the latches when the CS pin is set at a Low level.
10-bit dimming data (D1 to D10) and 32-bit segment data (S1 to S32) are used for inputting of dimming data and display data. To transfer these two data, the mode data (M0 to M2) must be sent after each of these data succeddingly.
The output data from the DATA I/O pin is output from the shift register at the rising edge of the serial clock.
ML9226 outputs 64-bit (8 ch × 8 bits) A/D data (A11 to A88) and 37-bit key data (S11 to S55, R1, Q11 to Q13, R2, Q21 to Q23, R3 and Q31 to Q33). To receive these data, the mode data (M0 to M2) mast be sent first and then CS must be set once to Low level and set again to High level.
Then inputting serial clocks, these data are output from the DATA I/O pin.
When the CS pin is set at a Low level, the DATA I/O pin returns to an input pin.
To stop the keyscan, the only mode data (M0 to M2) must be sent. After the mode data transfer, the key scanning is stopped immediately.

Segment Data Input [Function Mode: 0 to 3]

- ML9226 receives the segment data when function mode 0 to 3 are selected.
- The same segment data is transferred to the 3 segment data latch correspond to $\overline{GRID1}$ to $\overline{3}$ at the same time when the function mode 0 is selected.
- The segment data is transferred to only one segment data latch that is selected by mode data, when the function mode is 1, 2 or 3 is selected.
- Segment output (SEG1 to 32) becomes High level when the segment data (S1 to 32) is High level.

[Data Format]

Input Data : 35 bits
Segment Data : 32 bits
Mode Data : 3 bits

Bit	1	2	3	4	------	29	30	31	32	33	34	35
Input Data	S1	S2	S3	S4	------	S29	S30	S31	S32	M0	M1	M2

LSB ◄——— Segment Data (32 bits) ———► MSB ◄— Mode Data (3 bits) —►

[Bit correspondence between segment output and segment data]

SEG n	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Segment data	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16
SEG n	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Segment data	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30	S31	S32

Digital Dimming Data Input [Function Mode: 4]

- ML9226 receives the digital dimming data when function mode 4 is selected.
- The output duty changes in the range of 0/1024 (0%) to 1016/1024 (99.2%) for each grid.
- The 10-bit digital dimming data is input from LSB.

[Data Format]

Input Data : 13 bits
Digital Dimming Data : 10 bits
Mode Data : 3 bits

Bit	1	2	3	4	5	6	7	8	9	10	11	12	13
Input Data	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	M0	M1	M2
	LSB ← Digital Dimming Data (10 bits) → MSB										← Mode Data (3 bits) →		

(LSB) Dimming Data (MSB)										Duty Cycle
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	
0	0	0	0	0	0	0	0	0	0	0/1024
1	0	0	0	0	0	0	0	0	0	1/1024
				⋮						⋮
1	1	1	0	1	1	1	1	1	1	1015/1024
0	0	0	1	1	1	1	1	1	1	1016/1024
1	0	0	1	1	1	1	1	1	1	1016/1024
				⋮						⋮
1	1	1	1	1	1	1	1	1	1	1016/1024

Keyscan Stop [Function Mode: 5]

- ML9226 stops a key scanning when function mode 5 are selected.
- To select this mode, the only mode data (M0 to M2) is needed.
- The actual time lag range between receipt of the keyscan stop command and the ceasing of scanning is 2.4 μs to 3.6 μs

[Input Data Format]

Input Data : 3 bits
Mode Data : 3 bits

Bit	28	29	30
Input Data	M0	M1	M2
	← Mode Data (3 bits) →		

Switch Data Output [Function Mode: 6]

- ML9226 output the switch data when function mode 6 is selected.
- To select this mode, the only mode data (M0 to M2) is needed.
- When ML9226 recieves this mode, the DATA I/O pin is changed to an output pin.
- 37-bit switch data come out from the DATA I/O pin synchronizing with the rise edge of the clock.
- When the CS pin is set at the low level, the DATA I/O pin returns to an input pin.
- R1, R2, R3 = 0, implies Right rotation of the knob (Clockwise)
- R1, R2, R3 = 1, implies Left rotation of the knob (Counter Clockwise)
- Contact Count bits are Q11 (LSB) to Q13 (MSB), Q21 (LSB) to Q23 (MSB) and Q31 (LSB) to Q33 (MSB)

[Input Data Format]

Input Data : 3 bits
Mode Data : 3 bits

Bit	28	29	30
Input Data	M0	M1	M2

Mode Data (3 bits)

[Output Data Format]

Output Data : 37 bits
5 × 5 push swithc Data : 25 bits
Encoder switch Data : 12 bits

Bit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
Output Data	S11	S12	S13	S14	S15	S21	S22	S23	S24	S25	S31	S32	S33	S34	S35	S41	S42	S43	S44	S45	S51	S52	S53	S54	S55

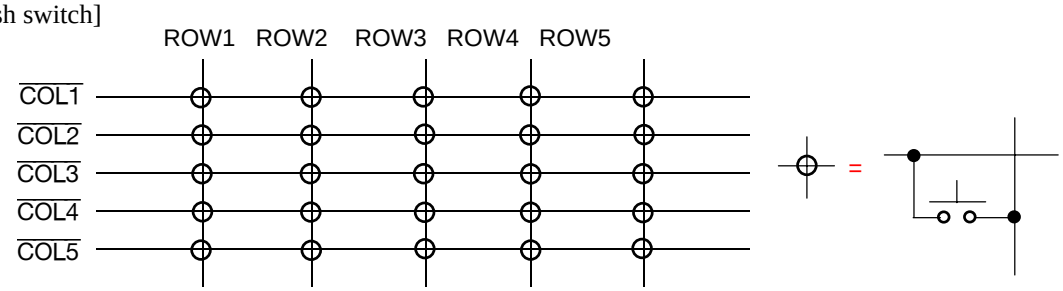
Bit	26	27	28	29	30	31	32	33	34	35	36	37
Output Data	R1	Q11	Q12	Q13	R2	Q21	Q22	Q23	R3	Q31	Q32	Q33

Sij: i = ROW1 to 5, j = $\overline{\text{COL1}}$ to $\overline{5}$

Sij = 1: Switch ON

Sij = 0: Switch OFF

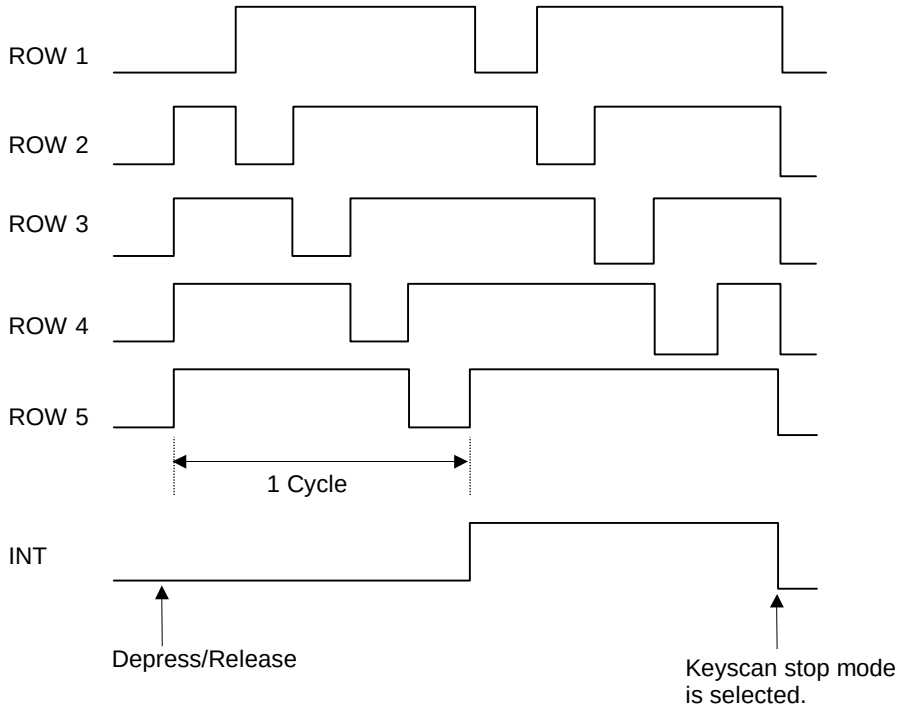
[5x5 Push switch]



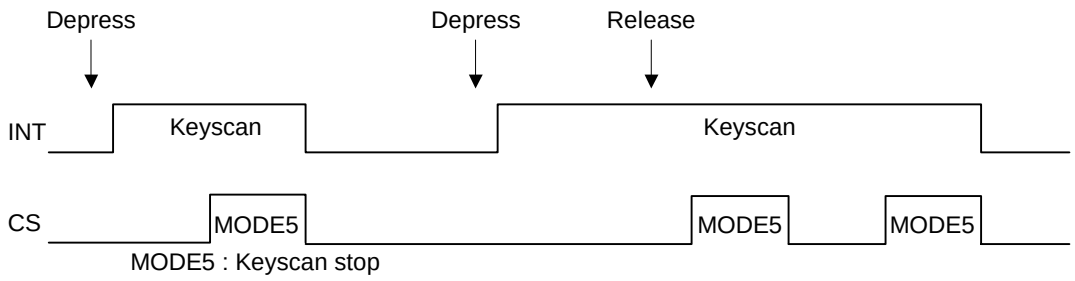
Keyscan

Keyscanning is started only when depression or release of any key is detected in order to minimize noise caused by scanning signal. Then, keyscanning is continued until the keyscan stop mode is sent from a microcomputer. The INT pin goes to the high level at the completion of 1-cycle scanning after the keyscan start, so the (high level) signal sent from the INT pin can be used as an interrupt signal.

[Keyscan Timing]



Note: Keyscanning cannot be stopped by selecting the keyscan stop mode only once if:
- keyscanning is started after depression or release of any key is detected, and then
- a key is depressed or released again before the keyscan stop mode is selected.
To stop keyscanning, it is required to select the keyscan stop mode once again.



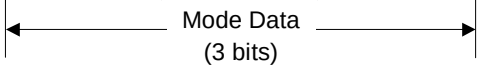
A/D Data Output [Function Mode: 7]

- ML9226 output the A/D data when function mode 7 is selected.
- To select this mode, the only mode data (M0 to M2) is needed.
- When ML9226 recieves this mode, the DATA I/O pin is changed to an output pin.
- 64-bit A/D data come out from the DATA I/O pin synchronizeing with the rise edge of the clock.
- When the CS pin is set at the low level, the DATA I/O pin returns to an input pin.

[Input Data Format]

Input Data : 3 bits
Mode Data : 3 bits

Bit	28	29	30
Input Data	M0	M1	M2



[Output Data Format]

Output Data : 64 bits
A/D Data : 64 bits

Bit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Output Data	A11 (LSB)	A12	A13	A14	A15	A16	A17	A18 (MSB)	A21 (LSB)	A22	A23	A24	A25	A26	A27	A28 (MSB)
A/D	CH1								CH2							
Bit	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Output Data	A31 (LSB)	A32	A33	A34	A35	A36	A37	A38 (MSB)	A41 (LSB)	A42	A43	A44	A45	A46	A47	A48 (MSB)
A/D	CH3								CH4							
Bit	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
Output Data	A51 (LSB)	A52	A53	A54	A55	A56	A57	A58 (MSB)	A61 (LSB)	A62	A63	A64	A65	A66	A67	A68 (MSB)
A/D	CH5								CH6							
Bit	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
Output Data	A71 (LSB)	A72	A73	A74	A75	A76	A77	A78 (MSB)	A81 (LSB)	A82	A83	A84	A85	A86	A87	A88 (MSB)
A/D	CH7								CH8							

The rotary encoder switch function.

As figure 1 shows, the rotary encoder switch circuit is consisted of Phase detection, Interrupt generation, Up/down counter, Direction latch and Parallel-in serial-out shift register.

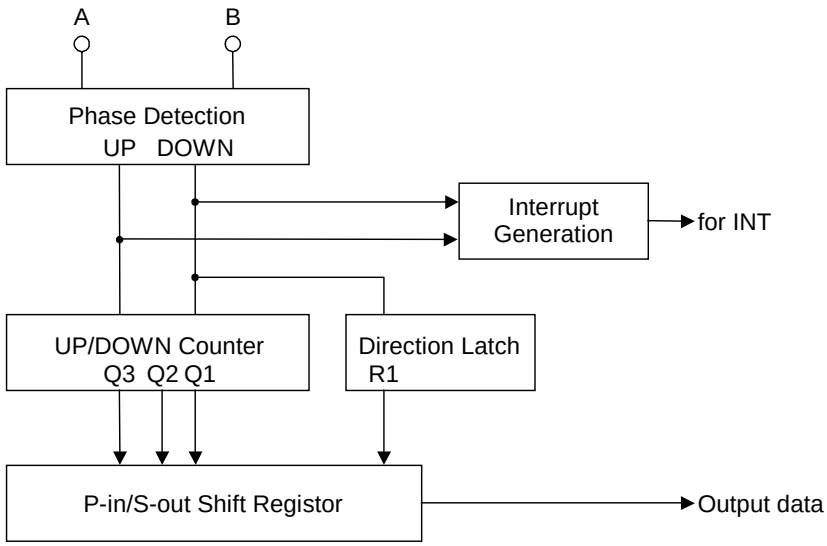


Fig.1 The Rotary Encoder Switch Circuit

1) Phase detection

1-1) Clockwise

When signal A and B input as fig. 2, the phase detection circuit outputs UP signal after the chattering absorption period. At this time, the output INT also goes to high level, so this signal can be used as an interrupt. The INT stays High level until the key scan stop mode is selected.

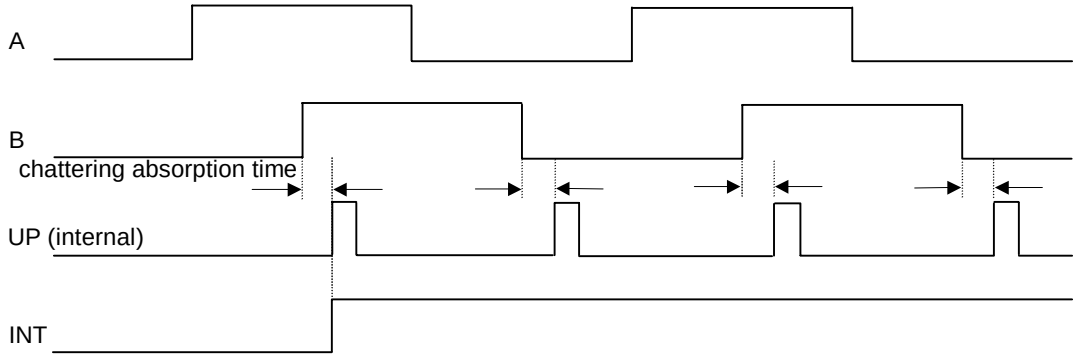


Fig.2 The Input and Output Timing in Case of Clockwise.

1-2) counter clockwise

When signal A and B input as fig. 3, the phase detection circuit outputs Down signal after the chattering absorption period. At this time, the output INT also goes to High level. The INT stays High level until the key scan stop mode is selected.

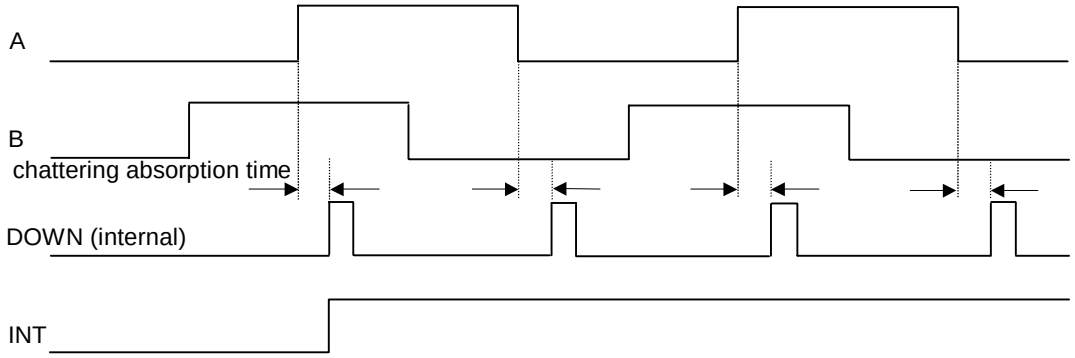


Fig.3 The Input and Output Timing in Case of Counter Clockwise.

2) UP/DOWN COUNTER

When the UP/DOWN COUNTER is input UP, it counts up and when it is input DOWN, it counts down. But if overcounte of "111" occurs the UP/DOWN COUNTER stays "111".

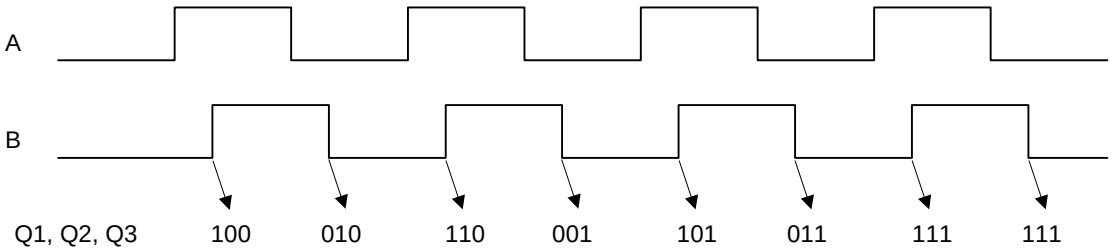


Fig.4

3) Direction latch

When the Direction latch is input DOWN the output R goes "1". But if the UP pulse is input and the counts value change to plus value, the output R goes to "0".

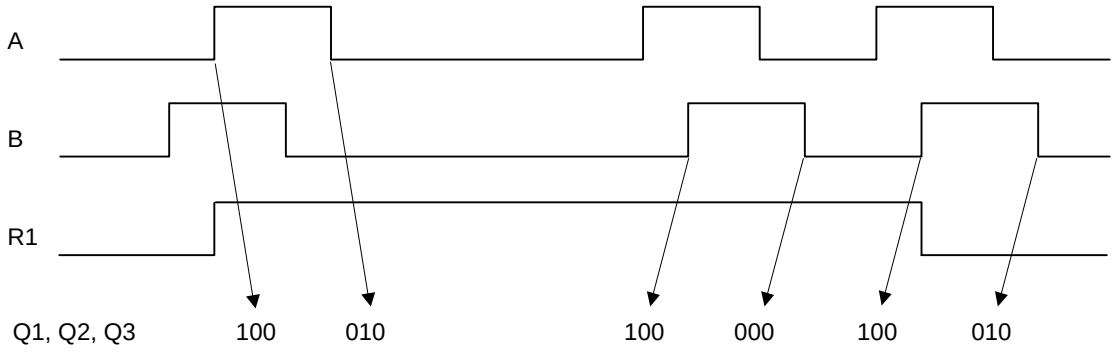


Fig.5

4) P-in/S-out shift resistor

When the key scan stop mode is selected and SC goes L, INT signal goes “L”.

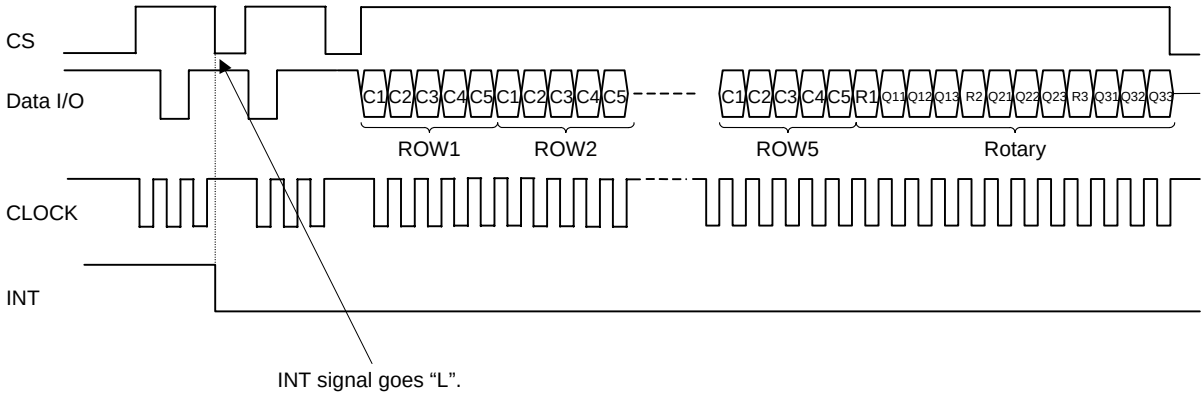
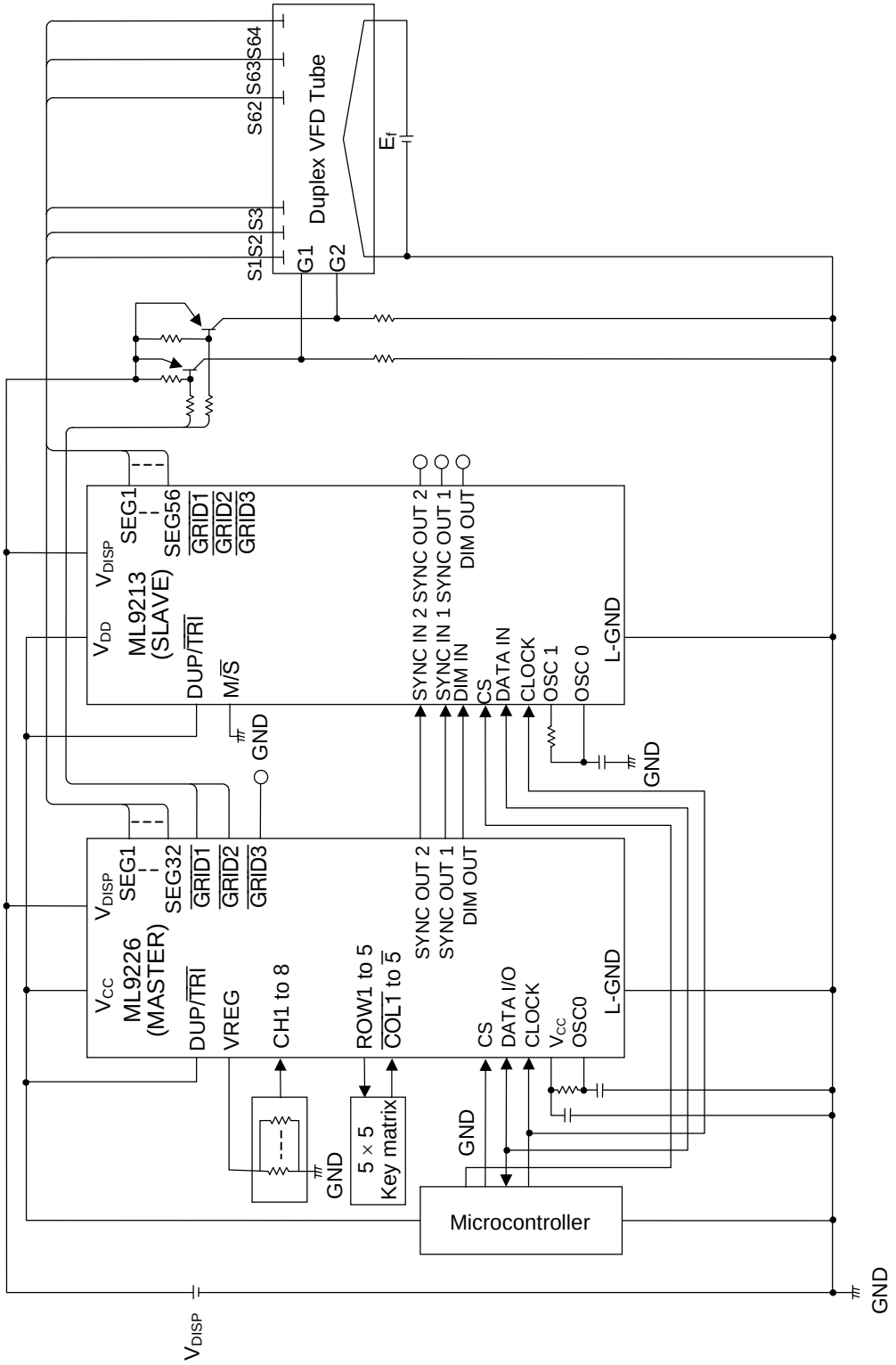


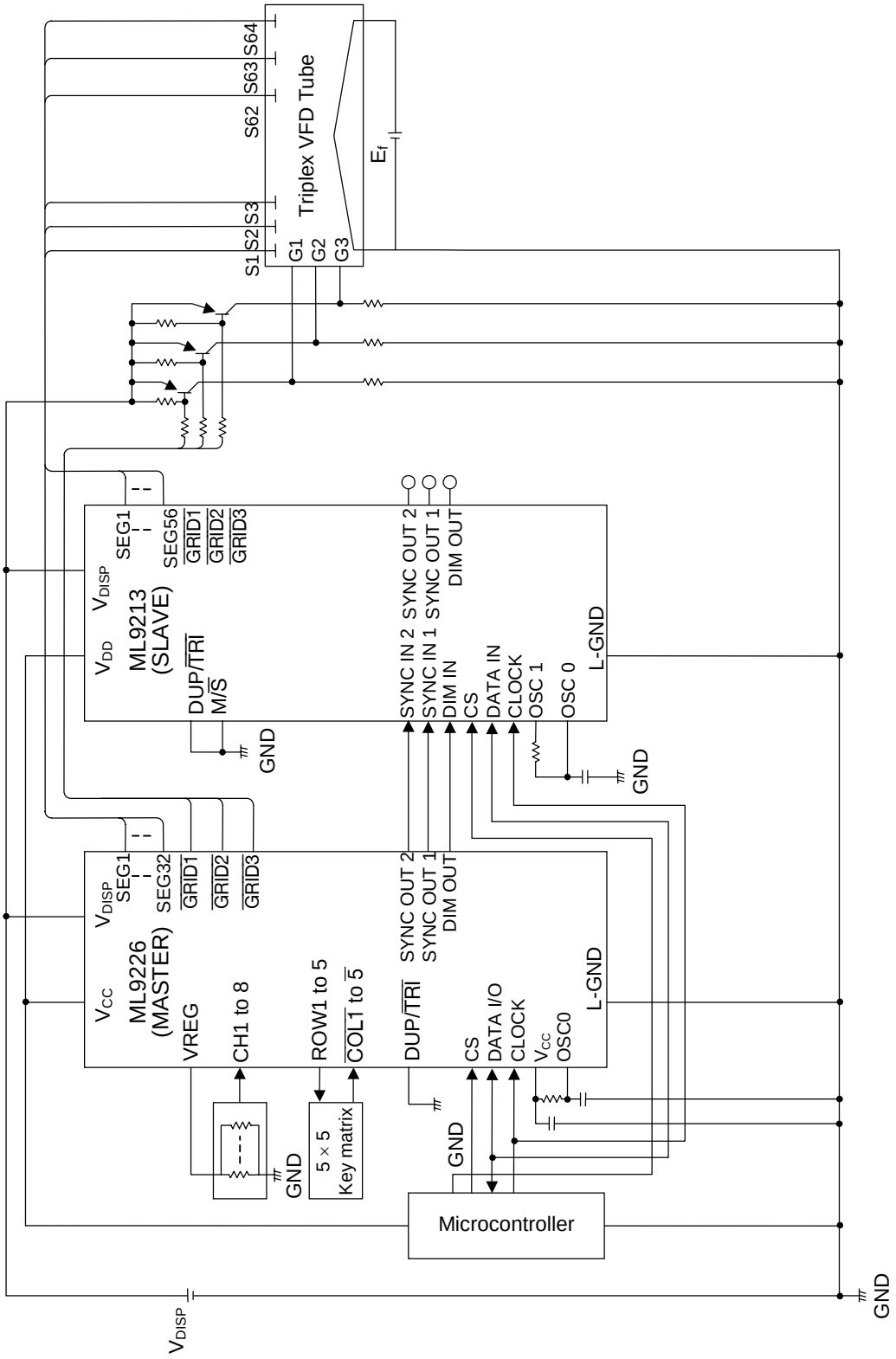
Fig.6

APPLICATION CIRCUITS

1. Circuit for the duplex VFD tube with 128 segments (2 Grid × 64 Anode)



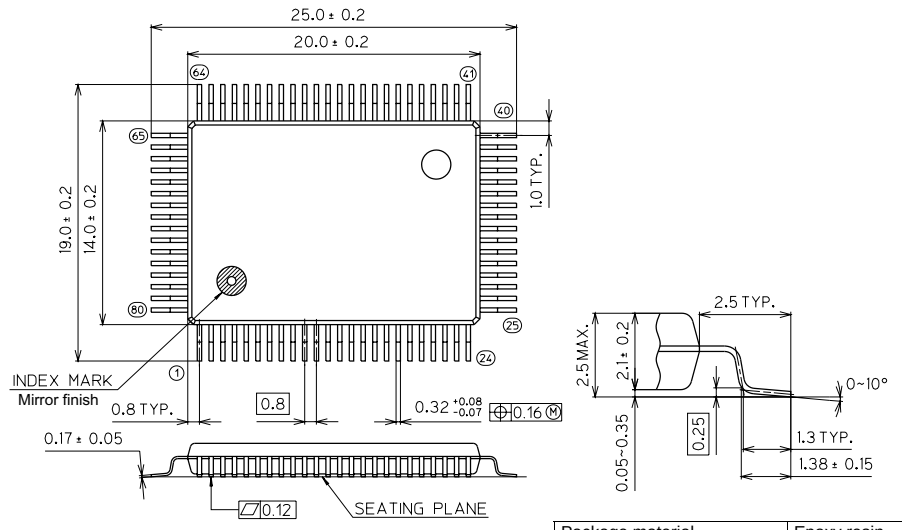
2. Circuit for the triplex VFD tube with 192 segments (3 Grid × 64 Anode)



PACKAGE DIMENSIONS

(Unit: mm)

QFP80-P-1420-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	1.27 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL9226-01	Dec. 11, 2002	–	–	Preliminary edition 1

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