PEDL9041A-02
Issue Date: Mar. 15, 2002

OKI Semiconductor

ML9041A-xxA/xxB

Preliminary

DOT MATRIX LCD CONTROLLER DRIVER

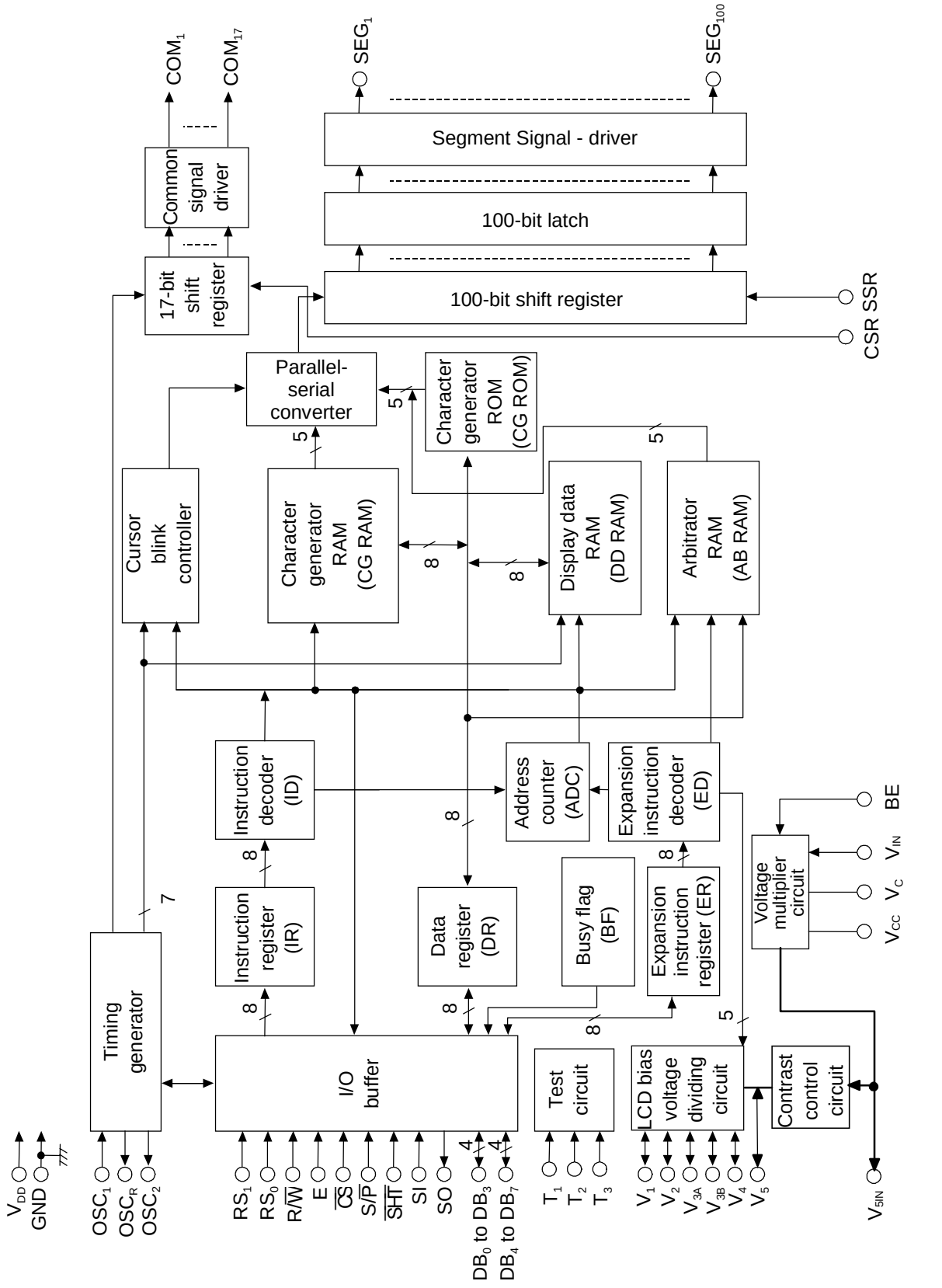
GENERAL DESCRIPTION

The ML9041A used in combination with an 8-bit or 4-bit microcontroller controls the operation of a character type dot matrix LCD.

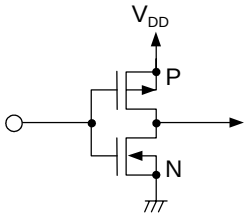
FEATURES

- Easy interfacing with 8-bit or 4-bit microcontroller
- Switchable between serial and parallel interfaces
- Dot-matrix LCD controller/driver for a small (5 × 7 dots) or large (5 × 10 dots) font
- Built-in circuit allowing automatic resetting at power-on
- Built-in 17 common signal drivers and 100 segment signal drivers
- Built-in character generation ROM capable of generating 160 small characters (5 × 7 dots) or 32 large characters (5 × 10 dots)
- Creation of character patterns by programming: up to 8 small character patterns (5 × 8 dots) or up to 4 large character patterns (5 × 11 dots)
- Built-in RC oscillation circuit using external or internal resistors
- Program-selectable duties: 1/9 duty (1 line: 5 × 7 dots + cursor + arbitrator), 1/12 duty (1 line: 5 × 10 dots + cursor + arbitrator), or 1/17 duty (2 lines: 5 × 7 dots + cursor + arbitrator)
- Built-in bias dividing resistors to drive the LCD
- Bi-directional transfer of segment outputs
- Bi-directional transfer of common outputs
- 100-dot arbitrator display
- Line display shifting
- Built-in contrast control circuit
- Built-in voltage multiplier circuit
- Gold Bump Chip
  With dummy bumps on both sides of the chip: ML9041A-xxA CVWA
  Without dummy bumps on both sides of the chip: ML9041A-xxB CVWA
  *xx indicates a character generator ROM code number.
  *01A and 01B indicate general character generator ROM code numbers.

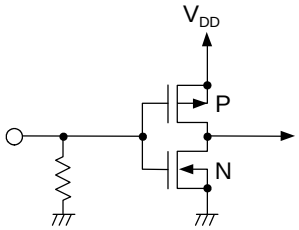
BLOCK DIAGRAM



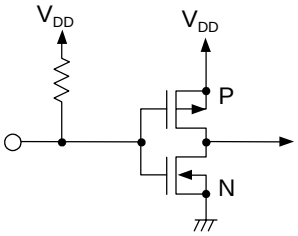
I/O CIRCUITS



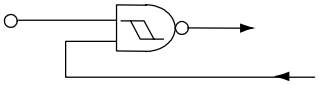
Applied to pins SSR, CSR, S/$\overline{P}$, and BE



Applied to pins T_1, T_2, and T_3

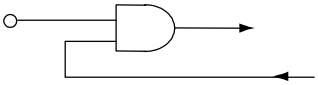


Applied to pins R/$\overline{W}$, RS_1, and RS_0



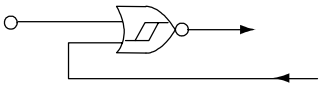
At serial I/F : "0"
At parallel I/F : "1"

Applied to pin E



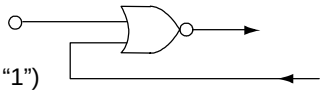
At serial I/F : "1" ($\overline{CS}$ = "0")
: "0" ($\overline{CS}$ = "1")
At parallel I/F : "0"

Applied to pin SI



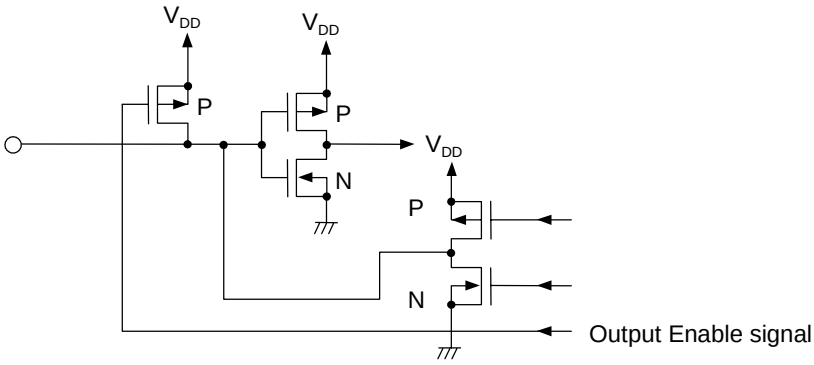
At serial I/F : "1" ($\overline{CS}$ = "1")
: "0" ($\overline{CS}$ = "0")
At parallel I/F : "1"

Applied to pin $\overline{SHT}$

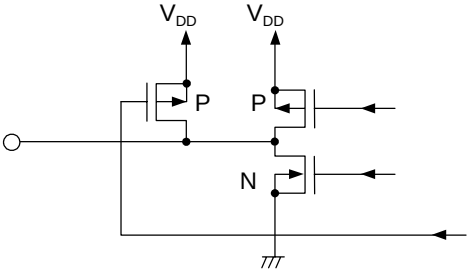


At serial I/F : "0"
At parallel I/F : "1"

Applied to pin $\overline{CS}$



Applied to pins DB_0 to DB_7



Applied to pin SO

PIN DESCRIPTIONS

<table>
<tr><th>Symbol</th><th>Description</th></tr>
<tr><td>R/$\overline{W}$</td><td>The input pin with a pull-up resistor to select Read (“H”) or Write (“L”) in the Parallel I/F Mode.
This pin should be open in the Serial I/F Mode.</td></tr>
<tr><td>RS_0, RS_1</td><td>The input pins with a pull-up resistor to select a register in the Parallel I/F Mode.
<table>
<tr><th>RS_1</th><th>RS_0</th><th>Name of register</th></tr>
<tr><td>H</td><td>H</td><td>Data register</td></tr>
<tr><td>H</td><td>L</td><td>Instruction register</td></tr>
<tr><td>L</td><td>L</td><td>Expansion Instruction register</td></tr>
</table>
This pin should be open in the Serial I/F Mode.</td></tr>
<tr><td>E</td><td>The input pin for data input/output between the CPU and the ML9041A and for activating instructions in the Parallel I/F Mode.
This pin should be open in the Serial I/F Mode.</td></tr>
<tr><td>DB_0 to DB_3</td><td>The input/output pins to transfer data of lower-order 4 bits between the CPU and the ML9041A in the Parallel I/F Mode. The pins are not used for the 4-bit interface and serial interface.
Each pin is equipped with a pull-up resistor, so this pin should be open when not used.</td></tr>
<tr><td>DB_4 to DB_7</td><td>The input/output pins to transfer data of upper 4 bits between the CPU and the ML9041A in the Parallel I/F Mode. The pins are not used for the serial interface.
Each pin is equipped with a pull-up resistor, so this pin should be open in the Serial I/F Mode when not used.</td></tr>
<tr><td>OSC_1
OSC_2
OSC_R</td><td>The clock oscillation pins required for LCD drive signals and the operation of the ML9041A by instructions sent from the CPU.
To input external clock, the OSC_1 pin should be used. The OSC_R and the OSC_2 pins should be open.
To start oscillation with an external resistor, the resistor should be connected between the OSC_1 and OSC_2 pins. The OSC_R pin should be open.
To start oscillation with an internal resistor, the OSC_2 and OSC_R pins should be short-circuited outside the ML9041A. The OSC_1 pin should be open.</td></tr>
<tr><td>COM_1 to COM_{17}</td><td>The LCD common signal output pins.
For 1/9 duty, non-selectable voltage waveforms are output via COM_{10} to COM_{17}. For 1/12 duty, non-selectable voltage waveforms are output via COM_{13} to COM_{17}.</td></tr>
<tr><td>SEG_1 to SEG_{100}</td><td>The LCD segment signal output pins.</td></tr>
</table>

Symbol	Description
CSR	The input pin to select the transfer direction of the common signal output data. At 1/n duty, data is transferred from COM1 to COMn when “L” is applied to this pin and transferred from COMn to COM1 when “H” is applied to this pin.
SSR	The input pin to select the transfer direction of the segment signal output data. “L”: Data transfer from SEG_1 to SEG_{100} “H”: Data transfer from SEG_{100} to SEG_1
V_1 , V_2, V_{3A}, V_{3B}, V_4	The pins to output bias voltages to the LCD. For 1/4 bias : The V_2 and V_{3B} pins are shorted. For 1/5 bias : The V_{3A} and V_{3B} pins are shorted.
BE	The input pin to enable or disable the voltage multiplier circuit. "L" disables the voltage multiplier circuit. "H" enables the voltage multiplier circuit. The voltage multiplier circuit doubles the input voltage between V_{DD} and V_{IN} and the multiplied voltage referenced to V_{DD} is output to the V_{5IN} pin. The voltage multiplier circuit can be used only when generating a level lower than GND.
V_{IN}	The pin to input voltage to the voltage multiplier.
V_5, V_{5IN}	The pins to supply the LCD drive voltage. The LCD drive voltage is supplied to the V_5 pin when the voltage multiplier is not used (BE = “0”) and the internal contrast adjusting circuit is also not used. At this time, the V_{5IN} pin should be open. The LCD drive voltage is supplied to the V_{5IN} pin when the voltage multiplier is not used (BE = “0”) but the internal contrast adjusting circuit is used. At this time, the V_5 pin should be open. When the voltage multiplier is used (BE = “1”), the V_5 pin should be open (the multiplied voltage is output to the V_{5IN} pin). In this case, the internal contrast adjusting circuit must be used. Capacitors for the voltage multiplier should be connected between the V_{DD} pin and the V_{5IN} pin.
V_C	The pin to connect the positive pin of the capacitor for the voltage multiplier. Leave the pin open when the voltage multiplier circuit is not used.
V_{CC}	The pin to connect the negative pin of the capacitor used for the voltage multiplier. Leave the pin open when the voltage multiplier circuit is not used.

Symbol	Description
T_1, T_2, T_3	The input pins for test circuits (normally open). Each of these pins is equipped with a pull-down resistor, so this pin should be left open.
V_{DD}	The power supply pin.
GND	The ground level input pin.
S/$\overline{P}$	The input pin to select the serial or parallel interface. "L" selects the parallel interface. "H" selects the serial interface.
$\overline{CS}$	The pin to enable this IC in the serial I/F mode. "L" enables this IC. "H" disables this IC. This pin should be open in the parallel I/F mode.
$\overline{SHT}$	The pin to input shift clock in the serial I/F mode. Data inputting to the SI pin is carried out synchronizing with the rising edge of this clock signal. Data outputting from the SO pin is carried out synchronizing with the falling edge of this clock signal. This pin should be open in the parallel I/F mode.
SI	The pin to input DATA in the serial I/F mode. Data inputting to this pin is carried out synchronizing with the rising edge of the $\overline{SHT}$ signal. This pin should be open in the parallel I/F mode.
SO	The pin to output DATA in the serial I/F mode. Data inputting to this pin is carried out synchronizing with the falling edge of the $\overline{SHT}$ signal. This pin should be open in the parallel I/F mode.
DUMMY	NC pin. Leave this pin open.

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V)

Parameter	Symbol	Condition	Rating	Unit	Applicable pins
Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +6.5	V	V_{DD}–GND
LCD Driving Voltage	V_1, V_2, V_3, V_4, V_5	Ta = 25°C	V_{DD}–7.5 to V_{DD}+0.3	V	V_1, V_4, V_5, V_{5IN}, V_2, V_{3A}, V_{3B}
Input Voltage	V_I	Ta = 25°C	–0.3 to V_{DD}+0.3	V	R/$\overline{W}$, E, $\overline{SHT}$, CSR, S/$\overline{P}$, SSR, SI, RS_0, RS_1, BE, $\overline{CS}$, T_1 to T_3, DB_0 to DB_7, V_{IN}
Storage Temperature	T_{STG}	—	–55 to +150	°C	—

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V)

Parameter	Symbol	Condition	Range	Unit	Applicable pins
Supply Voltage	V_{DD}	—	2.7 to 5.5	V	V_{DD}–GND
LCD Driving Voltage	V_{DD}–V_5 (See Note)	—	3.3 to 7.0	V	V_{DD}–V_5 (V_{5IN})
Voltage Multipler Operating Voltage	V_{MUL}	BE = "1"	2.7 to 3.5	V	V_{DD}–V_{IN}
Operating Temperature	T_{op}	—	–40 to +85	°C	—

Note: This voltage should be applied across V_{DD} and V_5. The following voltages are output to the V_1, V_2, V_{3A} (V_{3B}) and V_4 pins:

• 1/4 bias
$V_1 = \{V_{DD} – (V_{DD} – V_5)/4\} \pm 0.15$ V
$V_2 = V_{3B} = \{V_{DD} – (V_{DD} – V_5)/2\} \pm 0.15$ V
$V_4 = \{V_{DD} – 3 \times (V_{DD} – V_5)/4\} \pm 0.15$ V

• 1/5 bias
$V_1 = \{V_{DD} – (V_{DD} – V_5)/5\} \pm 0.15$ V
$V_2 = \{V_{DD} – 2 \times (V_{DD} – V_5)/5\} \pm 0.15$ V
$V_{3A} = V_{3B} = \{V_{DD} – 3 \times (V_{DD} – V_5)/5\} \pm 0.15$ V
$V_4 = \{V_{DD} – 4 \times (V_{DD} – V_5)/5\} \pm 0.15$ V

The voltages at the V_1, V_2, V_{3A} (V_{3B}), V_4 and V_5 pins should satisfy

$V_{DD} > V_1 > V_2 > V_{3A}$ (V_{3B}) $> V_4 > V_5$.
(Higher ← → Lower)

* If the chip is attached on a substrate using COG technology, the chip tends to be susceptible to electrical characteristics of the chip due to trace resistance on the glass substrate. It is recommended to use the chip by confirming that it operates on the glass substrate properly. Trace resistance, especially, V_{DD} and V_{SS} trace resistance, between the chip on the LCD panel and the flexible cable should be designed as low as possible. Trace resistance that cannot be very well decreased, larger size of the LCD panel, or greater trace capacitance between the microcontroller and the ML9041A device can cause device malfunction. In order to avoid the device malfunction, power noise should be reduced by serial interfacing of the microcontroller and the ML9041A device.

* Do not apply short-circuiting across output pins and across an output pin and an input/output pin or the power supply pin in the output mode.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(GND = 0 V, V_{DD} = 2.7 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
"H" Input Voltage	V_{IH}	—	0.8V_{DD}	—	V_{DD}	V	R/$\overline{W}$, RS_0, RS_1, E, DB_0 to DB_7, $\overline{SHT}$, S/$\overline{P}$, SI, $\overline{CS}$, OSC_1, SSR, CSR, BE
"L" Input Voltage	V_{IL}		0	—	0.2V_{DD}		
"H" Output Voltage 1	V_{OH1}	I_{OH} = –0.1 mA	0.75V_{DD}	—	—	V	DB_0 to DB_7, SO
"L" Output Voltage 1	V_{OL1}	I_{OL} = +0.1 mA	—	—	0.2V_{DD}		
"H" Output Voltage 2	V_{OH2}	I_{OH} = –13 µA	0.9V_{DD}	—	—	V	OSC_2
"L" Output Voltage 2	V_{OL2}	I_{OL} = +13 µA	—	—	0.1V_{DD}		
COM Voltage Drop	V_{CH}	I_{OCH} = –4 µA	V_{DD}–0.3	—	V_{DD}	V	COM_1 to COM_{17}
	V_{CMH}	I_{OCMH} = ±4 µA	V_1–0.3	—	V_1+0.3		
	V_{CML}	I_{OCML} = ±4 µA	V_4–0.3	—	V_4+0.3		
	V_{CL}	I_{OCL} = +4 µA	V_5	—	V_5+0.3		
SEG Voltage Drop	V_{SH}	I_{OSH} = –4 µA	V_{DD}–0.3	—	V_{DD}	V	SEG_1 to SEG_{100}
	V_{SMH}	I_{OSMH} = ±4 µA	V_2–0.3	—	V_2+0.3		
	V_{SML}	I_{OSML} = ±4 µA	V_3–0.3	—	V_3+0.3		
	V_{SL}	I_{OSL} = +4 µA	V_5	—	V_5+0.3		
		V_{DD} –V_5 = 5 V Note 1					
Input Leakage Current	| IIL |	V_{DD} = 5 V, V_I = 5 V or 0 V	—	—	1.0	µA	E, SSR, CSR, BE, $\overline{SHT}$, S/$\overline{P}$, $\overline{CS}$, SI
Input Current 1	| II1 |	V_{DD} = 5 V, V_I = GND	10	25	61	µA	R/$\overline{W}$, RS_0, RS_1, DB_0 to DB_7, SO
		V_{DD} = 5 V, V_I = V_{DD}, Excluding current flowing through the pull-up resistor and the output driving MOS	—	—	2.0		
Input Current 2	| II2 |	V_{DD} = 5 V, V_I = V_{DD}	15	45	105	µA	T_1, T_2, T_3
		V_{DD} = 5 V, V_I = GND Excluding current flowing through the pull-down resistor	—	—	2.0		
Supply Current	I_{DD}	V_{DD} = 5 V Note 2	—	—	1.2	mA	V_{DD}–GND
LCD Bias Resistor	R_{LB}		2.5	4.0	6.0	kΩ	V_{DD}, V_1, V_2, V_{3A}, V_{3B}, V_4, V_5
Oscillation Frequency of External Resistor Rf	f_{osc1}	Rf = 180 kΩ±2% Note 3	175	270	400	kHz	OSC_1, OSC_2
Oscillation Frequency of Internal Resistor Rf	f_{osc2}	OSC_1: Open Note 4 OSC_2 and OSC_R: Short-circuited	140	270	480	kHz	OSC_1, OSC_2, OSC_R
External Clock: Clock Input Frequency	f_{in}	OSC_2, OSC_R: Open Input from OSC_1	125	—	480	kHz	OSC_1
External Clock: Input Clock Duty	f_{duty}	Note 5	45	50	55	%	
External Clock: Input Clock Rise Time	f_{rf}	Note 6	—	—	0.2	µs	
External Clock: Input Clock Fall Time	f_{ff}	Note 6	—	—	0.2	µs	

(GND = 0 V, V_{DD} = 2.7 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable pins
Voltage Multiplier Input Voltage	V_{MUL}	Note 7		2.7	—	3.5	V	V_{DD}–V_{IN}
Voltage Multiplier Output Voltage	V_{5OUT}	V_{DD} = 2.7 V, V_{IN} = 0 V f = 125 kHz A capacitor for the voltage multiplier = 1 to 4.7 µF No load BE = "H"	1/5 bias	4.1	—	(V_{DD}–V_{IN}) × 2	V	V_{DD}–V_{5IN}
			1/4 bias	3.9	—	(V_{DD}–V_{IN}) × 2		
Maximum and minimum LCD drive voltages when internal variable resistors are used. Note 8	V_{LCD} MAX	V_{DD} = 5 V, V_{5IN} = –2 V, 1/5 bias, Contrast data: 1F, No load		6.6	—	—	V	V_{DD}–V_5
		V_{DD} = 5 V, V_{5IN} = –2 V, 1/4 bias, Contrast data: 1F, No load		6.6	—	—		
		V_{DD} = 4.1 V, V_{5IN} = 0 V, 1/5 bias, Contrast data: 1F, No load		3.8	—	—		
		V_{DD} = 3.9 V, V_{5IN} = 0 V, 1/4 bias, Contrast data: 1F, No load		3.6	—	—		
	V_{LCD} MIN	V_{DD} = 5 V, V_{5IN} = –2 V, 1/5 bias, Contrast data: 00, No load		4.0	—	4.6	V	
		V_{DD} = 5 V, V_{5IN} = –2 V, 1/4 bias, Contrast data: 00, No load		3.6	—	4.2		
		V_{DD} = 4.1 V, V_{5IN} = 0 V, 1/5 bias, Contrast data: 00, No load		2.2	—	2.8		
		V_{DD} = 3.9 V, V_{5IN} = 0 V, 1/4 bias, Contrast data: 00, No load		1.9	—	2.5		
Bias Voltage for Driving LCD	V_{LCD1}	V_{DD}–V_5 Note 9	1/5 bias	3.3	—	7.0	V	V_5
	V_{LCD2}		1/4 bias	3.3	—	7.0		

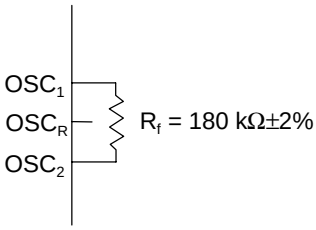
Note 1: Applied to the voltage drop occurring between any of the V_{DD}, V_1, V_4 and V_5 pins and any of the common pins (COM_1 to COM_{17}) when the current of 4 µA flows in or flows out at one common pin.
Also applied to the voltage drop occurring between any of the V_{DD}, V_2, V_{3A} (V_{3B}) and V_5 pins and any of the segment pins (SEG_1 to SEG_{100}) when the current of 4 µA flows in or flows out at one common pin.

The current of 4 µA flows out when the output level is V_{DD} or flows in when the output level is V_5.

Note 2: Applied to the current flowing into the V_{DD} pin when the external clock (f_{OSC2} = f_{in} = 270 kHz) is fed to the internal R_f oscillation or OSC_1 under the following conditions:

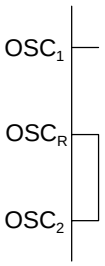
V_{DD} = 5 V
GND = V_5 = 0 V,
V_1, V_2, V_{3A} (V_{3B}) and V_4: Open
E, SSR, CSR, and BE: "L" (fixed)
Other input pins: "L" or "H" (fixed)
Other output pins: No load

Note 3:



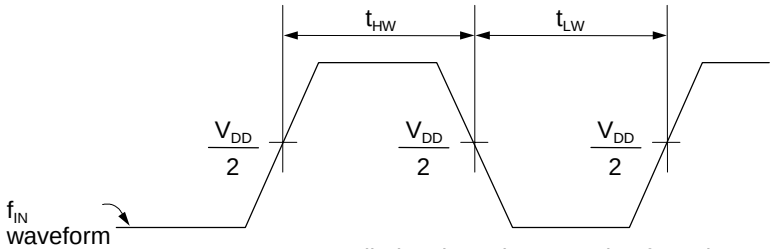
The wire between OSC_1 and R_f and the wire between OSC_2 and R_f should be as short as possible. Keep OSC_R open.

Note 4:



The wire between OSC_2 and OSC_R should be as short as possible. Keep OSC_1 open.

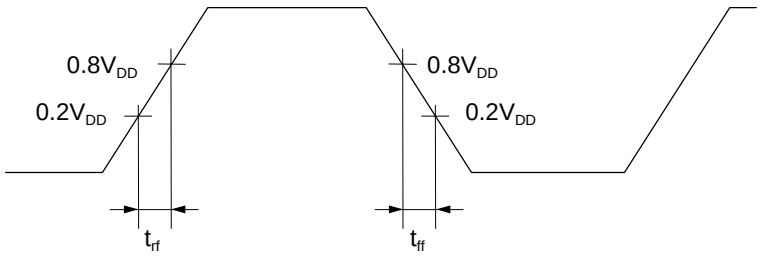
Note 5:



Applied to the pulses entering from the OSC_1 pin

$f_{duty} = t_{HW}/(t_{HW} + t_{LW}) \times 100$ (%)

Note 6:



Applied to the pulses entering from the OSC_1 pin

Note 7: The maximum value of the voltage multiplier input voltage should be set at 3.5 V, and the minimum value of the voltage multiplier input voltage should be set so that the voltage multiplier output voltage meets the specification for the bias voltage for driving LCD after contrast adjustment.

Note 8: If using the built-in contrast control circuit, control the circuit so that the voltage of V_{DD}-V_5 is the minimum value of the bias voltage for driving LCD or higher.

Note 9: For 1/4 bias, V_2 and V_{3B} pins are short-circuited. V_{3A} pin is open.
For 1/5 bias, V_{3A} and V_{3B} pins are short-circuited. V_2 pin is open.

Switching Characteristics (The following ratings are subject to change after ES evaluation.)

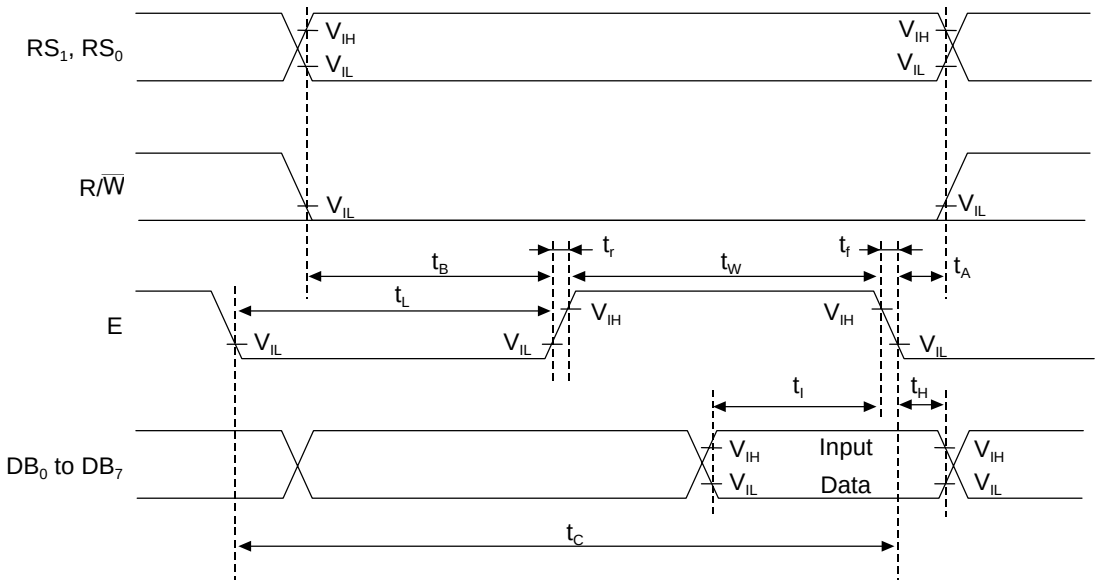
- Parallel Interface Mode

The timing for the input from the CPU (see 1) and the timing for the output to the CPU (see 2) are as shown below:

1) WRITE MODE (Timing for input from the CPU)

(V_{DD} = 2.7 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
R/$\overline{W}$, RS_0, RS_1 Setup Time	t_B	40	—	—	ns
E Pulse Width	t_W	450	—	—	ns
R/$\overline{W}$, RS_0, RS_1 Hold Time	t_A	10	—	—	ns
E Rise Time	t_r	—	—	25	ns
E Fall Time	t_f	—	—	25	ns
E Pulse Width	t_L	430	—	—	ns
E Cycle Time	t_C	1000	—	—	ns
DB_0 to DB_7 Input Data Hold Time	t_I	195	—	—	ns
DB_0 to DB_7 Input Data Setup Time	t_H	10	—	—	ns

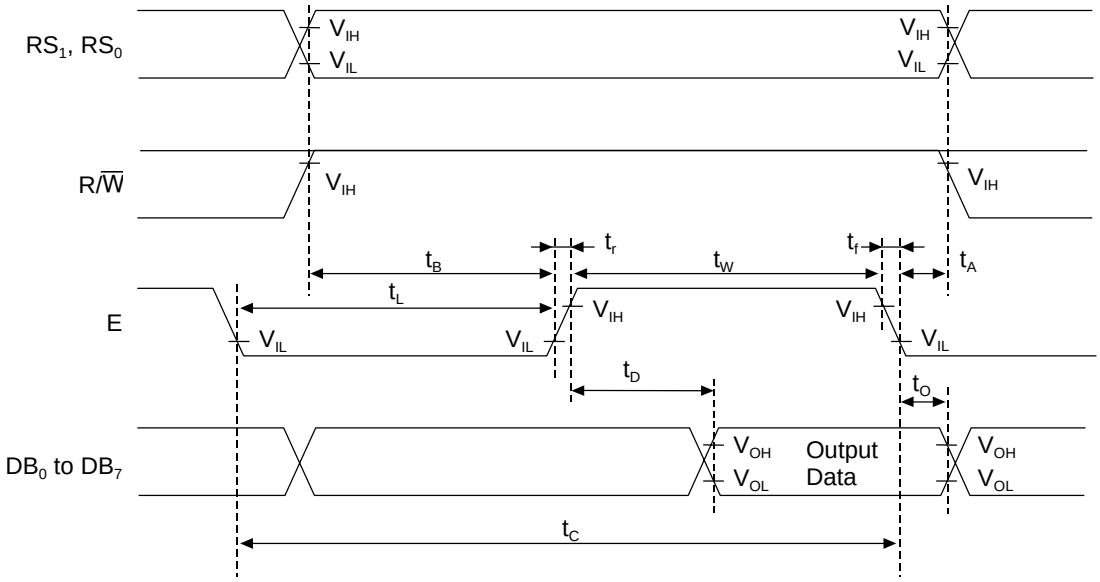


2) READ MODE (Timing for output to the CPU)

(V_{DD} = 2.7 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
R/$\overline{W}$, RS_1, RS_0 Setup Time	t_B	40	—	—	ns
E Pulse Width	t_W	450	—	—	ns
R/$\overline{W}$, RS_1, RS_0 Hold Time	t_A	10	—	—	ns
E Rise Time	t_r	—	—	25	ns
E Fall Time	t_f	—	—	25	ns
E Pulse Width	t_L	430	—	—	ns
E Cycle Time	t_C	1000	—	—	ns
DB_0 to DB_7 Output Data Delay Time	t_D	—	—	350	ns
DB_0 to DB_7 Output Data Hold Time	t_O	20	—	—	ns

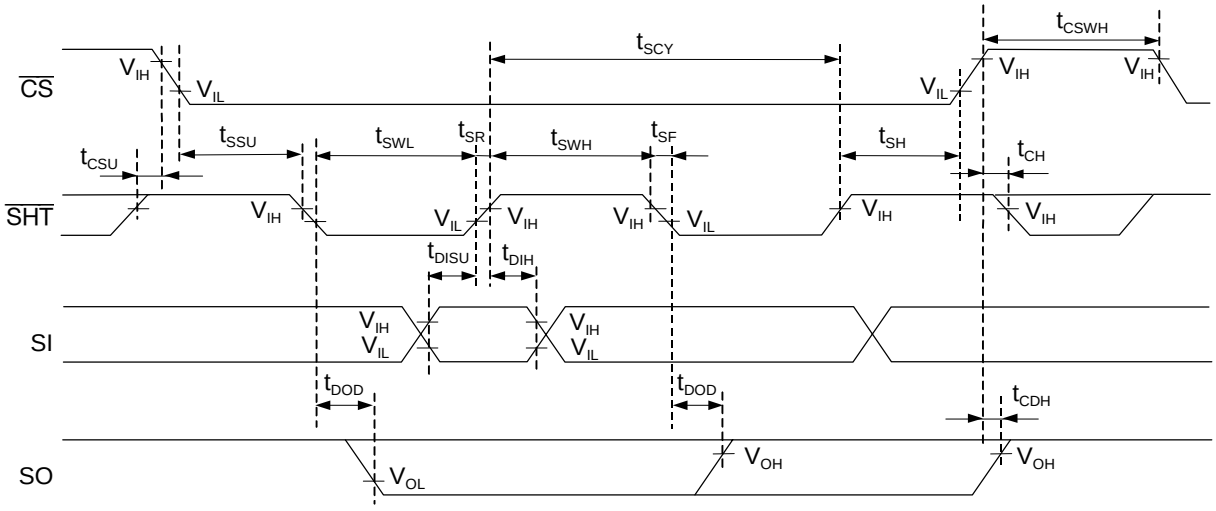
Note: A load capacitance of each of DB_0 to DB_7 must be 50 pF or less.



- Serial Interface Mode

(V_{DD} = 2.7 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{SHT}$ Cycle Time	t_{SCY}	500	—	—	ns
$\overline{CS}$ Setup Time	t_{CSU}	100	—	—	ns
$\overline{CS}$ Hold Time	t_{CH}	100	—	—	ns
$\overline{CS}$ "H" Pulse Width	t_{CSWH}	200	—	—	ns
$\overline{SHT}$ Setup Time	t_{SSU}	60	—	—	ns
$\overline{SHT}$ Hold Time	t_{SH}	200	—	—	ns
$\overline{SHT}$ "H" Pulse Width	t_{SWH}	200	—	—	ns
$\overline{SHT}$ "L" Pulse Width	t_{SWL}	200	—	—	ns
$\overline{SHT}$ Rise Time	t_{SR}	—	—	50	ns
$\overline{SHT}$ Fall Time	t_{SF}	—	—	50	ns
SI Setup Time	t_{DISU}	100	—	—	ns
SI Hold Time	t_{DIH}	100	—	—	ns
Data Output Delay Time	t_{DOD}	—	—	160	ns
Data Output Hold Time	t_{CDH}	0	—	—	ns



FUNCTIONAL DESCRIPTION

Instruction Register (IR), Data Register (DR), and Expansion Instruction Register (ER)

These registers are selected by setting the level of the Register Selection input pins RS_0 and RS_1. The DR is selected when both RS_0 and RS_1 are "H". The IR is selected when RS_0 is "L" and RS_1 is "H". The ER is selected when both RS_0 and RS_1 are "L". (When RS_0 is "H" and RS_1 is "L", the ML9041A is not selected.)
The IR stores an instruction code and sets the address code of the display data RAM (DDRAM) or the character generator RAM (CGRAM).
The microcontroller (CPU) can write to the IR but cannot read from the IR.
The ER stores a contrast adjusting code and sets the address code of the arbitrator RAM (ABRAM).
The CPU can write to or read from the ER.
The DR stores data to be written in the DDRAM, ABRAM and CGRAM and also stores data read from the DDRAM, ABRAM and CGRAM.
The data written in the DR by the CPU is automatically written in the DDRAM, ABRAM or CGRAM.
When an address code is written in the IR or ER, the data of the specified address is automatically transferred from the DDRAM, ABRAM or CGRAM to the DR. The data of the DDRAM, ABRAM and CGRAM can be checked by allowing the CPU to read the data stored in the DR.
After the CPU writes data in the DR, the data of the next address in the DDRAM, ABRAM or CGRAM is selected to be ready for the next writing by the CPU. Similarly, after the CPU reads the data in the DR, the data of the next address in the DDRAM, ABRAM or CGRAM is set in the DR to be ready for the next reading by the CPU.
Writing in or reading from these 3 registers is controlled by changing the status of the R/$\overline{W}$ (Read/Write) pin.

Table 1 R/$\overline{W}$ pin status and register operation

R/$\overline{W}$	RS_0	RS_1	Operation
L	L	H	Writing in the IR
H	L	H	Reading the Busy flag (BF) and the address counter (ADC)
L	H	H	Writing in the DR
H	H	H	Reading from the DR
L	L	L	Writing in the ER
H	L	L	Reading the contrast code
L	H	L	Disabled (Not in a busy state, not performing the writes)
H	H	L	Disabled (Not in a busy state, not performing the reads. Note data read by the CPU is undefined since the data bus is high impedance.)

Busy Flag (BF)

The status "1" of the Busy Flag (BF) indicates that the ML9041A is carrying out internal operation.
When the BF is "1", any new instruction is ignored.
When R/$\overline{W}$ = "H", RS_0 = "L" and RS_1 = "H", the data in the BF is output to the DB_7.
New instructions should be input when the BF is "0".
When the BF is "1", the output code of the address counter (ADC) is undefined.

Address Counter (ADC)

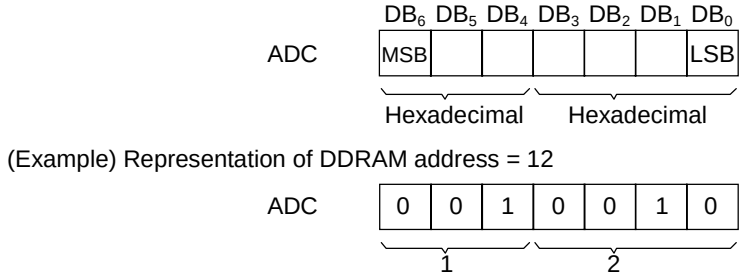
The address counter provides a read/write address for the DDRAM, ABRAM or CGRAM and also provides a cursor display address.
When an instruction code specifying DDRAM, ABRAM or CGRAM address setting is input to the pre-defined register, the register selects the specified DDRAM, ABRAM or CGRAM and transfers the address code to the ADC. The address data in the ADC is automatically incremented (or decremented) by 1 after the display data is written in or read from the DDRAM, ABRAM or CGRAM.
The data in the ADC is output to DB_0 to DB_6 when R/$\overline{W}$ = "H", RS_0 = "L", RS_1 = "H" and BF = "0".

Timing Generator

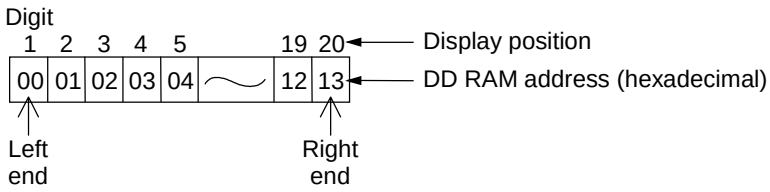
The timing generator generates timing signals for the internal operation of the ML9041A activated by the instruction sent from the CPU or for the operation of the internal circuits of the ML9041A such as DDRAM, ABRAM, CGRAM and CGROM. Timing signals are generated so that the internal operation carried out for LCD displaying will not be interfered by the internal operation initiated by accessing from the CPU. For example, when the CPU writes data in the DDRAM, the display of the LCD not corresponding to the written data is not affected.

Display Data RAM (DDRAM)

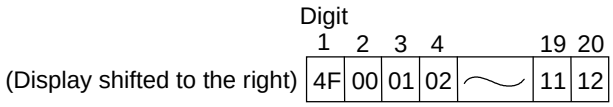
This RAM stores the 8-bit character codes (see Table 2).
The DDRAM addresses correspond to the display positions (digits) of the LCD as shown below. The DDRAM addresses (to be set in the ADC) are represented in hexadecimal.

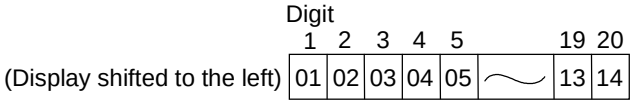


1) Relationship between DDRAM addresses and display positions (1-line display mode)

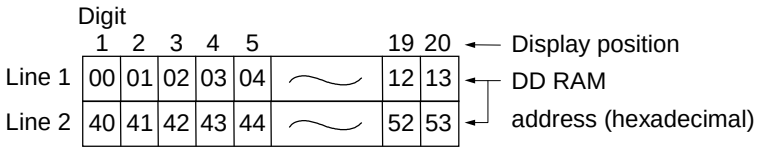


In the 1-line display mode, the ML9041A can display up to 20 characters from digit 1 to digit 20. While the DDRAM has addresses “00” to “4F” for up to 80 character codes, the area not used for display can be used as a RAM area for general data. When the display is shifted by instruction, the relationship between the LCD display and the DDRAM address changes as shown below:





2) Relationship between DDRAM addresses and display positions (2-line display mode)
In the 2-line mode, the ML9041A can display up to 40 characters (20 characters per line) from digit 1 to digit 20.



Note: The DDRAM address at digit 20 in the first line is not consecutive to the DDRAM address at digit 1 in the second line.

When the display is shifted by instruction, the relationship between the LCD display and the DDRAM address changes as shown below:

(Display shifted to the right)

Digit	1	2	3	4	5		19	20
Line 1	27	00	01	02	03		11	12
Line 2	67	40	41	42	43		51	52

(Display shifted to the left)

Digit	1	2	3	4	5		19	20
Line 1	01	02	03	04	05		13	14
Line 2	41	42	43	44	45		53	54

Character Generator ROM (CGROM)

The CGROM generates small character patterns (5 × 7 dots, 160 patterns) or large character patterns (5 × 10 dots, 32 patterns) from the 8-bit character code signals in the DDRAM.
When the 8-bit character code corresponding to a character pattern in the CGROM is written in the DDRAM, the character pattern is displayed in the display position specified by the DDRAM address.
Character codes 20 to 7F and A0 to FF are contained in the character code area in the CG ROM.
Character codes 20 to 7F and A0 to DF are contained in the character code area for the 5 × 7-dot character patterns.
Character codes E0 to FF are contained in the ROM area for 5 × 10-dot character patterns.
The general character generator ROM codes are 01A/01B.
The relationship between character codes and general purpose character patterns are indicated in Table 2.

Character Generator RAM (CGRAM)

The CGRAM is used to generate user-specific character patterns that are not in the CGROM. CGRAM (64 bytes = 512 bits) can store up to 8 small character patterns (5 × 8 dots) or up to 4 large character patterns (5 × 11 dots). When displaying a character pattern stored in the CGRAM, write an 8-bit character code (00 to 07 or 08 to 0F; hex.) assigned in Table 2 to the DDRAM. This enables outputting the character pattern to the LCD display position corresponding to the DDRAM address.
The cursor or blink is also displayed even when a CGRAM or ABRAM address is set in the ADC. Therefore, the cursor or blink display should be inhibited while the ADC is holding a CGRAM or ABRAM address.
The following describes how character patterns are written in and read from the CGRAM.

1) Small character patterns (5 × 8 dots) (See Table 3-1.)

(1) A method of writing character patterns to the CGRAM from the CPU
The three CGRAM address bit weights 0 to 2 select one of the lines constituting a character pattern.
First, set the mode to increment or decrement from the CPU, and then input the CGRAM address.
Write each line of the character pattern in the CGRAM through DB_0 to DB_7.
The data lines DB_0 to DB_7 correspond to the CGRAM data bit weights 0 to 7, respectively (see Table 3-1). Input data "1" represents the ON status of an LCD dot and "0" represents the OFF status. Since the ADC is automatically incremented or decremented by 1 after the data is written to the CGRAM, it is not necessary to set the CGRAM address again.
The bottom line of a character pattern (the CGRAM address bit weights 0 to 2 are all "1", which means 7 in hexadecimal) is the cursor line. The ON/OFF pattern of this line is ORed with the cursor pattern for displaying on the LCD. Therefore, the pattern data for the cursor position should be all zeros to display the cursor.
Whereas the data given by the CGRAM data bit weights 0 to 4 is output to the LCD as display data, the data given by the CGRAM data bit weights 5 to 7 is not. Therefore, the CGRAM data bit weights 5 to 7 can be used as a RAM area.

(2) A method of displaying CGRAM character patterns on the LCD
The CGRAM is selected when the higher-order 4 bits of a character code are all zeros. Since bit weight 3 of a character code is not used, the character pattern "0" in Table 3-1 can be selected using the character code "00" or "08" in hexadecimal.
When the 8-bit character code corresponding to a character pattern in the CGRAM is written to the DDRAM, the character pattern is displayed in the display position specified by the DDRAM address. (The DDRAM data bit weights 0 to 2 correspond to the CGRAM address bit weights 3 to 5, respectively.)

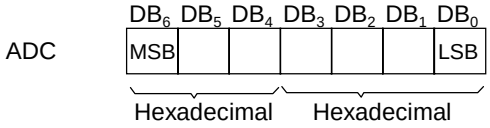
2) Large character patterns (5 × 11 dots) (See Table 3-2.)

(1) A method of writing character patterns to the CGRAM from the CPU
The four CGRAM address bit weights 0 to 3 select one of the lines constituting a character pattern.
First, set the mode to increment or decrement from the CPU, and then input the CGRAM address.
Write each line of the character pattern code in the CGRAM through DB_0 to DB_7.
The data lines DB_0 to DB_7 correspond to the CGRAM data bit weights 0 to 7, respectively (see Table 3-2). Input data "1" represents the ON status of an LCD dot and "0" represents the OFF status. Since the ADC is automatically incremented or decremented by 1 after the data is written to the CGRAM, it is not necessary to set the CGRAM address again.
The bottom line of a character pattern (the CGRAM address bit weights 0 to 3 are all "1", which means A in hexadecimal) is a cursor line. The ON/OFF pattern of this line is ORed with the cursor pattern for displaying on the LCD. Therefore, the pattern data for the cursor position should be all zeros to display the cursor.
Whereas CGRAM data bit weights 0 to 4 are output as display data to the LCD when CGRAM address bit weights 0 to 3 are "0" to "A" in hexadecimal, the data given by the CGRAM data bit weights 5 to 7 or the CGRAM addresses B to F in hexadecimal is not. These bits can be written and read as a RAM area.

(2) A method of displaying CGRAM character patterns on the LCD
The CGRAM is selected when the higher-order 4 bits of a character code are all zeros. Since bit weights 0 and 3 of a character code are not used, the character pattern "g" in Table 3-2 can be selected with a character code "02", "03", "0A" or "0B" in hexadecimal.
When the 8-bit character code corresponding to a character pattern in the CGRAM is written to the DDRAM, the character pattern is displayed in the display position specified by the DDRAM address. (The DDRAM data bit weights 1 and 2 correspond to the CGRAM address bit weights 4 and 5, respectively.)

Arbitrator RAM (ABRAM)

The arbitrator RAM (ABRAM) stores arbitrator display data.
100 dots can be displayed in both 1-line and 2-line display modes. The arbitrator RAM has the addresses (hexadecimal) from "00" to "1F" and the valid display address area is from 00 to 19 (0H to 13H). The area of 20 to 31 (14H to 1FH) not used for display can be used as a data RAM area for general data. Even if the display is shifted by instruction, the arbitrator display is not shifted.
A capacity of 8 bits by 32 addresses (= 256 bits) is available for data write.
First set the mode to increment or decrement from the CPU, and then input the ABRAM address.
Write Display-ON data in the ABRAM through DB_0 to DB_7.
DB_0 to DB_7 correspond to the ABRAM data bit weights 0 to 7 respectively. Input data "1" represents the ON status of an LCD dot and "0" represents the OFF status.
Since ADC is automatically incremented or decremented by 1 after the data is written to the ABRAM, it is not necessary to set the ABRAM address again.
Whereas ABRAM data bit weights 0 to 4 are output as display data to the LCD, the ABRAM data bit weights 5 to 7 are not. These bits can be used as a RAM area.
The cursor or blink is also displayed even when a CGRAM or ABRAM address is set in the ADC. Therefore, the cursor or blink display should be inhibited while the ADC is holding a CGRAM or ABRAM address.



The arbitrator RAM can store a maximum of 100 dots of the arbitrator Display-ON data in units of 5 dots.
The relationship with the LCD display positions is shown below.

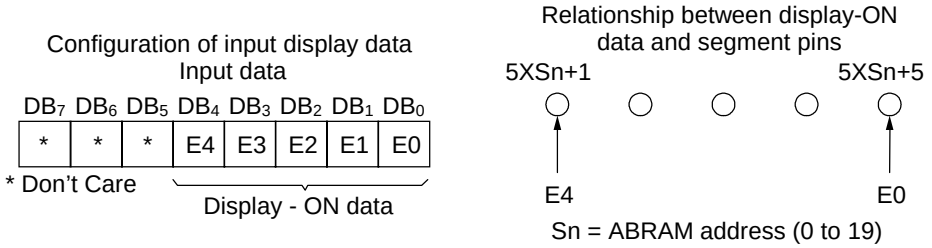


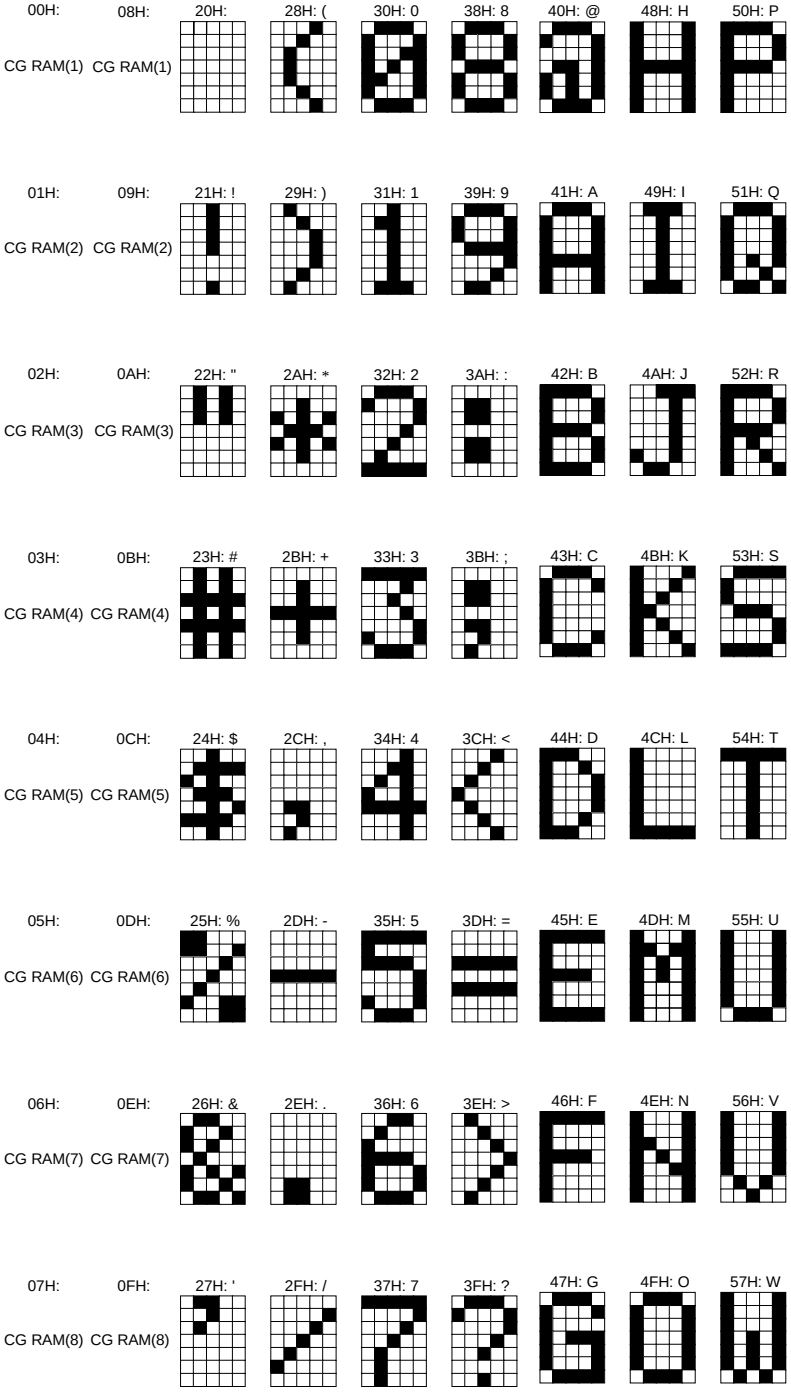
Table 2 Relationship between Character Codes and Character Patterns of the ML9041A-01A/01B (General Character Codes)

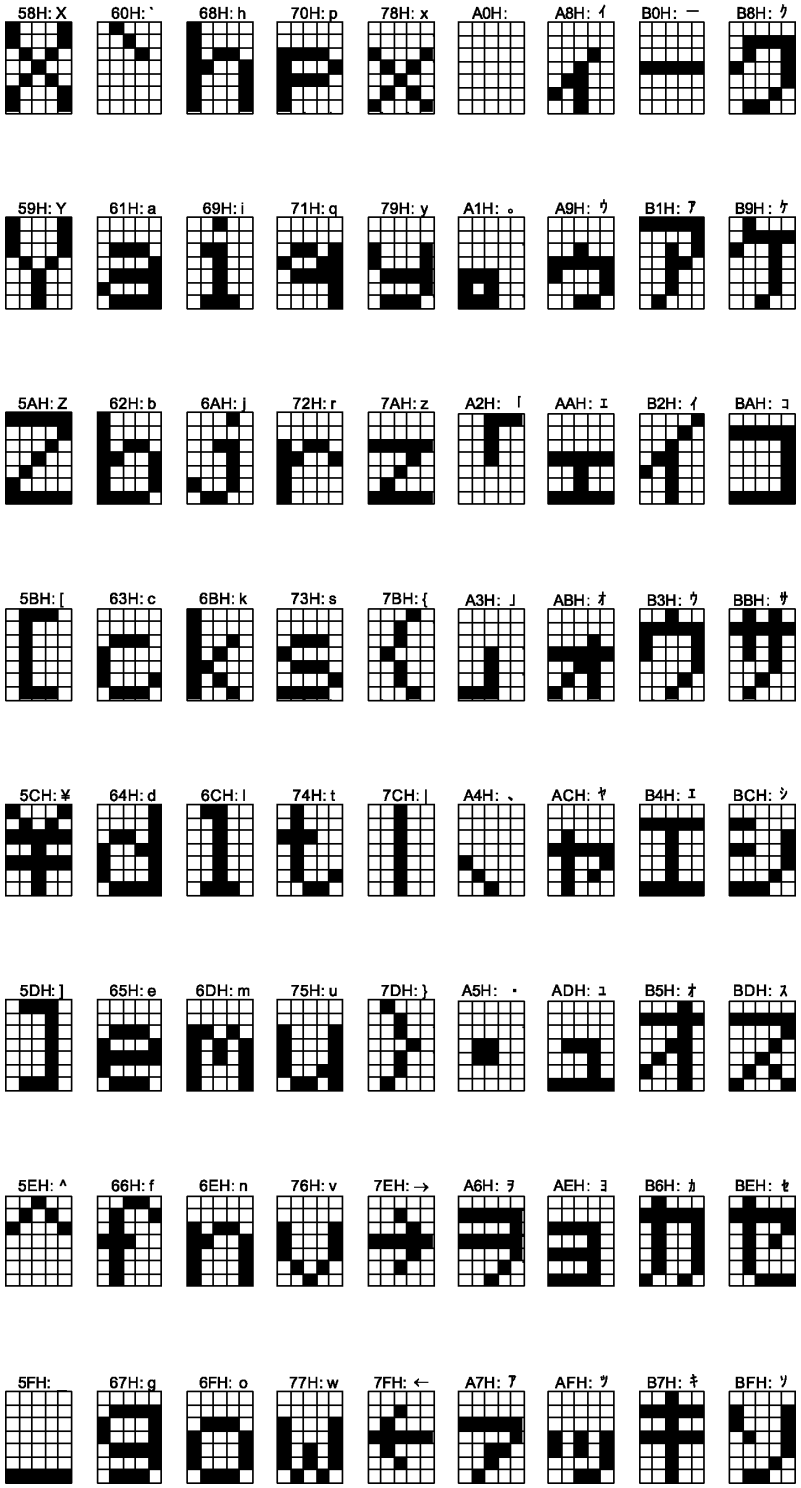
The character code area in the CG ROM: Character codes 20H to 7FH, A0H to FFH.

5×7-dot ROM area: 20H to 7FH, A0H to DFH

5×10-dot ROM area: E0H to FFH

The CG RAM area : Character codes 00H to 0FH




58H: X
60H: `
68H: h
70H: p
78H: x
A0H:
A8H: ｲ
B0H: ｰ
B8H: ｸ
59H: Y
61H: a
69H: i
71H: q
79H: y
A1H: 。
A9H: ｳ
B1H: ｱ
B9H: ｹ
5AH: Z
62H: b
6AH: j
72H: r
7AH: z
A2H: 「
AAH: ｴ
B2H: ｲ
BAH: ｺ
5BH: [
63H: c
6BH: k
73H: s
7BH: {
A3H: 」
ABH: ｵ
B3H: ｳ
BBH: ｻ
5CH: ¥
64H: d
6CH: l
74H: t
7CH: |
A4H: 、
ACH: ｬ
B4H: ｴ
BCH: ｼ
5DH:]
65H: e
6DH: m
75H: u
7DH: }
A5H: ・
ADH: ｭ
B5H: ｵ
BDH: ｽ
5EH: ^
66H: f
6EH: n
76H: v
7EH: →
A6H: ｦ
AEH: ｮ
B6H: ｶ
BEH: ｾ
5FH:
67H: g
6FH: o
77H: w
7FH: ←
A7H: ｧ
AFH: ｯ
B7H: ｷ
BFH: ｿ

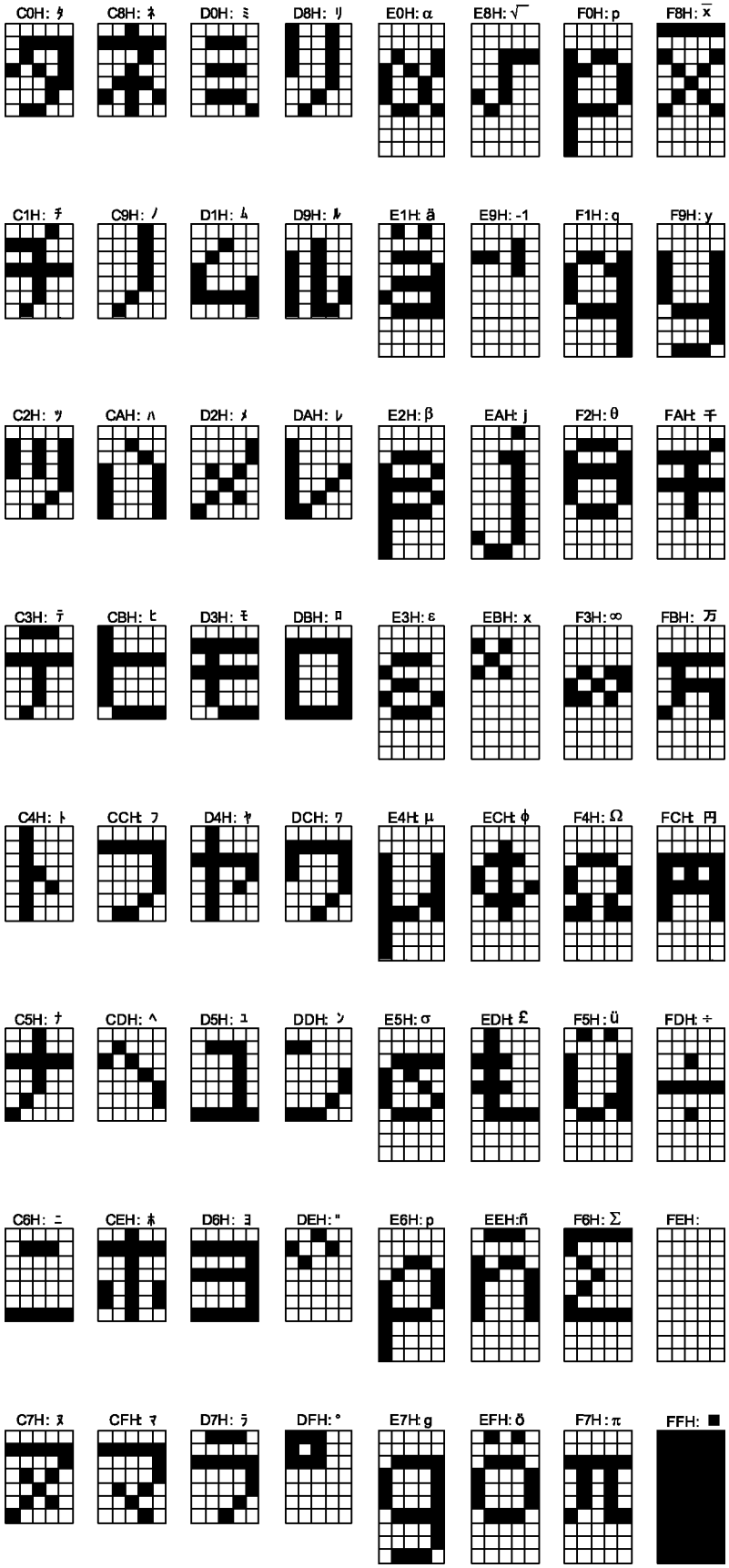

C0H: ｦ
C8H: ｷ
D0H: ﾐ
D8H: ﾘ
E0H: α
E8H: √
F0H: ρ
F8H: x̄
C1H: ｱ
C9H: ﾉ
D1H: ﾑ
D9H: ﾙ
E1H: ä
E9H: -1
F1H: q
F9H: y
C2H: ｳ
CAH: ﾊ
D2H: ﾒ
DAH: ﾚ
E2H: β
EAH: j
F2H: θ
FAH: 千
C3H: ｴ
CBH: ﾋ
D3H: ﾓ
DBH: ﾛ
E3H: ε
EBH: x
F3H: ∞
FBH: 万
C4H: ｵ
CCH: ﾌ
D4H: ﾔ
DCH: ﾜ
E4H: μ
ECH: φ
F4H: Ω
FCH: 円
C5H: ｶ
CDH: ﾍ
D5H: ﾕ
DDH: ﾝ
E5H: σ
EDH: £
F5H: ü
FDH: ÷
C6H: ｺ
CEH: ﾎ
D6H: ﾖ
DEH: "
E6H: ρ
EEH: ñ
F6H: Σ
FEH:
C7H: ｻ
CFH: ﾏ
D7H: ﾗ
DFH: °
E7H: g
EFH: ö
F7H: π
FFH: ■

Table 3-1 Relationship between CGRAM address bits, CGRAM data bits (character pattern) and DDRAM data bits (character code) in 5 × 7 dot character mode. (Examples)

CG RAM address	CG RAM data (Character pattern)	DD RAM data (Character code)
5 4 3 2 1 0 (MSB LSB)	7 6 5 4 3 2 1 0 (MSB LSB)	7 6 5 4 3 2 1 0 (MSB LSB)
0 0 0 0 0 0	× × × 0 1 1 1 0	0 0 0 0 × 0 0 0
0 0 0 0 1	1 0 0 0 1	
0 0 0 1 0	1 0 0 0 1	
0 0 0 1 1	1 0 0 0 1	
0 0 1 0 0	1 0 0 0 1	
0 0 1 0 1	1 0 0 0 1	
0 0 1 1 0	0 1 1 1 0	
0 0 1 1 1	0 0 0 0 0	
0 0 1 0 0 0	× × × 1 0 0 0 1	0 0 0 0 × 0 0 1
0 0 1 0 0 1	1 0 0 1 0	
0 0 1 0 1 0	1 0 1 0 0	
0 0 1 0 1 1	1 1 0 0 0	
0 0 1 1 0 0	1 0 1 0 0	
0 0 1 1 0 1	1 0 0 1 0	
0 0 1 1 1 0	1 0 0 0 1	
0 0 1 1 1 1	0 0 0 0 0	
⋮	⋮	⋮
1 1 1 0 0 0	× × × 0 1 1 1 0	0 0 0 0 × 1 1 1
1 1 1 0 0 1	0 0 1 0 0	
1 1 1 0 1 0	0 0 1 0 0	
1 1 1 0 1 1	0 0 1 0 0	
1 1 1 1 0 0	0 0 1 0 0	
1 1 1 1 0 1	0 0 1 0 0	
1 1 1 1 1 0	0 1 1 1 0	
1 1 1 1 1 1	0 0 0 0 0	

×: Don't Care

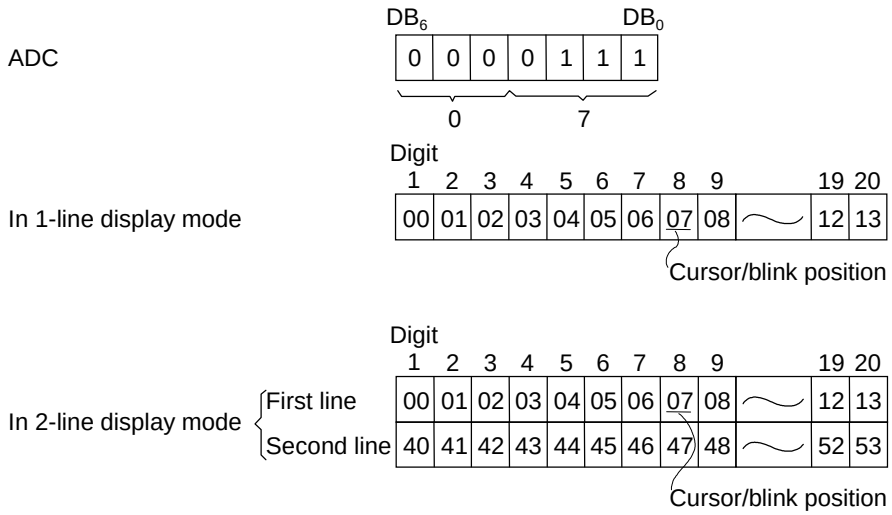
Table 3-2 Relationship between CGRAM address bits, CGRAM data bits (character pattern) and DDRAM data bits (character code) in 5 × 10 dot character mode (Examples)

CG RAM address	CG RAM data (Character pattern)	DD RAM data (Character code)
5 4 3 2 1 0 (MSB LSB)	7 6 5 4 3 2 1 0 (MSB LSB)	7 6 5 4 3 2 1 0 (MSB LSB)
0 0 0 0 0 0	× × × 0 1 0 0 0	0000×00×
0 0 0 0 1	0 1 1 1 1	
0 0 0 1 0	1 0 0 1 0	
0 0 0 1 1	0 1 1 1 1	
0 0 1 0 0	0 1 0 1 0	
0 0 1 0 1	1 1 1 1 1	
0 0 1 1 0	0 0 0 1 0	
0 0 1 1 1	0 0 0 0 0	
0 1 0 0 0	0 0 0 0 0	
0 1 0 0 1	0 0 0 0 0	
0 1 0 1 0	0 0 0 0 0	
0 1 0 1 1	× × × × ×	
0 1 1 0 0		
0 1 1 0 1		
0 1 1 1 0		
0 1 1 1 1		
0 1 0 0 0 0	× × × 0 0 0 0 0	0000×01×
0 0 0 0 1	0 0 0 0 0	
0 0 0 1 0	0 1 1 1 1	
0 0 0 1 1	1 0 0 0 1	
0 0 1 0 0	1 0 0 0 1	
0 0 1 0 1	1 0 0 0 1	
0 0 1 1 0	0 1 1 1 1	
0 0 1 1 1	0 0 0 0 1	
0 1 0 0 0	0 0 0 0 1	
0 1 0 0 1	0 1 1 1 0	
0 1 0 1 0	0 0 0 0 0	
0 1 0 1 1	× × × × ×	
0 1 1 0 0		
0 1 1 0 1		
0 1 1 1 0		
0 1 1 1 1		
1 1 0 0 0 0	× × × 0 0 0 0 0	0000×11×
0 0 0 0 1	0 0 0 0 0	
0 0 0 1 0	1 1 0 1 1	
0 0 0 1 1	0 1 0 1 0	
0 0 1 0 0	1 0 0 0 1	
0 0 1 0 1	1 0 0 0 1	
0 0 1 1 0	0 1 1 1 0	
0 0 1 1 1	0 0 0 0 0	
0 1 0 0 0	0 0 0 0 0	
0 1 0 0 1	0 0 0 0 0	
0 1 0 1 0	0 0 0 0 0	
0 1 0 1 1	× × × × ×	
0 1 1 0 0		
0 1 1 0 1		
0 1 1 1 0		
0 1 1 1 1		

×: Don't Care

Cursor/Blink Control Circuit

This circuit generates the cursor and blink of the LCD.
The operation of this circuit is controlled by the program of the CPU.
The cursor/blink display is carried out in the position corresponding to the DDRAM address set in the ADC (Address Counter).
For example, when the ADC stores a value of "07" (hexadecimal), the cursor or blink is displayed as follows:



Note: The cursor or blink is also displayed even when a CGRAM or ABRAM address is set in the ADC. Therefore, the cursor or blink display should be inhibited while the ADC is holding a CGRAM or ABRAM address.

LCD Display Circuit (COM1 to COM17, SEG1 to SEG100, SSR and CSR)

The ML9041A has 17 common signal outputs and 100 segment signal outputs to display 20 characters (in the 1-line display mode) or 40 characters (in the 2-line display mode).
The character pattern is converted into serial data and transferred in series through the shift register.
The transfer direction of serial data is determined by the SSR pin. The shift direction of common signals is determined by the CSR pin. The following tables show the transfer and shift directions:

SSR	Transfer direction
L	$SEG_1 \rightarrow SEG_{100}$
H	$SEG_{100} \rightarrow SEG_1$

CSR	duty	AS bit	Shift Direction	Arbitrator's common pin
L	1/9	L	COM1 → COM9	COM9
L	1/9	H	COM1 → COM9	COM1
L	1/12	L	COM1 → COM12	COM12
L	1/12	H	COM1 → COM12	COM1
L	1/17	L	COM1 → COM17	COM17
L	1/17	H	COM1 → COM17	COM1
H	1/9	L	COM9 → COM1	COM1
H	1/9	H	COM9 → COM1	COM9
H	1/12	L	COM12 → COM1	COM1
H	1/12	H	COM12 → COM1	COM12
H	1/17	L	COM17 → COM1	COM1
H	1/17	H	COM17 → COM1	COM17

* Refer to the Expansion Instruction Codes section about the AS bit.

Signals to be input to the SSR and CSR pins should be determined at power-on and be kept unchanged.

Built-in Reset Circuit

The ML9041A is automatically initialized when the power is turned on.
During initialization, the Busy Flag (BF) is "1" and the ML9041A does not accept any instruction from the CPU (other than the Read BF instruction).
The Busy Flag is "1" for about 15 ms after the V_{DD} becomes 2.7 V or higher.
During this initialization, the ML9041A performs the following instructions:

1) Display clearing
2) CPU interface data length = 8 bits (DL = "1")
3) 1-line LCD display (N = "0")
4) Font size = 5 × 7 dots (F = "0")
5) ADC counting = Increment (I/D = "1")
6) Display shifting = None (S = "0")
7) Display = Off (D = "0")
8) Cursor = Off (C = "0")
9) Blinking = Off (B = "0")
10) Arbitrator = Displayed in the lower line (AS = "0")
11) Setting 1FH (hexadecimal) to the Contrast Data

To use the built-in reset circuit, the power supply conditions shown below should be satisfied. Otherwise, the built-in reset circuit may not work properly. In such a case, initialize the ML9041A with the instructions from the CPU. The use of a battery always requires such initialization from the CPU. (See "Initial Setting of Instructions")

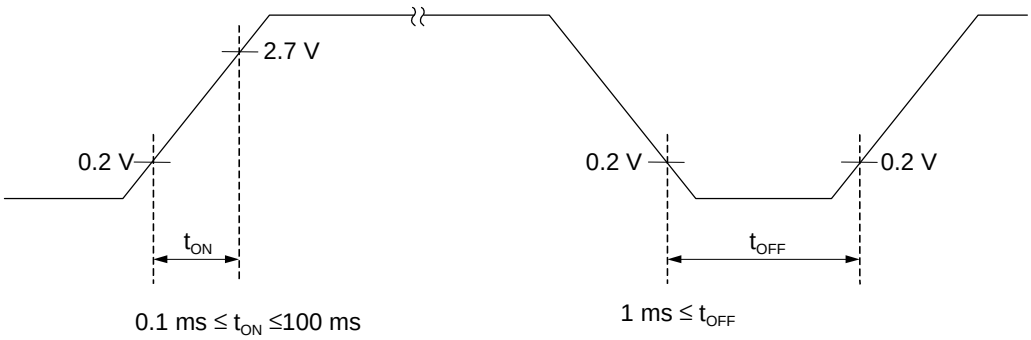


Figure 1 Power-on and Power-off Waveform

I/F with CPU

Parallel interface mode
The ML9041A can transfer either 8 bits once or 4 bits twice on the data bus for interfacing with any 8-bit or 4-bit microcontroller (CPU).

1) 8-bit interface data length
   The ML9041A uses all of the 8 data bus lines DB_0 to DB_7 at a time to transfer data to and from the CPU.

2) 4-bit interface data length
   The ML9041A uses only the higher-order 4 data bus lines DB_4 to DB_7 twice to transfer 8-bit data to and from the CPU.
   The ML9041A first transfers the higher-order 4 bits of 8-bit data (DB_4 to DB_7 in the case of 8-bit interface data length) and then the lower-order 4 bits of the data (DB_0 to DB_3 in the case of 8-bit interface data length).
   The lower-order 4 bits of data should always be transferred even when only the transfer of the higher-order 4 bits of data is required. (Example: Reading the Busy Flag)
   Two transfers of 4 bits of data complete the transfer of a set of 8-bit data. Therefore, when only one access is made, the following data transfer cannot be completed properly.

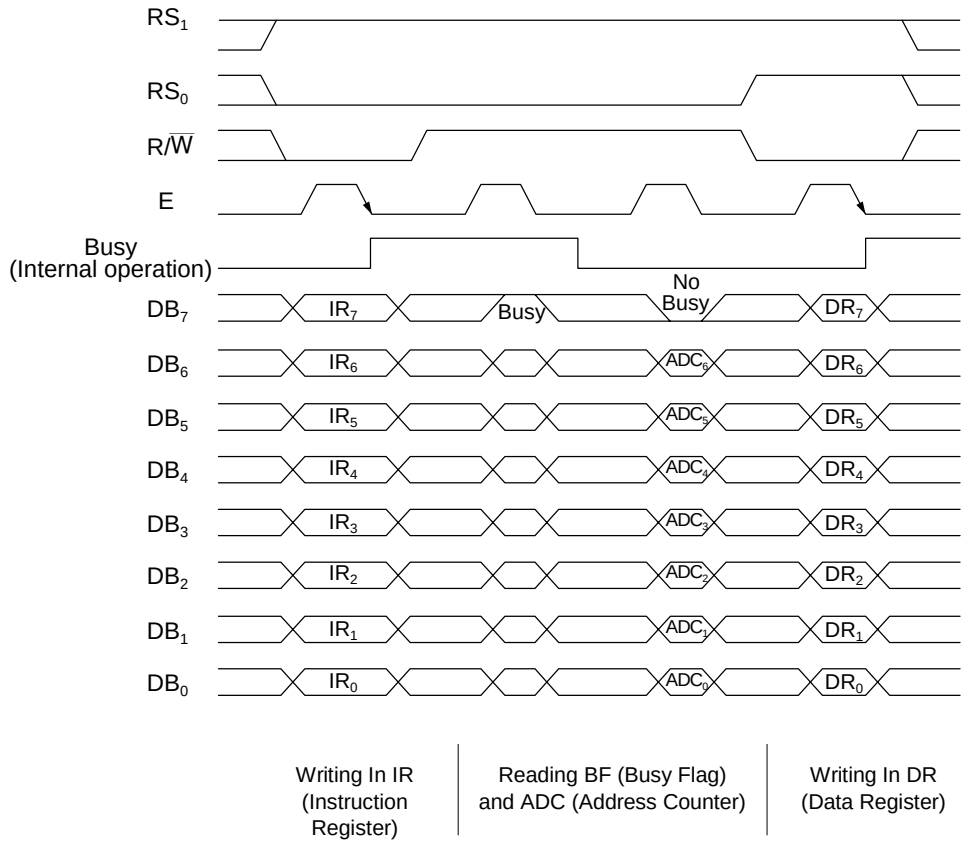


Figure 2 8-Bit Data Transfer

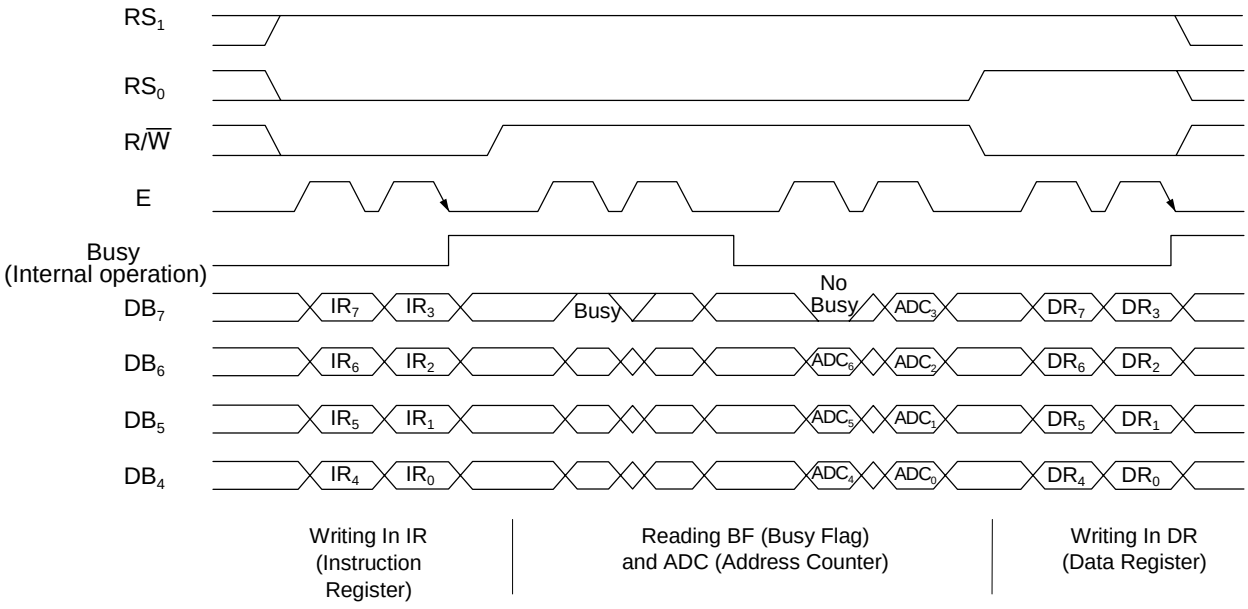


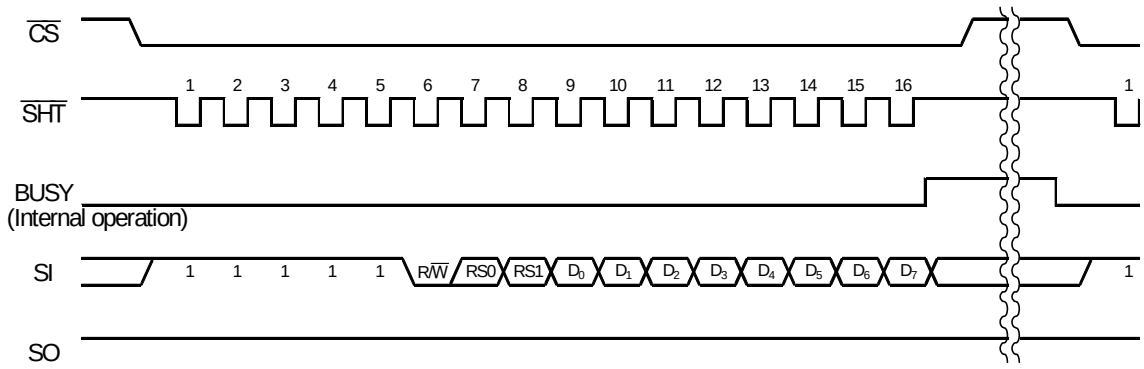
Figure 3 4-Bit Data Transfer

Serial Interface Mode

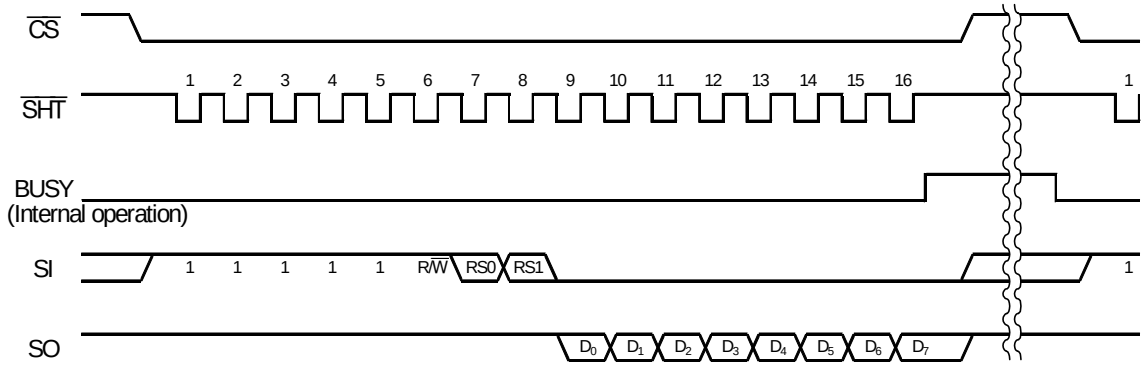
In the Serial I/F Mode, the ML9041A interfaces with the CPU via the $\overline{CS}$, $\overline{SHT}$, SI and SO pins.
Writing and reading operations are executed in units of 16 bits after the $\overline{CS}$ signal falls down. If the $\overline{CS}$ signal rises up before the completion of 16-bit unit access, this access is ignored.
When the BF bit is "1", the ML9041A cannot accept any other instructions. Before inputting a new instruction, check that the BF bit is "0". Any access when the BF bit is "1" is ignored.
Data format is LSB-first.

Examples of Access in the Serial I/F Mode

1) WRITE MODE



2) READ MODE



Note 1: Higher 5 bits of each instruction must be input at a "H" level.
Note 2: Lower 8 bits are "don't care" when the instructions in the READ MODE are set.
Note 3: After one instruction is input, the next instruction must be input after the $\overline{CS}$ pin is pulled at a "H" level.

Instruction Codes

Table of Instruction Codes

Instruction	Code											Function	Execution Time f = 270 kHz
	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Display Clear	1	0	0	0	0	0	0	0	0	0	1	Clears all the displayed digits of the LCD and sets the DDRAM address 0 in the address counter. The arbitrator data is cleared.	1.52 ms
Cursor Home	1	0	0	0	0	0	0	0	0	1	X	Sets the DDRAM address 0 in the address counter and shifts the display back to the original. The content of the DDRAM remains unchanged.	1.52 ms
Entry Mode Setting	1	0	0	0	0	0	0	0	1	I/D	S	Determines the direction of movement of the cursor and whether or not to shift the display. This instruction is executed when data is written or read.	37 µs
Display ON/OFF Control	1	0	0	0	0	0	0	1	D	C	B	Sets LCD display ON/OFF (D), cursor ON/OFF or cursor-position character blinking ON/OFF.	37 µs
Cursor/Display Shift	1	0	0	0	0	0	1	S/C	R/L	X	X	Moves the cursor or shifts the display without changing the content of the DDRAM.	37 µs
Function Setting	1	0	0	0	0	1	DL	N	F	X	X	Sets the interface data length (DL), the number of display lines (N) or the type of character font (F).	37 µs
CGRAM Address Setting	1	0	0	0	1	ACG						Sets on CGRAM address. After that, CGRAM data is transferred to and from the CPU.	37 µs
DDRAM Address Setting	1	0	0	1	ADD							Sets a DDRAM address. After that, DDRAM data is transferred to and from the CPU.	37 µs
Busy Flag/ Address Read	1	0	1	BF	ADC							Reads the Busy Flag (indicating that the ML9041A is operating) and the content of the address counter.	0 µs
RAM Data Write	1	1	0	WRITE DATA								Writes data in DDRAM, ABRAM or CGRAM.	37 µs
RAM Data Read	1	1	1	READ DATA								Reads data from DDRAM, ABRAM or CGRAM.	37 µs
Arbitrator Display Line Set	0	0	0	0	0	0	0	0	0	1	AS	Sets the arbitrator display line.	37 µs
Contrast Control Data Write	0	0	0	0	0	1	WRITE (Contrast Data) DATA					Writes data to control the contrast of the LCD.	37 µs
Contrast Control Data Read	0	0	1	0	0	0	READ (Contrast Data) DATA					Reads data to control the contrast of the LCD.	37 µs
ABRAM Address Setting	0	0	0	0	1	1	AAB					Sets an ABRAM address. After that, ABRAM data is transferred to and from the CPU.	37 µs
—	I/D = "1" (Increment) I/D = "0" (Decrement) S = "1" (Shifts the display.) S/C = "1" (Shifts display.) S/C = "0" (Moves the cursor.) R/L = "1" (Right shift) R/L = "0" (Left shift) D/L = "1" (8-bit data) DL = "0" (4-bit data) N = "1" (2 lines) N = "0" (1 line) F = "1" (5 x 10 dots) F = "0" (5 x 7 dots) BF = "1" (Busy) BF = "0" (Ready to accept an instruction) B = "1" (Enables blinking) C = "1" (Displays the cursor.) D = "1" (Displays a character pattern.) AS = "1" (Arbitrator Displays arbitrator on the upper line) AS = "0" (Arbitrator Displays arbitrator on the lower line)											DD RAM: Display data RAM CG RAM: Character generator RAM ABRAM: Arbitrator data RAM ACG: CGRAM address ADD: DDRAM address (Corresponds to the cursor address) AAB: ABRAM address ADC: Address counter (Used by DDRAM, ABRAM and CGRAM)	The execution time is dependent upon frequencies.

×: Don't Care

Instruction Codes

An instruction code is a signal sent from the CPU to access the ML9041A. The ML9041A starts operation as instructed by the code received. The busy status of the ML9041A is rather longer than the cycle time of the CPU, since the internal processing of the ML9041A starts at a timing which does not affect the display on the LCD. In the busy status (Busy Flag is "1"), the ML9041A cannot input the Busy Flag Read instruction only. Therefore, the CPU should ensure that the Busy Flag is "0" before sending an instruction code to the ML9041A.

1) Display Clear

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction Code:	1	0	0	0	0	0	0	0	0	0	1

When this instruction is executed, the LCD display including arbitrator display is cleared and the I/D entry mode is set to "Increment". The value of "S" (Display shifting) remains unchanged. The position of the cursor or blink being displayed moves to the left end of the LCD (or the left end of the line 1 in the 2-line display mode).

Note: All DDRAM and ABRAM data turn to "20" and "00" in hexadecimal, respectively. The value of the address counter (ADC) turns to the one corresponding to the address "00" (hexadecimal) of the DDRAM.
The execution time of this instruction is 1.52 ms (maximum) at an oscillation frequency of 270 kHz.

2) Cursor Home

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	0	0	0	0	0	0	0	1	×

×: Don't Care

When this instruction is executed, the cursor or blink position moves to the left end of the LCD (or the left end of line 1 in the 2-line display mode). If the display has been shifted, the display returns to the original display position before shifting.

Note: The value of the address counter (ADC) goes to the one corresponding to the address "00" (hexadecimal) of the DDRAM).
The execution time of this instruction is 1.52 ms (maximum) at an oscillation frequency of 270 kHz.

3) Entry Mode Setting

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	0	0	0	0	0	0	1	I/D	S

(1) When the I/D is set, the cursor or blink shifts to the right by 1 character position (ID= "1"; increment) or to the left by 1 character position (I/D= "0"; decrement) after an 8-bit character code is written to or read from the DDRAM. At the same time, the address counter (ADC) is also incremented by 1 (when I/D = "1"; increment) or decremented by 1 (when I/D = "0"; decrement). After a character pattern is written to or read from the CGRAM, the address counter (ADC) is incremented by 1 (when I/D = "1"; increment) or decremented by 1 (when I/D = "0"; decrement).
Also after data is written to or read from the ABRAM, the address counter (ADC) is incremented by 1 (when I/D = "1"; increment) or decremented by 1 (when I/D = "0"; decrement).

(2) When S = "1", the cursor or blink stops and the entire display shifts to the left (I/D = "1") or to the right (I/D = "0") by 1 character position after a character code is written to the DDRAM.
In the case of S = "1", when a character code is read from the DDRAM, when a character pattern is written to or read from the CGRAM or when data is written to or read from the ABRAM, normal read/write is carried out without shifting of the entire display. (The entire display does not shift, but the cursor or blink shifts to the right (I/D = "1") or to the left (I/D = "0") by 1 character position.)
When S = "0", the display does not shift, but normal write/read is performed.

Note: The execution time of this instruction is 37 μs (maximum) at an oscillation frequency of 270 kHz.

4) Display ON/OFF Control

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	0	0	0	0	0	1	D	C	B

(1) The "D" bit (DB2) of this instruction determines whether or not to display character patterns on the LCD.
When the "D" bit is "1", character patterns are displayed on the LCD.
When the "D" bit is "0", character patterns are not displayed on the LCD and the cursor/blinking also disappear.

Note: Unlike the Display Clear instruction, this instruction does not change the character code in the DDRAM and ABRAM.

(2) When the "C" bit (DB1) is "0", the cursor turns off. When both the "C" and "D" bits are "1", the cursor turns on.

(3) When the "B" bit (DB0) is "0", blinking is canceled. When both the "B" and "D" bits are "1", blinking is performed.
In the Blinking mode, all dots including those of the cursor, the character pattern and the cursor are alternately displayed.

Note: The execution time of this instruction is 37 μs (maximum) at an oscillation frequency of 270 kHz.

5) Cursor/Display Shift

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	0	0	0	0	1	S/C	R/L	×	×

×: Don't Care

S/C = "0", R/L = "0" This instruction shifts left the cursor and blink positions by 1 (decrements the content of the ADC by 1).

S/C = "0", R/L = "1" This instruction shifts right the cursor and blink positions by 1 (increments the content of the ADC by 1).

S/C = "1", R/L = "0" This instruction shifts left the entire display by 1 character position. The cursor and blink positions move to the left together with the entire display. The Arbitrator display is not shifted. (The content of the ADC remains unchanged.)

S/C = "1", R/L = "1" This instruction shifts right the entire display by 1 character position. The cursor and blink positions move to the right together with the entire display. The Arbitrator display is not shifted. (The content of the ADC remains unchanged.)

In the 2-line mode, the cursor or blink moves from the first line to the second line when the cursor at digit 40 (27; hex) of the first line is shifted right.
When the entire display is shifted, the character pattern, cursor or blink will not move between the lines (from line 1 to line 2 or vice versa).

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

6) Function Setting

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	0	0	0	1	DL	N	F	×	×

×: Don't Care

(1) When the "DL" bit (DB_4) of this instruction is "1", the data transfer to and from the CPU is performed once by the use of 8 bits DB_7 to DB_0.
When the "DL" bit (DB_4) of this instruction is "0", the data transfer to and from the CPU is performed twice by the use of 4 bits DB_7 to DB_4.

(2) The 2-line display mode is selected when the "N" bit (DB_3) of this instruction is "1". The 1-line display mode is selected when the "N" bit is "0".

(3) The character font represented by 5×7 dots is selected when the "F" bit (DB_2) of this instruction is "1". The character font represented by 5×10 dots is selected when the "F" bit is "1" and the "N" bit is "0".
After the ML9041A is powered on, this function setting should be carried out before execution of any instruction except the Busy Flag Read. After this function setting, no instructions other than the DL Set instruction can be executed. In the Serial I/F Mode, DL setting is ignored.

N	F	Number of display lines	Font size	Duty	Number of biases	Number of common signals
0	0	1	5×7	1/9	4	9
0	1	1	5×10	1/12	4	12
1	0	2	5×7	1/17	5	17
1	1	2	5×7	1/17	5	17

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

7) CGRAM Address Setting

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	0	0	1	C_5	C_4	C_3	C_2	C_1	C_0

This instruction sets the CGRAM address to the data represented by the bits C_5 to C_0 (binary).
The CGRAM addresses are valid until DDRAM or ABRAM addresses are set.
The CPU writes or reads character patterns starting from the one represented by the CGRAM address bits C_5 to C_0 set in the instruction code at that time.

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

8) DDRAM Address Setting

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	0	1	D_6	D_5	D_4	D_3	D_2	D_1	D_0

This instruction sets the DDRAM address to the data represented by the bits D_6 to D_0 (binary).
The DDRAM addresses are valid until CGRAM or ABRAM addresses are set.
The CPU writes or reads character codes starting from the one represented by the DDRAM address bits D_6 to D_0 set in the instruction code at that time.
In the 1-line mode (the “N” bit is “0”), the DDRAM address represented by bits D_6 to D_0 (binary) should be in the range “00” to “4F” in hexadecimal.
In the 2-line mode (the “N” bit is “1”), the DDRAM address represented by bits D_6 to D_0 (binary) should be in the range “00” to “27” or “40” to “67” in hexadecimal.
If an address other than above is input, the ML9041A cannot properly write a character code in or read it from the DDRAM.

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

9) DDRAM/ABRAM/CGRAM Data Write

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	1	0	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0

A character code (E_7 to E_0) is written to the DDRAM, Display-ON data (E_7 to E_0) to the ABRAM or a character pattern (E_7 to E_0) to the CGRAM.
The DDRAM, ABRAM or CGRAM is selected at the preceding address setting.
After data is written, the address counter (ADC) is incremented or decremented as set by the Entry Mode Setting instruction (see 3).

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

10) Busy Flag/Address Counter Read (Execution time: 0 μs)

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	1	BF	O_6	O_5	O_4	O_3	O_2	O_1	O_0

The "BF" bit (DB7) of this instruction tells whether the ML9041A is busy in internal operation (BF = "1") or not (BF = "0").
When the "BF" bit is "1", the ML9041A cannot accept any other instructions. Before inputting a new instruction, check that the "BF" bit is "0".
When the "BF" bit is "0", the ML9041A outputs the correct value of the address counter. The value of the address counter is equal to the DDRAM, ABRAM or CGRAM address. Which of the DDRAM, ABRAM and CGRAM addresses is set in the counter is determined by the preceding address setting.
When the "BF" bit is "1", the value of the address counter is not always correct because it may have been incremented or decremented by 1 during internal operation.

11) DDRAM/ABRAM/CGRAM Data Read

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	1	1	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

A character code (P_7 to P_0) is read from the DDRAM, Display-ON data (P_7 to P_0) from the ABRAM or a character pattern (P_7 to P_0) from the CGRAM.
The DDRAM, ABRAM or CGRAM is selected at the preceding address setting.
After data is read, the address counter (ADC) is incremented or decremented as set by the Entry Mode Setting instruction (see 3).

Note: Conditions for reading correct data

(1) The DDRAM, ABRAM or CGRAM Setting instruction is input before this data read instruction is input.

(2) When reading a character code from the DDRAM, the Cursor/Display Shift instruction (see 5) is input before this Data Read instruction is input.

(3) When two or more consecutive RAM Data Read instructions are executed, the following read data is correct.
Correct data is not output under conditions other than the cases (1), (2) and (3) above.

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

Expansion Instruction Codes

The busy status of the ML9041A is rather longer than the cycle time of the CPU, since the internal processing of the ML9041A starts at a timing which does not affect the display on the LCD. In the busy status (Busy Flag is "1"), the ML9041A executes the Busy Flag Read instruction only. Therefore, the CPU should ensure that the Busy Flag is "0" before sending an expansion instruction code to the ML9041A.

1) Arbitrator Display Line Set

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Expansion instruction code:	0	0	0	0	0	0	0	0	0	1	AS

This expansion instruction code sets the Arbitrator display line. The relationship between the status of this bit and the common outputs is as follows:
For display examples, refer to LCD Drive Waveforms section.

CSR	duty	AS bit	Shift direction	Arbitrator's common pin
L	1/9	L	COM1→COM9	COM9
L	1/9	H	COM1→COM9	COM1
L	1/12	L	COM1→COM12	COM12
L	1/12	H	COM1→COM12	COM1
L	1/17	L	COM1→COM17	COM17
L	1/17	H	COM1→COM17	COM1
H	1/9	L	COM9→COM1	COM1
H	1/9	H	COM9→COM1	COM9
H	1/12	L	COM12→COM1	COM1
H	1/12	H	COM12→COM1	COM12
H	1/17	L	COM17→COM1	COM1
H	1/17	H	COM17→COM1	COM17

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

2) Contrast Adjusting Data Write

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Expansion instruction code:	0	0	0	0	0	1	F_4	F_3	F_2	F_1	F_0

This instruction writes contrast adjusting data (F_4 to F_0) to the contrast register.
After contrast adjusting data is written in the register, the potential (VLCD) output to the V_5 pin varies according to the data written.
The VLCD becomes maximum when the content of the contrast register is "1F" (hexadecimal) and becomes minimum when it is "00" (hexadecimal).

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

3) Contrast Adjusting Data Read

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Expansion instruction code:	0	0	1	0	0	0	G_4	G_3	G_2	G_1	G_0

This instruction reads contrast adjusting data (G_4 to G_0) from the contrast register.

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

4) ABRAM Address Setting

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Expansion instruction code:	0	0	1	0	1	1	H_4	H_3	H_2	H_1	H_0

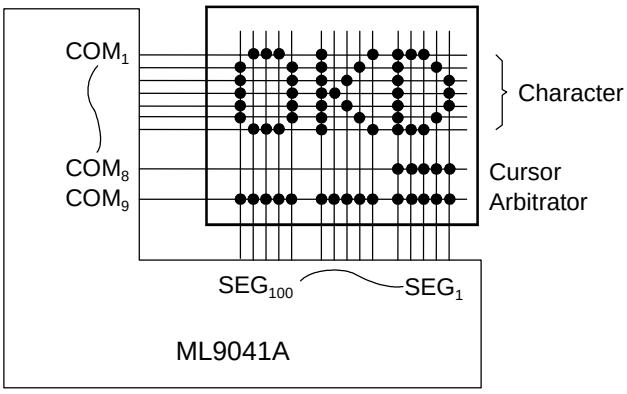
This instruction sets the ABRAM address to the data represented by the bits H_4 to H_0 (binary).
The ABRAM addresses are valid until CGRAM or DDRAM addresses are set.
The CPU writes or reads the Display-ON data starting from the one represented by the ABRAM address bits H_4 to H_0 set in the instruction code at that time.
When the ABRAM address represented by bits H_4 to H_0 (binary) is in the range “00” to “13” in hexadecimal, data is output to the LCD as the arbitrator.

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

Examples of Combinations of ML9041A and LCD Panel

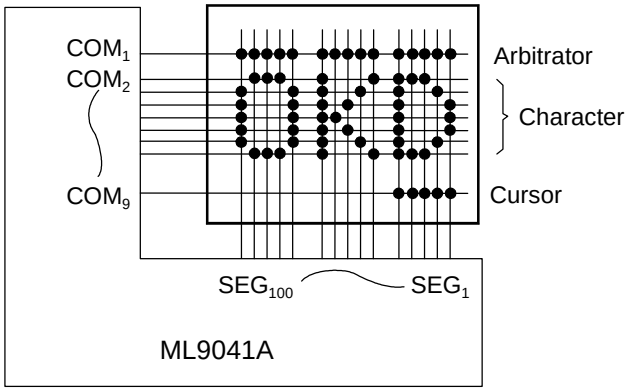
(1) Driving the LCD of one 20-character line under the conditions of the 1-line display mode and the character font of 5 × 7 dots

(1/9 duty, AS = "0", CSR = "L", SSR = "H")



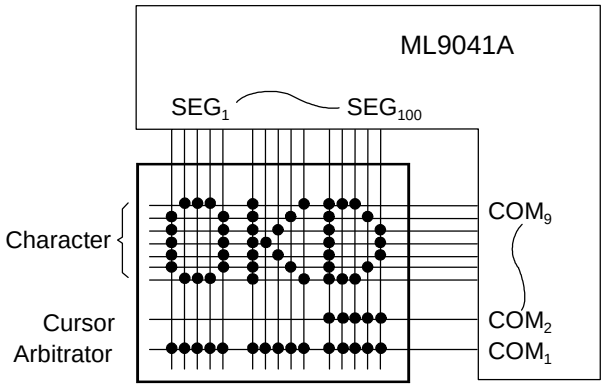
- COM_{10} to COM_{17} output Display-OFF common signals.

(1/9 duty, AS = "1", CSR = "L", SSR = "H")



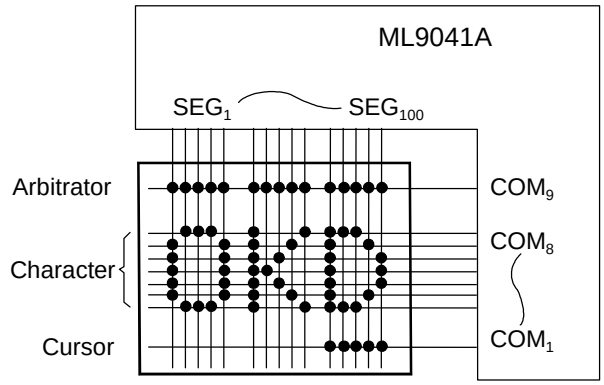
- COM_{10} to COM_{17} output Display-OFF common signals.

(1/9 duty, AS = “0”, CSR = “H”, SSR = “L”)



- COM_{10} to COM_{17} output Display-OFF common signals.

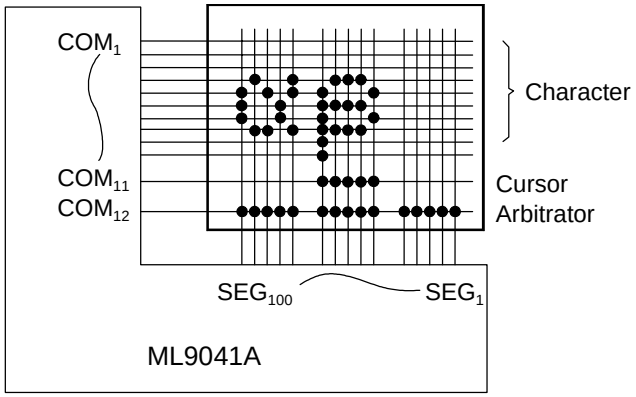
(1/9 duty, AS = “1”, CSR = “H”, SSR = “L”)



- COM_{10} to COM_{17} output Display-OFF common signals.

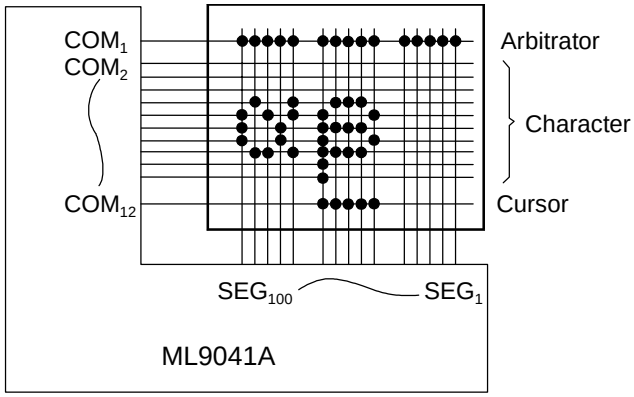
(2) Driving the LCD of one 20-character line under the conditions of the 1-line display mode and the character font of 5 × 10 dots

(1/12 duty, AS = “0”, CSR = “L”, SSH = “H”)



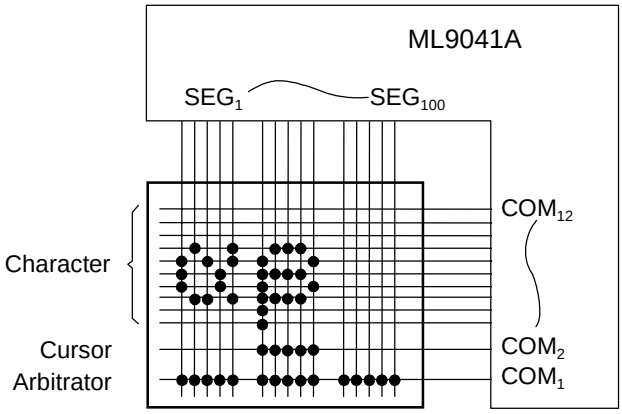
- COM_{13} to COM_{17} output Display-OFF common signals.

(1/12 duty, AS = “1”, CSR = “L”, SSR = “H”)



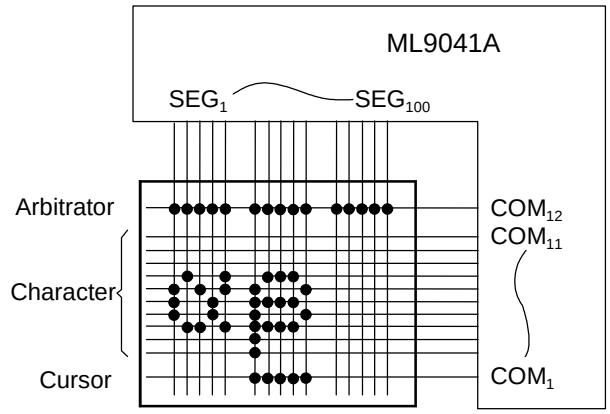
- COM_{13} to COM_{17} output Display-OFF common signals.

(1/12 duty, AS = “0”, CSR = “H”, SSR = “L”)



- COM_{13} to COM_{17} output Display-OFF common signals.

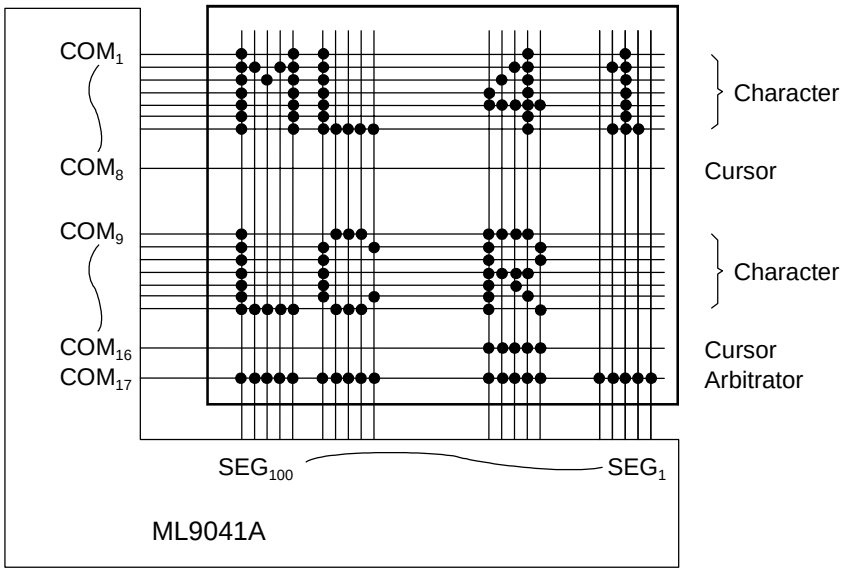
(1/12 duty, AS = “1”, CSR = “H”, SSR = “L”)



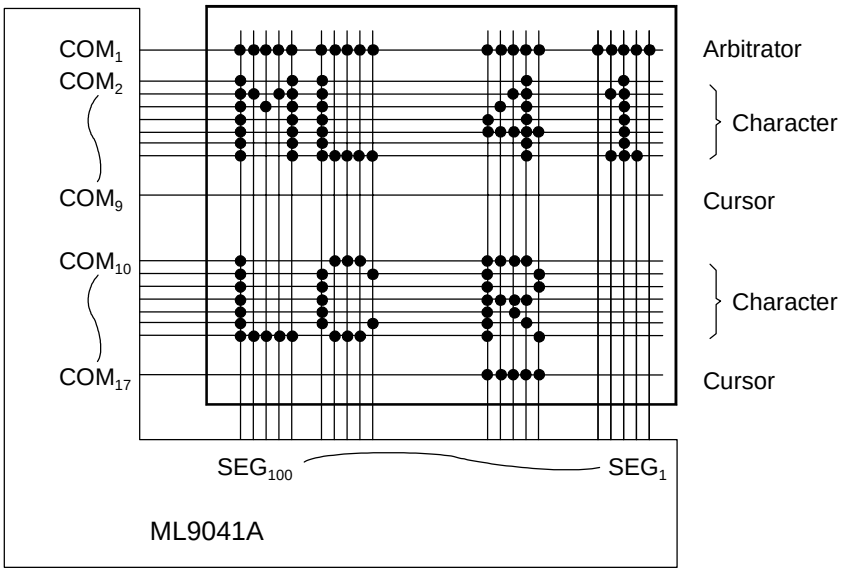
- COM_{13} to COM_{17} output Display-OFF common signals.

(3) Driving the LCD of two 20-character lines under the conditions of the 2-line display mode and the character font of 5 × 7 dots

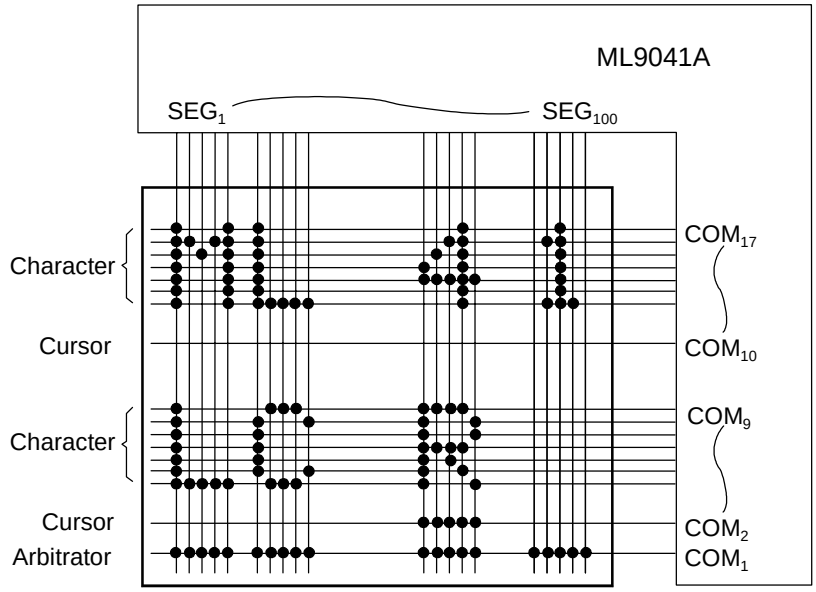
(1/17 duty, AS = “0”, CSR = “L”, SSR = “H”)



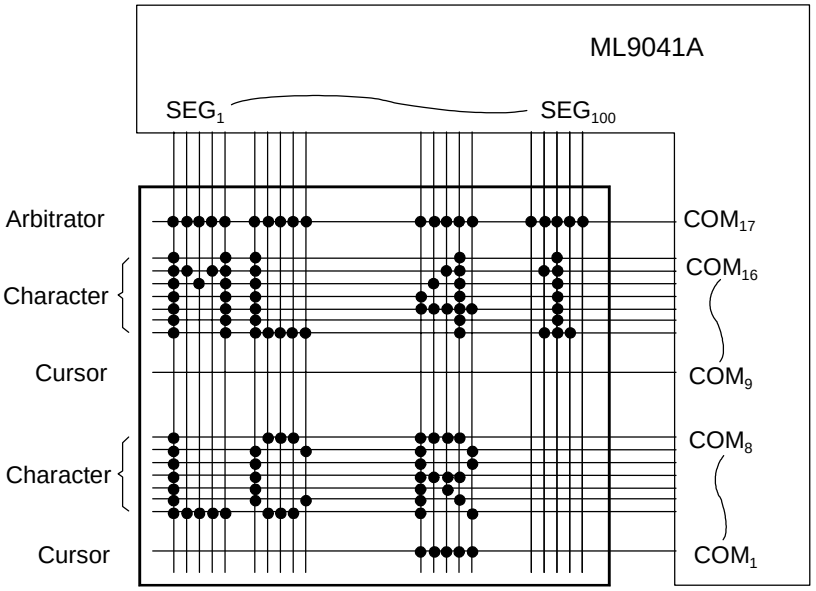
(1/17 duty, AS = “1”, CSR = “L”, SSR = “H”)



(1/17 duty, AS = “0”, CSR = “H”, SSR = “L”)

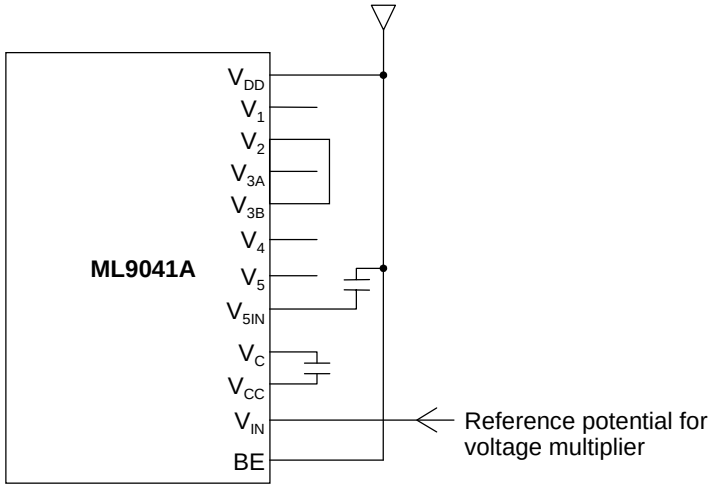


(1/17 duty, AS = “1”, CSR = “H”, SSR = “L”)

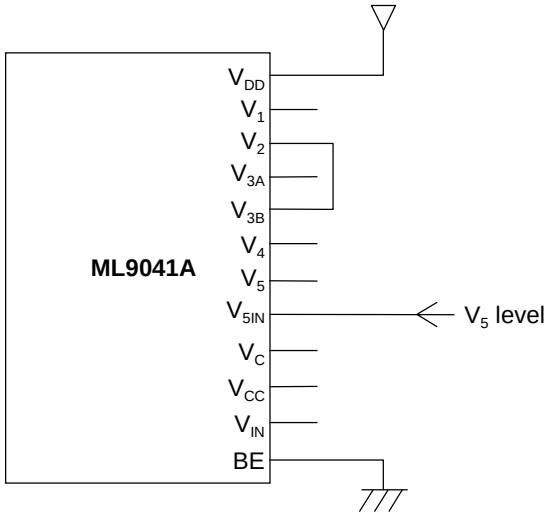


EXAMPLES OF VLCD GENERATION CIRCUITS

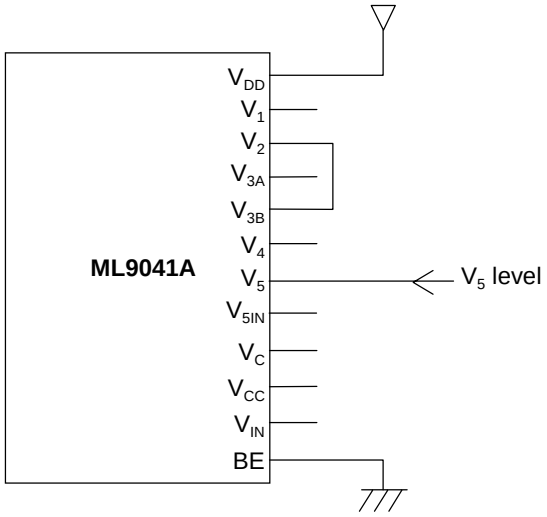
- With 1/4bias, a built-in contrast adjusting circuit and a voltage multiplier



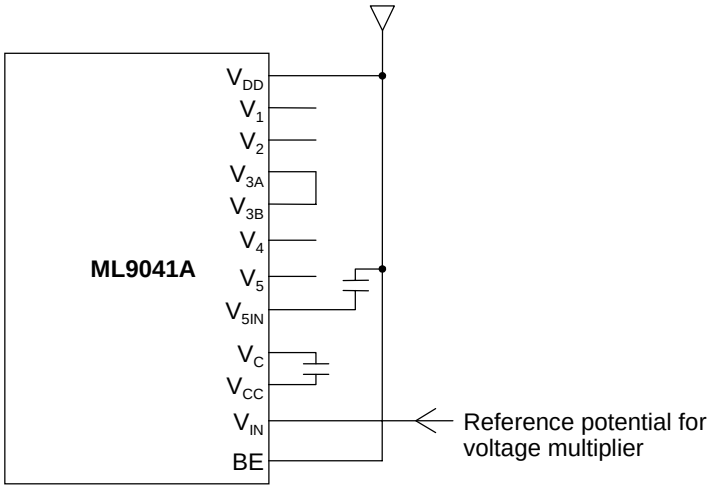
- With 1/4 bias, a built-in contrast adjusting circuit and the V_5 level input from an external circuit



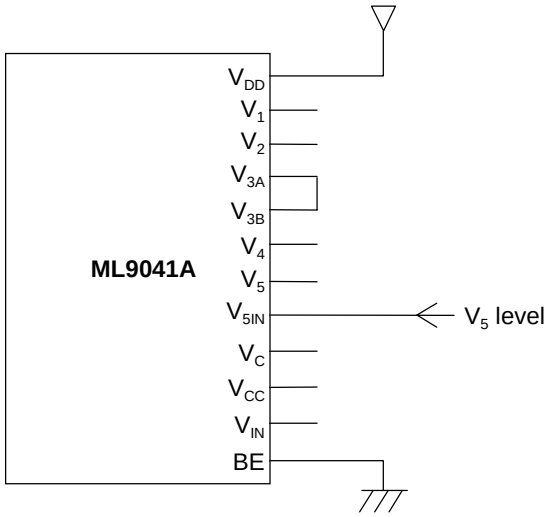
- With 1/4 bias, no built-in contrast adjusting circuit and the V_5 level input from an external circuit



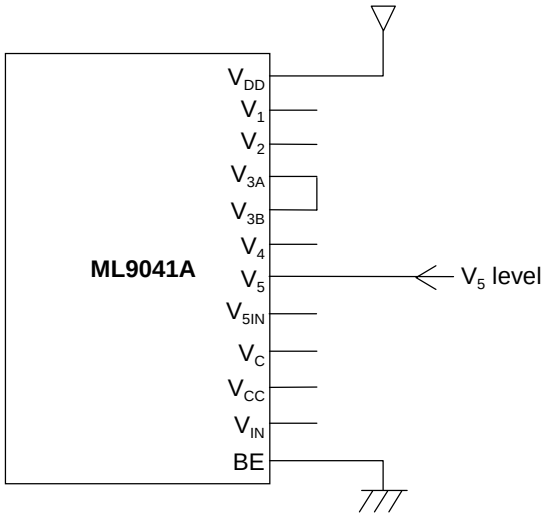
- With 1/5 bias, a built-in contrast adjusting circuit and a voltage multiplier



- With 1/5 bias, a built-in contrast adjusting circuit and the V_5 level input from an external circuit



- With 1/5 bias, no built-in contrast adjusting circuit and the V_5 level input from an external circuit



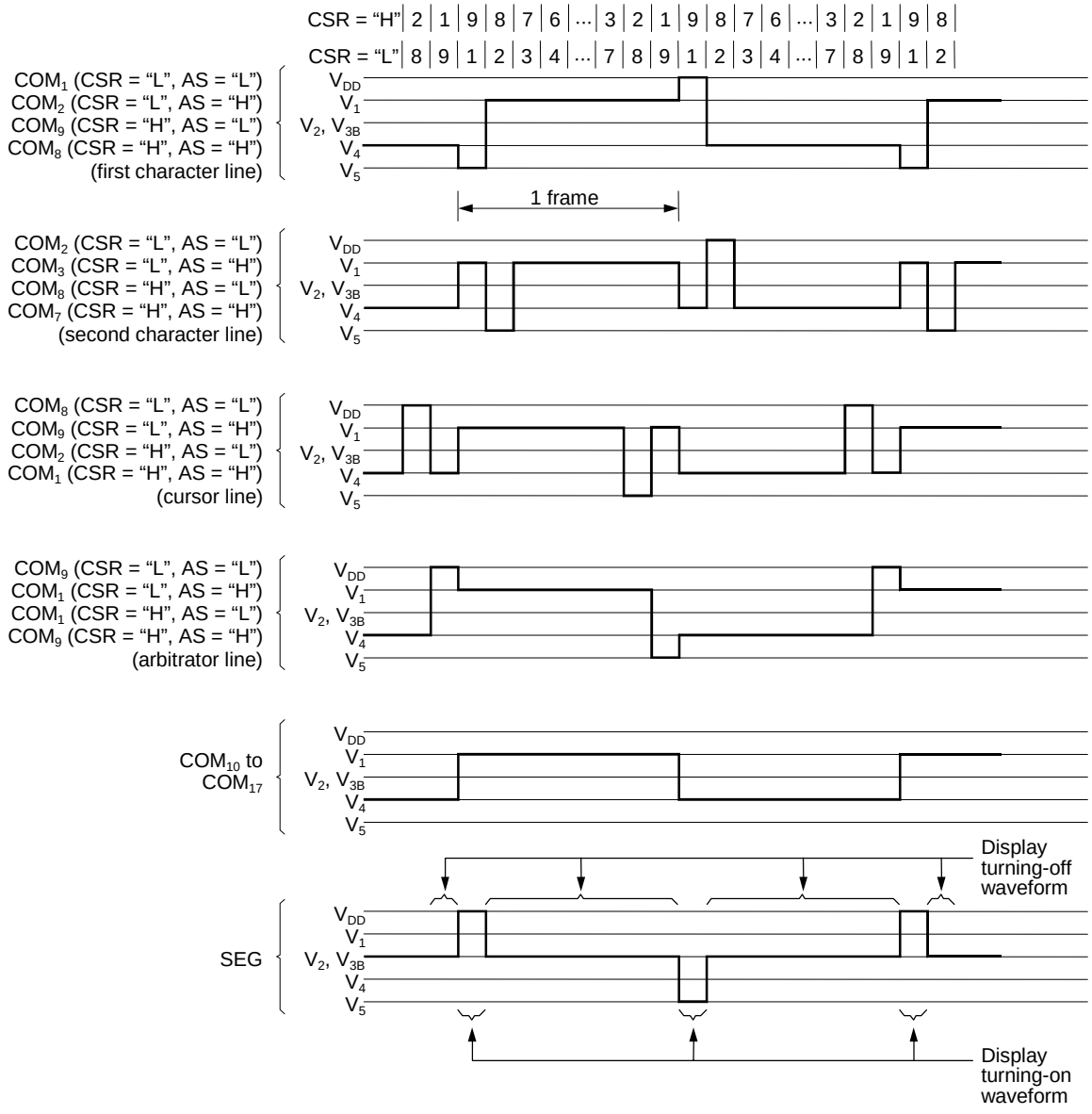
LCD Drive Waveforms

The COM and SEG waveforms (AC signal waveforms for display) vary according to the duty (1/9, 1/12 and 1/17 duties). See 1) to 3) below.
The relationship between the duty ratio and the frame frequency is as follows:

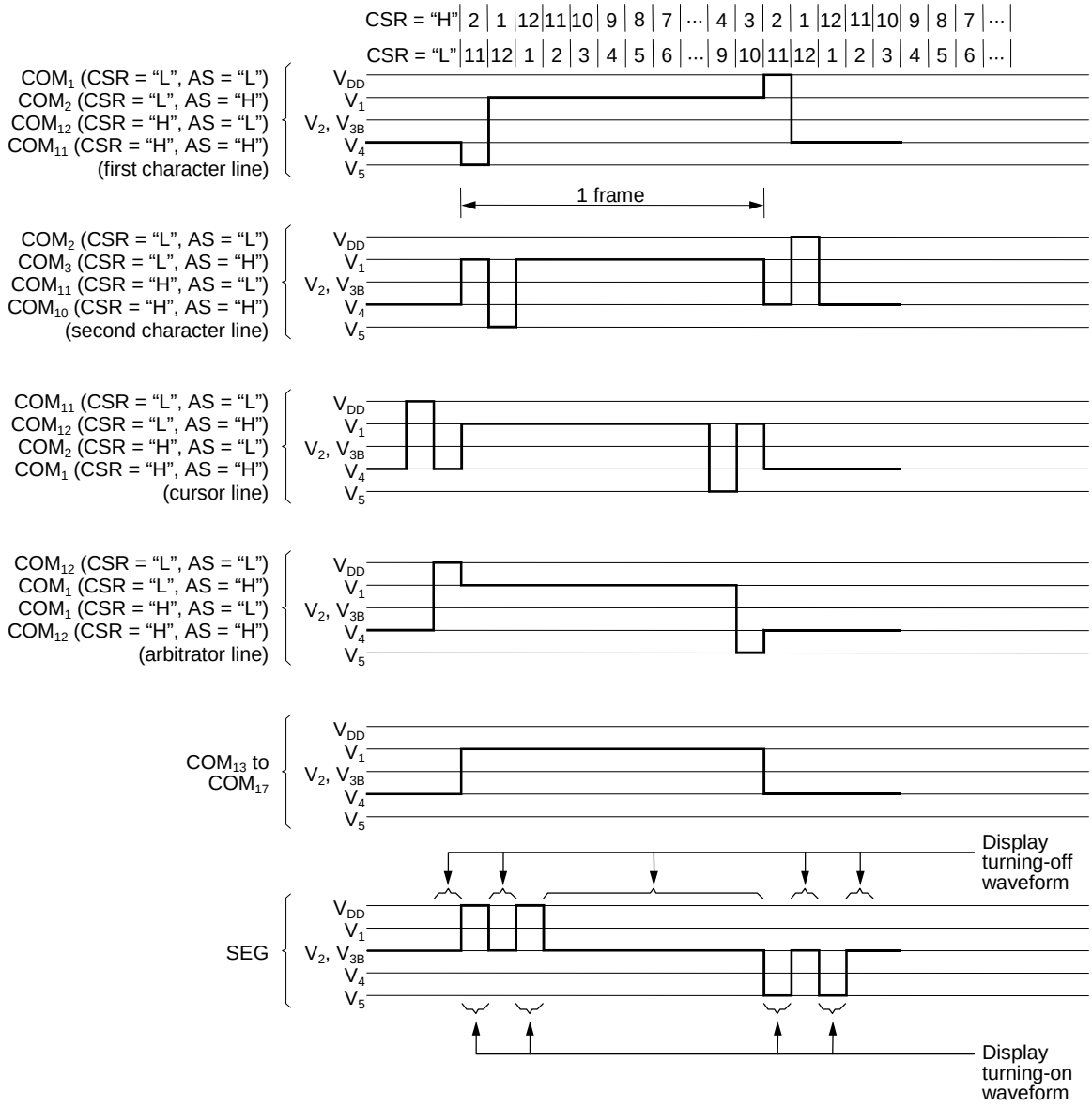
Duty ratio	Frame Frequency
1/9	75.0 Hz
1/12	56.3 Hz
1/17	79.4 Hz

Note: At an oscillation frequency (OSC) of 270 kHz

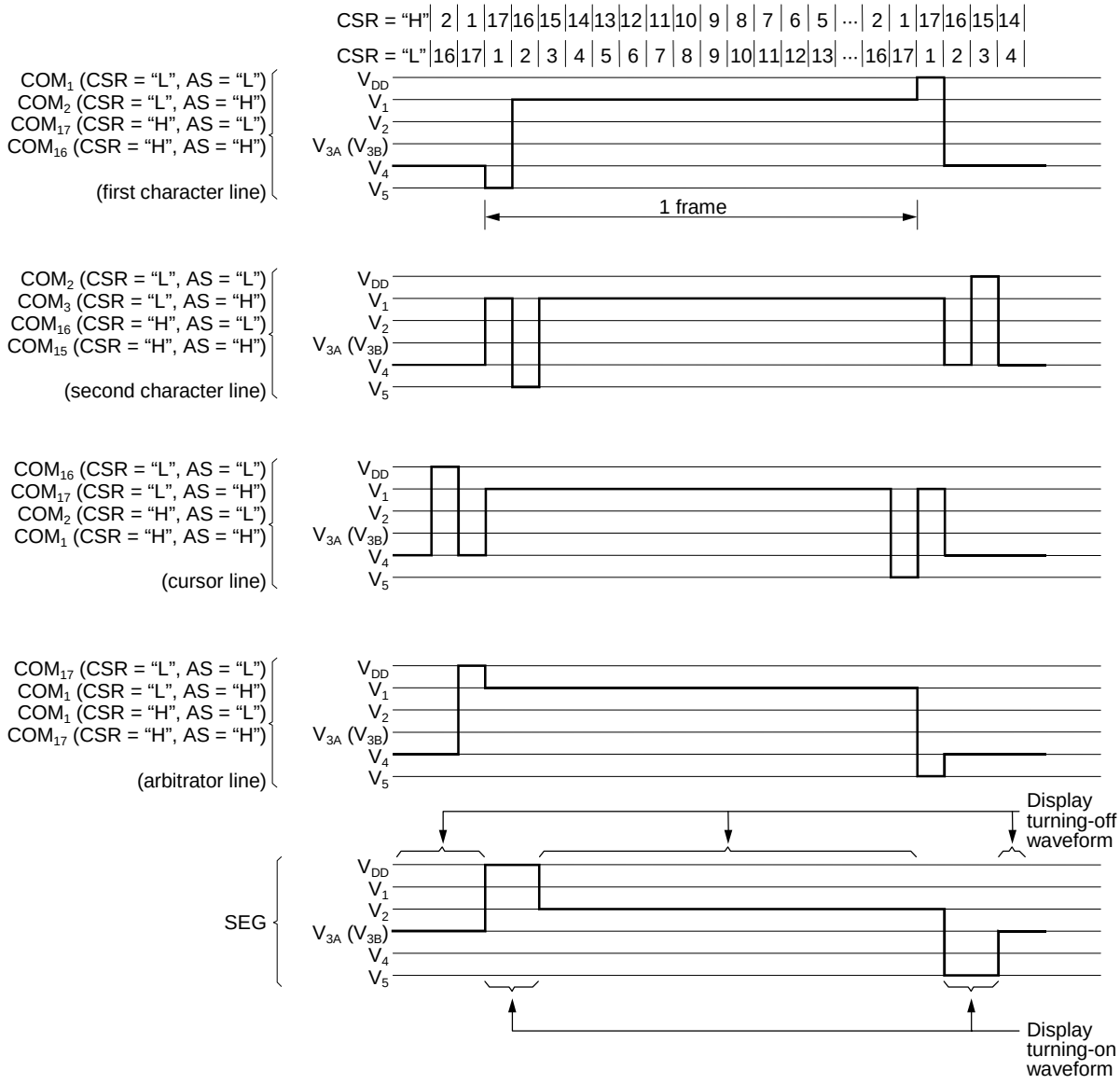
1) COM and SEG Waveforms on 1/9 Duty



2) COM and SEG Waveforms on 1/12 Duty



3) COM and SEG Waveforms on 1/17 Duty



Initial Setting of Instructions

(a) Data transfer from and to the CPU using 8 bits of DB_0 to DB_7

1) Turn on the power.
2) Wait for 15 ms or more after V_{DD} has reached 2.7 V or higher.
3) Set “8 bits” with the Function Setting instruction.
4) Wait for 4.1 ms or more.
5) Set “8 bits” with the Function Setting instruction.
6) Wait for 100 μs or more.
7) Set “8 bits” with the Function Setting instruction.
8) Check the Busy Flag for No Busy (or wait for 100 μs or more).
9) Set “8 bits”, “Number of LCD lines” and “Font size” with the Function Setting instruction. (After this, the number of LCD lines and the font size cannot be changed.)
10) Check the Busy Flag for No Busy.
11) Execute the Display ON/OFF control Instruction, Display Clear Instruction, Entry Mode Setting instruction and Arbitrator Display Line Setting Instruction.
12) Check the Busy Flag for No Busy.
13) Initialization is completed.

An example of instruction code for 3), 5) and 7)

RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	0	0	0	0	1	1	×	×	×	×

×: Don’t Care

(b) Data transfer from and to the CPU using 4 bits of DB_4 to DB_7

1) Turn on the power.
2) Wait for 15 ms or more after V_{DD} has reached 2.7 V or higher.
3) Set “8 bits” with the Function Setting instruction.
4) Wait for 4.1 ms or more.
5) Set “8 bits” with the Function Setting instruction.
6) Wait for 100 μs or more.
7) Set “8 bits” with the Function Setting instruction.
8) Check the Busy Flag for No Busy (or wait for 100 μs or longer).
9) Set “4 bits” with the Function Setting instruction.
10) Wait for 100 μs or longer.
11) Set “4 bits”, “Number of LCD lines” and “Font size” with the Function Setting instruction. (After this, the number of LCD lines and the font size cannot be changed.)
12) Check the Busy Flag for No Busy.
13) Execute the Display ON/OFF control Instruction, Display Clear Instruction, Entry Mode Setting instruction and Arbitrator Display Line Setting Instruction.
14) Check the Busy Flag for No Busy.
15) Initialization is completed.

An example of instruction code for 3), 5) and 7)

RS_1	RS_0	R/W	DB_7	DB_6	DB_5	DB_4
1	0	0	0	0	1	1

An example of instruction code for 9)

RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4
1	0	0	0	0	1	0

*: From 11), input data twice by the use of 4-bit data.
*: In 13), check the Busy Flag for No Busy before executing each instruction.

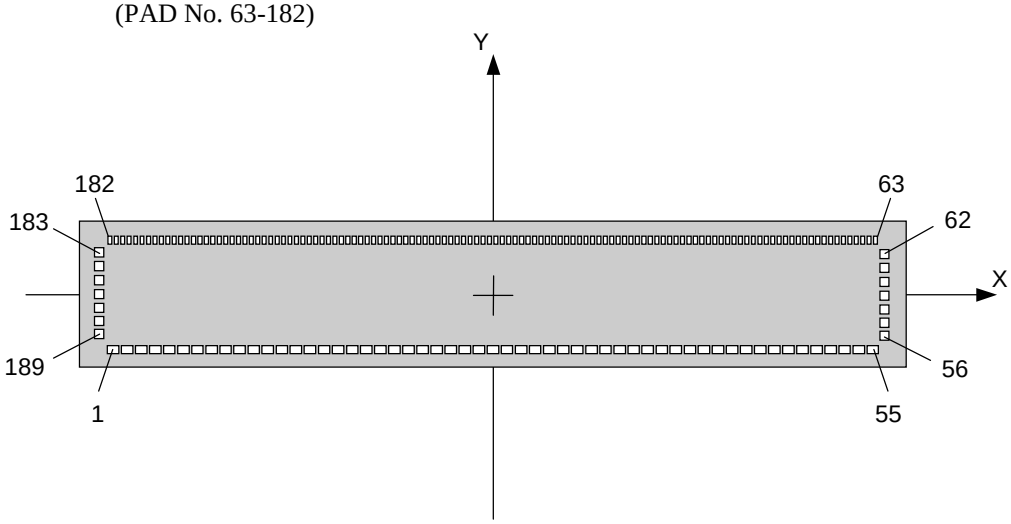
(c) Data transfer from and to the CPU using the serial I/F
1) Turn on the power.
2) Wait for 15 ms or more after V_{DD} has reached 2.7 V or higher.
3) Check the busy flag for No Busy.
4) Set “Number of LCD lines” and “Font size” with the Function Setting Instruction. (After this, the number of LCD lines and the font size cannot be changed.)
5) Check the busy flag for No Busy.
6) Execute the Display ON/OFF control Instruction, the Display Clear Instruction, the Entry Mode Instruction and the Arbitrator Display Line Setting Instruction.
7) Check the busy flag for No Busy.
8) Initialization is completed.

*: In 6), check the Busy Flag for No Busy before executing each instruction.

ML9041A-xxA CVWA PAD CONFIGURATION

Pad Layout

Chip Size: 10.62 × 2.55 mm
Chip Thickness: 625±20 µm
Bump Size (1): 72 × 72 µm
(PAD No. 1-62, 183-189)
Bump Size (2): 54 × 96 µm
(PAD No. 63-182)



Pad Coordinates

Pad	Symbol	X (µm)	Y (µm)	Pad	Symbol	X (µm)	Y (µm)
1	V_1	–5103	–1100	21	DB_3	–1323	–1100
2	V_2	–4914	–1100	22	DB_2	–1134	–1100
3	V_{3A}	–4725	–1100	23	DB_1	–945	–1100
4	V_{3B}	–4536	–1100	24	DB_0	–756	–1100
5	V_4	–4347	–1100	25	E	–567	–1100
6	V_5	–4158	–1100	26	R/$\overline{W}$	–378	–1100
7	V_{5IN}	–3969	–1100	27	RS_0	–189	–1100
8	V_{CC}	–3780	–1100	28	RS_1	0	–1100
9	V_C	–3591	–1100	29	SO	189	–1100
10	V_{IN}	–3402	–1100	30	SI	378	–1100
11	BE	–3213	–1100	31	$\overline{SHT}$	567	–1100
12	V_{DD}	–3024	–1100	32	$\overline{CS}$	756	–1100
13	CSR	–2835	–1100	33	OSC_2	945	–1100
14	SSR	–2646	–1100	34	OSC_R	1134	–1100
15	S/$\overline{P}$	–2457	–1100	35	OSC_1	1323	–1100
16	V_{SS}	–2268	–1100	36	T_3	1512	–1100
17	DB_7	–2079	–1100	37	T_2	1701	–1100
18	DB_6	–1890	–1100	38	T_1	1890	–1100
19	DB_5	–1701	–1100	39	COM_1	2079	–1100
20	DB_4	–1512	–1100	40	COM_2	2268	–1100

Pad	Symbol	X (µm)	Y (µm)
41	COM_3	2457	–1100
42	COM_4	2646	–1100
43	COM_5	2835	–1100
44	COM_6	3024	–1100
45	COM_7	3213	–1100
46	COM_8	3402	–1100
47	COM_9	3591	–1100
48	COM_{10}	3780	–1100
49	COM_{11}	3969	–1100
50	COM_{12}	4158	–1100
51	COM_{13}	4347	–1100
52	COM_{14}	4536	–1100
53	COM_{15}	4725	–1100
54	COM_{16}	4914	–1100
55	COM_{17}	5103	–1100
56	DUMMY	5184	–720
57	DUMMY	5184	–480
58	DUMMY	5184	–240
59	DUMMY	5184	0
60	DUMMY	5184	240
61	DUMMY	5184	480
62	DUMMY	5184	720
63	DUMMY	4998	1088
64	DUMMY	4914	1088
65	DUMMY	4830	1088
66	DUMMY	4746	1088
67	DUMMY	4662	1088
68	DUMMY	4578	1088
69	DUMMY	4494	1088
70	DUMMY	4410	1088
71	DUMMY	4326	1088
72	DUMMY	4242	1088
73	SEG_{100}	4158	1088
74	SEG_{99}	4074	1088
75	SEG_{98}	3990	1088
76	SEG_{97}	3906	1088
77	SEG_{96}	3822	1088
78	SEG_{95}	3738	1088
79	SEG_{94}	3654	1088
80	SEG_{93}	3570	1088

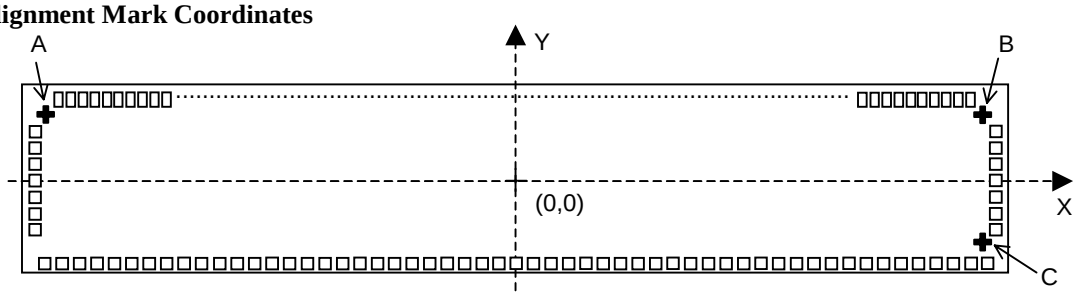
Pad	Symbol	X (µm)	Y (µm)
81	SEG_{92}	3486	1088
82	SEG_{91}	3402	1088
83	SEG_{90}	3318	1088
84	SEG_{89}	3234	1088
85	SEG_{88}	3150	1088
86	SEG_{87}	3066	1088
87	SEG_{86}	2982	1088
88	SEG_{85}	2898	1088
89	SEG_{84}	2814	1088
90	SEG_{83}	2730	1088
91	SEG_{82}	2646	1088
92	SEG_{81}	2562	1088
93	SEG_{80}	2478	1088
94	SEG_{79}	2394	1088
95	SEG_{78}	2310	1088
96	SEG_{77}	2226	1088
97	SEG_{76}	2142	1088
98	SEG_{75}	2058	1088
99	SEG_{74}	1974	1088
100	SEG_{73}	1890	1088
101	SEG_{72}	1806	1088
102	SEG_{71}	1722	1088
103	SEG_{70}	1638	1088
104	SEG_{69}	1554	1088
105	SEG_{68}	1470	1088
106	SEG_{67}	1386	1088
107	SEG_{66}	1302	1088
108	SEG_{65}	1218	1088
109	SEG_{64}	1134	1088
110	SEG_{63}	1050	1088
111	SEG_{62}	966	1088
112	SEG_{61}	882	1088
113	SEG_{60}	798	1088
114	SEG_{59}	714	1088
115	SEG_{58}	630	1088
116	SEG_{57}	546	1088
117	SEG_{56}	462	1088
118	SEG_{55}	378	1088
119	SEG_{54}	294	1088
120	SEG_{53}	210	1088

Pad	Symbol	X (µm)	Y (µm)
121	SEG_{52}	126	1088
122	SEG_{51}	42	1088
123	SEG_{50}	–42	1088
124	SEG_{49}	–126	1088
125	SEG_{48}	–210	1088
126	SEG_{47}	–294	1088
127	SEG_{46}	–378	1088
128	SEG_{45}	–462	1088
129	SEG_{44}	–546	1088
130	SEG_{43}	–630	1088
131	SEG_{42}	–714	1088
132	SEG_{41}	–798	1088
133	SEG_{40}	–882	1088
134	SEG_{39}	–966	1088
135	SEG_{38}	–1050	1088
136	SEG_{37}	–1134	1088
137	SEG_{36}	–1218	1088
138	SEG_{35}	–1302	1088
139	SEG_{34}	–1386	1088
140	SEG_{33}	–1470	1088
141	SEG_{32}	–1554	1088
142	SEG_{31}	–1638	1088
143	SEG_{30}	–1722	1088
144	SEG_{29}	–1806	1088
145	SEG_{28}	–1890	1088
146	SEG_{27}	–1974	1088
147	SEG_{26}	–2058	1088
148	SEG_{25}	–2142	1088
149	SEG_{24}	–2226	1088
150	SEG_{23}	–2310	1088
151	SEG_{22}	–2394	1088
152	SEG_{21}	–2478	1088
153	SEG_{20}	–2562	1088
154	SEG_{19}	–2646	1088
155	SEG_{18}	–2730	1088

Pad	Symbol	X (µm)	Y (µm)
156	SEG_{17}	–2814	1088
157	SEG_{16}	–2898	1088
158	SEG_{15}	–2982	1088
159	SEG_{14}	–3066	1088
160	SEG_{13}	–3150	1088
161	SEG_{12}	–3234	1088
162	SEG_{11}	–3318	1088
163	SEG_{10}	–3402	1088
164	SEG_{9}	–3486	1088
165	SEG_{8}	–3570	1088
166	SEG_{7}	–3654	1088
167	SEG_{6}	–3738	1088
168	SEG_{5}	–3822	1088
169	SEG_{4}	–3906	1088
170	SEG_{3}	–3990	1088
171	SEG_{2}	–4074	1088
172	SEG_{1}	–4158	1088
173	DUMMY	–4242	1088
174	DUMMY	–4326	1088
175	DUMMY	–4410	1088
176	DUMMY	–4494	1088
177	DUMMY	–4578	1088
178	DUMMY	–4662	1088
179	DUMMY	–4746	1088
180	DUMMY	–4830	1088
181	DUMMY	–4914	1088
182	DUMMY	–4998	1088
183	DUMMY	–5184	720
184	DUMMY	–5184	480
185	DUMMY	–5184	240
186	DUMMY	–5184	0
187	DUMMY	–5184	–240
188	DUMMY	–5184	–480
189	DUMMY	–5184	–720

ML9041A-xxACVWA ALIGNMENT MARK SPECIFICATION

Alignment Mark Coordinates

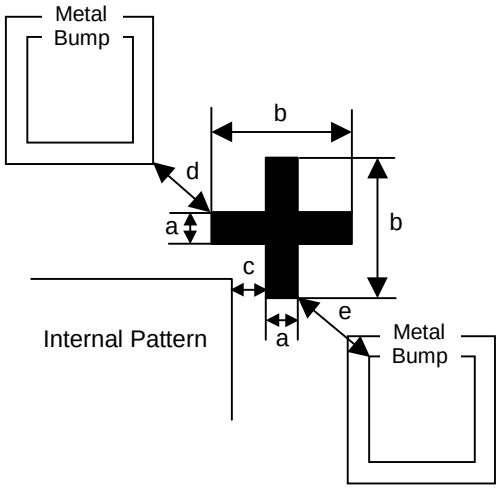


Alignment Mark	X (µm)	Y (µm)
A	–5100	960
B	5100	960
C	5100	–840

Alignment Mark Layer
Metal layers

Alignment Mark Specification

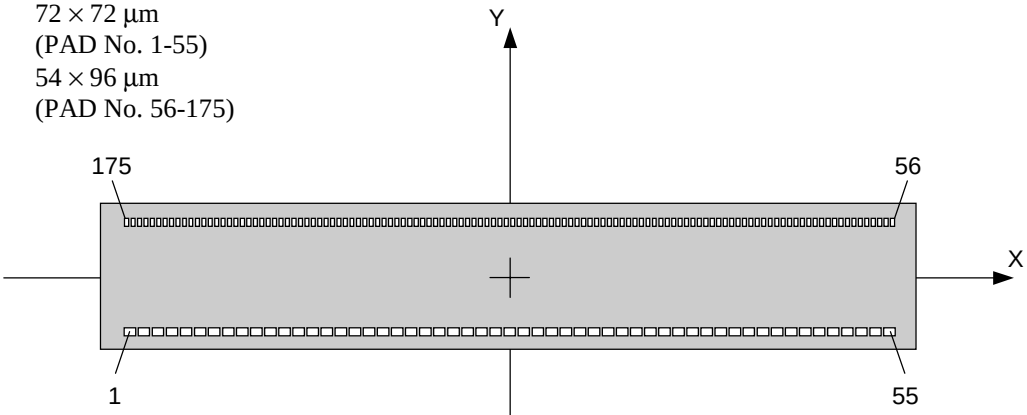
Symbol	Parameter	Mark	Size (µm)
a	Alignment Mark Width	—	25.2
b	Alignment Mark Size	—	100.2
c	Distance between Mark and Internal Pattern (MIN)	Mark A	26.8
		Mark B	17.1
		Mark C	87.3
d	Distance between Mark and Adjacent Pad Metal Layer (MIN)	Mark A	57.3
		Mark B	57.3
		Mark C	36.3
e	Distance between Mark and Adjacent Pad Bump (MIN)	Mark A	69.1
		Mark B	69.1
		Mark C	49.0



ML9041A-xxB CVWA PAD CONFIGURATION

Pad Layout

Chip Size: 10.62 × 2.55 mm
Chip Thickness: 625±20 µm
Bump Size (1): 72 × 72 µm
(PAD No. 1-55)
Bump Size (2): 54 × 96 µm
(PAD No. 56-175)



Note:
The ML9041A-xxB does not have the dummy pads corresponding to the pad numbers 56 to 62 and 183 to 189 for the ML9041A-xxA.

Pad Coordinates

Pad	Symbol	X (µm)	Y (µm)	Pad	Symbol	X (µm)	Y (µm)
1	V_1	–5103	–1100	21	DB_3	–1323	–1100
2	V_2	–4914	–1100	22	DB_2	–1134	–1100
3	V_{3A}	–4725	–1100	23	DB_1	–945	–1100
4	V_{3B}	–4536	–1100	24	DB_0	–756	–1100
5	V_4	–4347	–1100	25	E	–567	–1100
6	V_5	–4158	–1100	26	$R/\overline{W}$	–378	–1100
7	V_{5IN}	–3969	–1100	27	RS_0	–189	–1100
8	V_{CC}	–3780	–1100	28	RS_1	0	–1100
9	V_C	–3591	–1100	29	SO	189	–1100
10	V_{IN}	–3402	–1100	30	SI	378	–1100
11	BE	–3213	–1100	31	$\overline{SHT}$	567	–1100
12	V_{DD}	–3024	–1100	32	$\overline{CS}$	756	–1100
13	CSR	–2835	–1100	33	OSC_2	945	–1100
14	SSR	–2646	–1100	34	OSC_R	1134	–1100
15	$S/\overline{P}$	–2457	–1100	35	OSC_1	1323	–1100
16	V_{SS}	–2268	–1100	36	T_3	1512	–1100
17	DB_7	–2079	–1100	37	T_2	1701	–1100
18	DB_6	–1890	–1100	38	T_1	1890	–1100
19	DB_5	–1701	–1100	39	COM_1	2079	–1100
20	DB_4	–1512	–1100	40	COM_2	2268	–1100

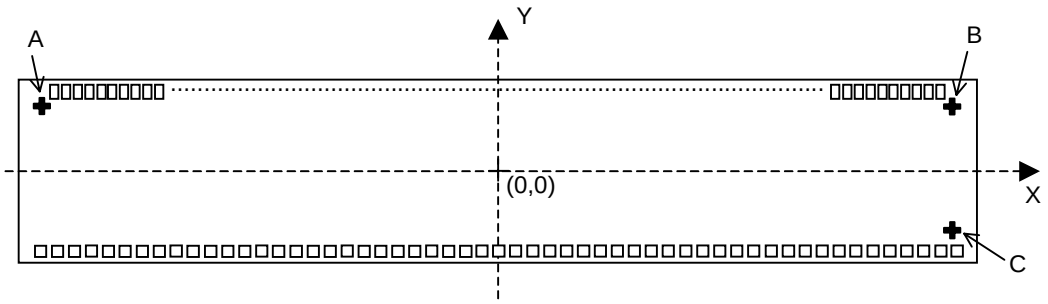
Pad	Symbol	X (µm)	Y (µm)	Pad	Symbol	X (µm)	Y (µm)
41	COM_3	2457	–1100	81	SEG_{85}	2898	1088
42	COM_4	2646	–1100	82	SEG_{84}	2814	1088
43	COM_5	2835	–1100	83	SEG_{83}	2730	1088
44	COM_6	3024	–1100	84	SEG_{82}	2646	1088
45	COM_7	3213	–1100	85	SEG_{81}	2562	1088
46	COM_8	3402	–1100	86	SEG_{80}	2478	1088
47	COM_9	3591	–1100	87	SEG_{79}	2394	1088
48	COM_{10}	3780	–1100	88	SEG_{78}	2310	1088
49	COM_{11}	3969	–1100	89	SEG_{77}	2226	1088
50	COM_{12}	4158	–1100	90	SEG_{76}	2142	1088
51	COM_{13}	4347	–1100	91	SEG_{75}	2058	1088
52	COM_{14}	4536	–1100	92	SEG_{74}	1974	1088
53	COM_{15}	4725	–1100	93	SEG_{73}	1890	1088
54	COM_{16}	4914	–1100	94	SEG_{72}	1806	1088
55	COM_{17}	5103	–1100	95	SEG_{71}	1722	1088
56	DUMMY	4998	1088	96	SEG_{70}	1638	1088
57	DUMMY	4914	1088	97	SEG_{69}	1554	1088
58	DUMMY	4830	1088	98	SEG_{68}	1470	1088
59	DUMMY	4746	1088	99	SEG_{67}	1386	1088
60	DUMMY	4662	1088	100	SEG_{66}	1302	1088
61	DUMMY	4578	1088	101	SEG_{65}	1218	1088
62	DUMMY	4494	1088	102	SEG_{64}	1134	1088
63	DUMMY	4410	1088	103	SEG_{63}	1050	1088
64	DUMMY	4326	1088	104	SEG_{62}	966	1088
65	DUMMY	4242	1088	105	SEG_{61}	882	1088
66	SEG_{100}	4158	1088	106	SEG_{60}	798	1088
67	SEG_{99}	4074	1088	107	SEG_{59}	714	1088
68	SEG_{98}	3990	1088	108	SEG_{58}	630	1088
69	SEG_{97}	3906	1088	109	SEG_{57}	546	1088
70	SEG_{96}	3822	1088	110	SEG_{56}	462	1088
71	SEG_{95}	3738	1088	111	SEG_{55}	378	1088
72	SEG_{94}	3654	1088	112	SEG_{54}	294	1088
73	SEG_{93}	3570	1088	113	SEG_{53}	210	1088
74	SEG_{92}	3486	1088	114	SEG_{52}	126	1088
75	SEG_{91}	3402	1088	115	SEG_{51}	42	1088
76	SEG_{90}	3318	1088	116	SEG_{50}	–42	1088
77	SEG_{89}	3234	1088	117	SEG_{49}	–126	1088
78	SEG_{88}	3150	1088	118	SEG_{48}	–210	1088
79	SEG_{87}	3066	1088	119	SEG_{47}	–294	1088
80	SEG_{86}	2982	1088	120	SEG_{46}	–378	1088

Pad	Symbol	X (μm)	Y (μm)
121	SEG_{45}	–462	1088
122	SEG_{44}	–546	1088
123	SEG_{43}	–630	1088
124	SEG_{42}	–714	1088
125	SEG_{41}	–798	1088
126	SEG_{40}	–882	1088
127	SEG_{39}	–966	1088
128	SEG_{38}	–1050	1088
129	SEG_{37}	–1134	1088
130	SEG_{36}	–1218	1088
131	SEG_{35}	–1302	1088
132	SEG_{34}	–1386	1088
133	SEG_{33}	–1470	1088
134	SEG_{32}	–1554	1088
135	SEG_{31}	–1638	1088
136	SEG_{30}	–1722	1088
137	SEG_{29}	–1806	1088
138	SEG_{28}	–1890	1088
139	SEG_{27}	–1974	1088
140	SEG_{26}	–2058	1088
141	SEG_{25}	–2142	1088
142	SEG_{24}	–2226	1088
143	SEG_{23}	–2310	1088
144	SEG_{22}	–2394	1088
145	SEG_{21}	–2478	1088
146	SEG_{20}	–2562	1088
147	SEG_{19}	–2646	1088
148	SEG_{18}	–2730	1088

Pad	Symbol	X (μm)	Y (μm)
149	SEG_{17}	–2814	1088
150	SEG_{16}	–2898	1088
151	SEG_{15}	–2982	1088
152	SEG_{14}	–3066	1088
153	SEG_{13}	–3150	1088
154	SEG_{12}	–3234	1088
155	SEG_{11}	–3318	1088
156	SEG_{10}	–3402	1088
157	SEG_{9}	–3486	1088
158	SEG_{8}	–3570	1088
159	SEG_{7}	–3654	1088
160	SEG_{6}	–3738	1088
161	SEG_{5}	–3822	1088
162	SEG_{4}	–3906	1088
163	SEG_{3}	–3990	1088
164	SEG_{2}	–4074	1088
165	SEG_{1}	–4158	1088
166	DUMMY	–4242	1088
167	DUMMY	–4326	1088
168	DUMMY	–4410	1088
169	DUMMY	–4494	1088
170	DUMMY	–4578	1088
171	DUMMY	–4662	1088
172	DUMMY	–4746	1088
173	DUMMY	–4830	1088
174	DUMMY	–4914	1088
175	DUMMY	–4998	1088

ML9041A-xxBCVWA ALIGNMENT MARK SPECIFICATION

Alignment Mark Coordinates



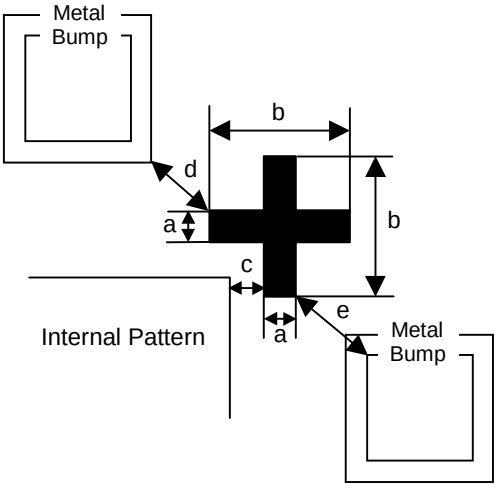
Alignment Mark	X (µm)	Y (µm)
A	–5100	960
B	5100	960
C	5100	–840

Alignment Mark Layer

Metal layers

Alignment Mark Specification

Symbol	Parameter	Mark	Size (µm)
a	Alignment Mark Width	—	25.2
b	Alignment Mark Size	—	100.2
c	Distance between Mark and Internal Pattern (MIN)	Mark A	26.8
		Mark B	17.1
		Mark C	87.3
d	Distance between Mark and Adjacent Pad Metal Layer (MIN)	Mark A	57.3
		Mark B	57.3
		Mark C	164.7
e	Distance between Mark and Adjacent Pad Bump (MIN)	Mark A	69.1
		Mark B	69.1
		Mark C	173.7



ML9041A-xxA/xxBCVWA GOLD BUMP SPECIFICATION

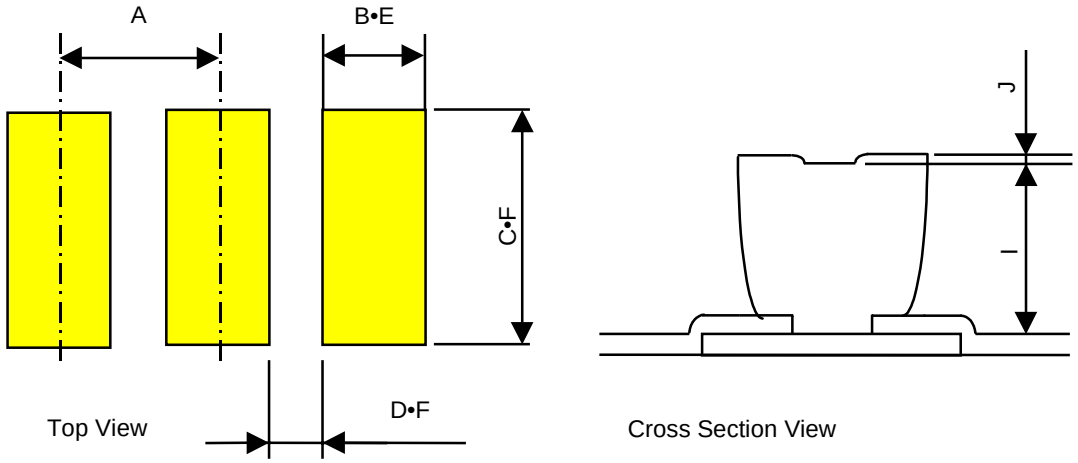
Gold Bump Specification

(Unit: μm)

Symbol	Parameter	MIN	TYP	MAX
A	Bump Pitch (Min Section: Output Section)	84	—	—
B	Bump Size (Output Section: Pitch Direction)	49	54	59
C	Bump Size (Output Section: Depth Direction)	91	96	101
D	Bump-to-Bump Distance (Output Section: Pitch Direction)	25	30	35
E	Bump Size (Input Section: Pitch Direction)	67	72	77
F	Bump Size (Input Section: Depth Direction)	67	72	77
G	Bump-to-Bump Distance (Input Section: Pitch Direction)	112	117	122
H	Sliding of Total Bump Pitches	—	—	2
I	Bump Height	10	15	20
	Bump Height Dispersion Inside Chip (Range)	—	—	4
J	Bump Edge Height	—	—	5
K	Shear Strength (g)	30	—	—
L	Bump Hardness (Hv: 25 g load)	50	90	130

■ Chip Size; 10.62 mm × 2.55 mm
■ Chip Thickness; 625 ±20 μm

Top View and Cross Section View



REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
Version1	Dec. 2001	–	–	Preliminary first edition
PEDL9041A-02	Mar. 15, 2002	1	1	Partially changed the content of Section "FEATURES".
		5	5	Changed descriptions of Symbol BE. Changed descriptions of Symbols V_C and V_{CC}.
		6	6	Changed description of Symbol S/$\overline{P}$. Added Symbol DUMMY and descriptions.
		8	8	Integrated Parameters " "H" Input Voltage 1" and " "H" Input Voltage 2", and Parameters " "L" Input Voltage 1" and " "L" Input Voltage 2". Changed Min. value of " "L" input voltage" from –0.3 to 0. Changed condition of Parameter "Input Current 2" from $V_1 = V_{DD}$ to V_1 = GND. Changed a symbol in column "Applicable pin" from CS to $\overline{CS}$.
		10	10	Changed Note 6.
		12	12	Added Note.
		13	13	Added $\overline{CS}$ "H" pulse width.
		19	19	Partially changed Section (1) of 1).
		20	20	Partially changed Section (2).
		21	21	Partially changed Section "Arbitrator RAM (ABRAM)".
		27	27	Changed the figure for ADC.
		32	32	Changed timing diagrams. Added Note 3.
		35	35	Partially changed Section 3). Changed caption 4) from "Display Mode Setting" to "Display ON/OFF Control". Partially changed Section (1) of 4).
		36	36	Partially changed Section (3) of 6).
		37	37	Partially changed Section 7), Section 8), and Section 9).
		38	38	Partially changed Section 11).
		40	40	Partially changed Section 4).
		53	53	Partially added the content of Section 4) in (C).

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